A Critical Assessment of the State of the Art in Multiscale Multiphysics Modeling of Microelectronics

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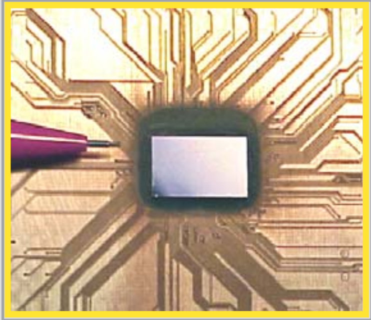
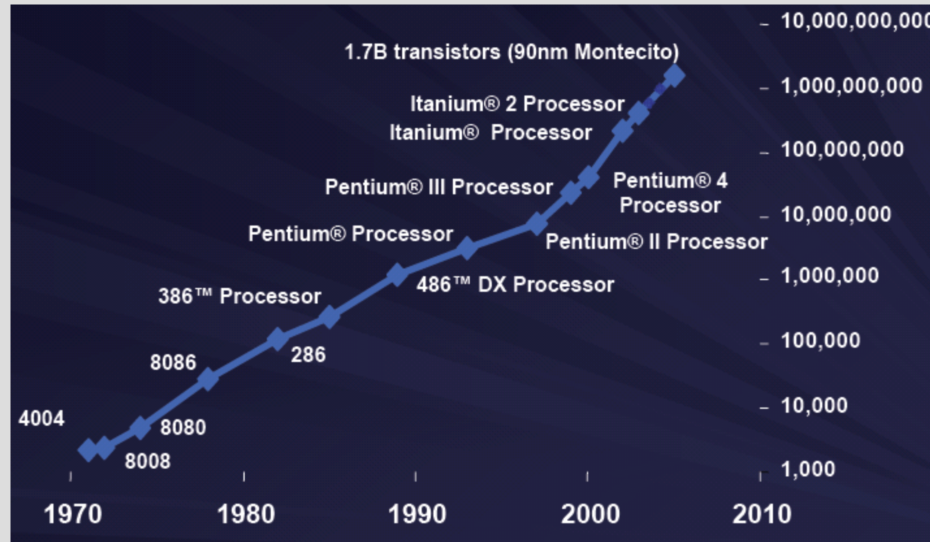
Multiscale

Silicon Die (10^{-2}m)



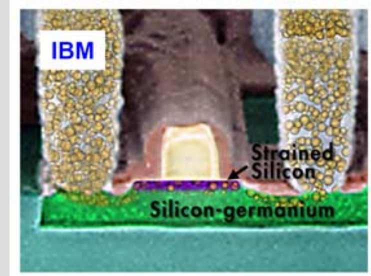
Package (10^{-2} m)

Heat Sink (10^{-1}m)



System (10^{0} m)

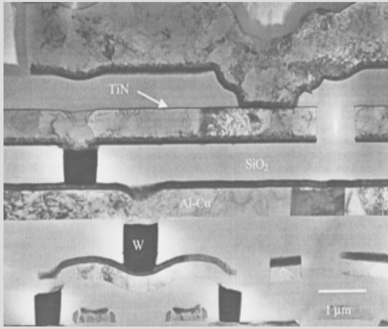
Transistor (10^{-9} m)



Ravi Mahajan: Intel

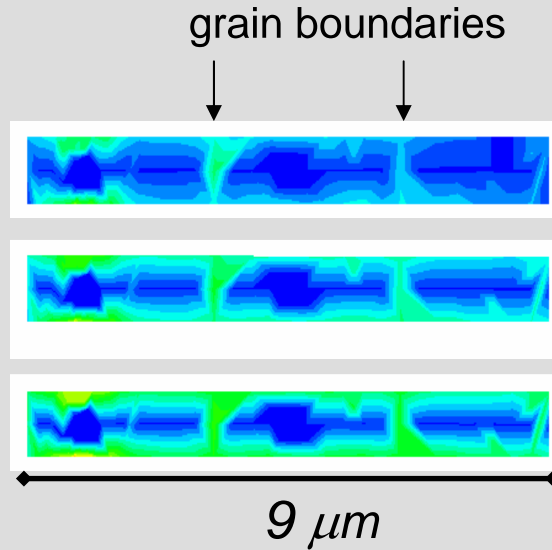
Facility (10^{2} m)

Multiphysics

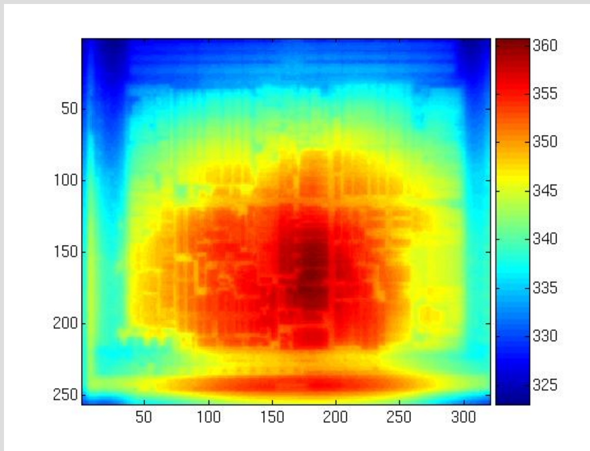


TEM cross-section of a multilevel interconnect, Intel Corp.(2000)

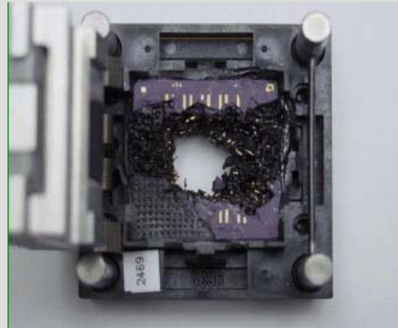
grain boundaries

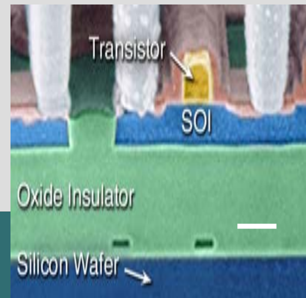


M. Cuitiño, M. Koslowski, M. Ortiz, D. Pantusso and S. Shankar, 2004



F.J. Mesa-Martinez, et al, 2007.

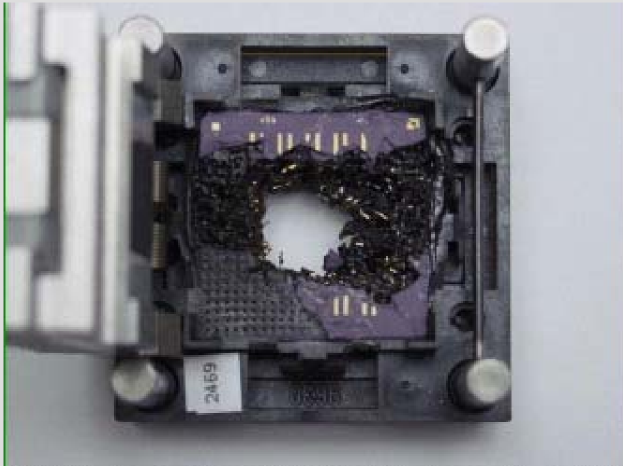




Electrical performance and mechanical integrity linked strongly to temperature.

Correct prediction of temperature coupled to power essential at a range of scales!

Motivation for Thermally-Aware Circuit Design



Thermal Runaway

- Decrease in V_{DD} has necessitated drop V_t and increase in sub-threshold leakage
- Exponential dependence of leakage current on local temperature
- Large range of scales
  - Transistors ~100 nm
  - Gate ~ 500 nm
  - Circuits ~10-100 microns
  - Spot cooling ~100's of microns
- Multi-scale simulation necessary

Integrated Electrothermal Optimization Engine

Architectural Level
Microarch. design,
multicore tradeoffs

~10 blocks

1 mm-2 cm

RTL Level
Task Migration,
performance mitigation,
floorplanning

~100 blocks

100 μm – 1 mm

Logic/Circuit Level
ET placement, routing,
performance mitigation

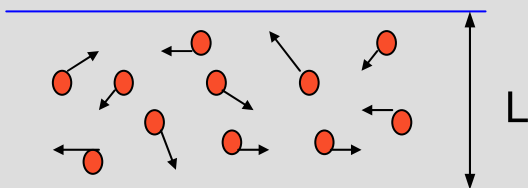
~10K-10M blocks

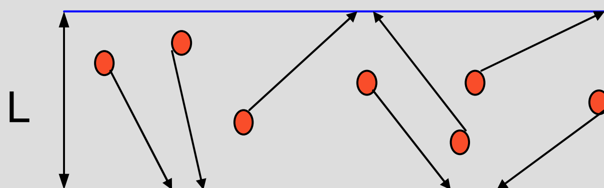
100 nm – 100 μm

Adapted from
Sapatnekar, 2007

Electrothermal Transport at Device Scale

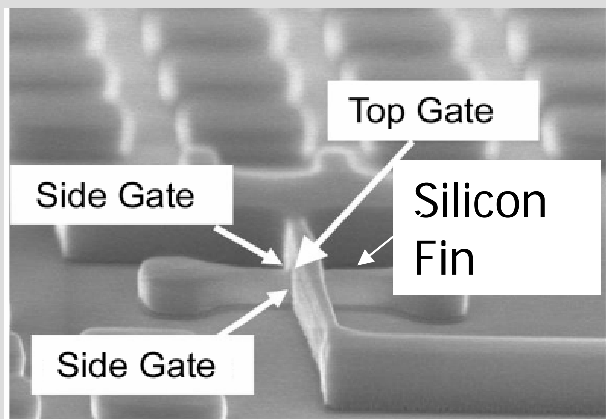
Sub-micron Heat Conduction in Semiconductors and Dielectrics





(a) $\Lambda << L$
Fourier's Law valid

(b) $\Lambda >> L$
Fourier's Law invalid

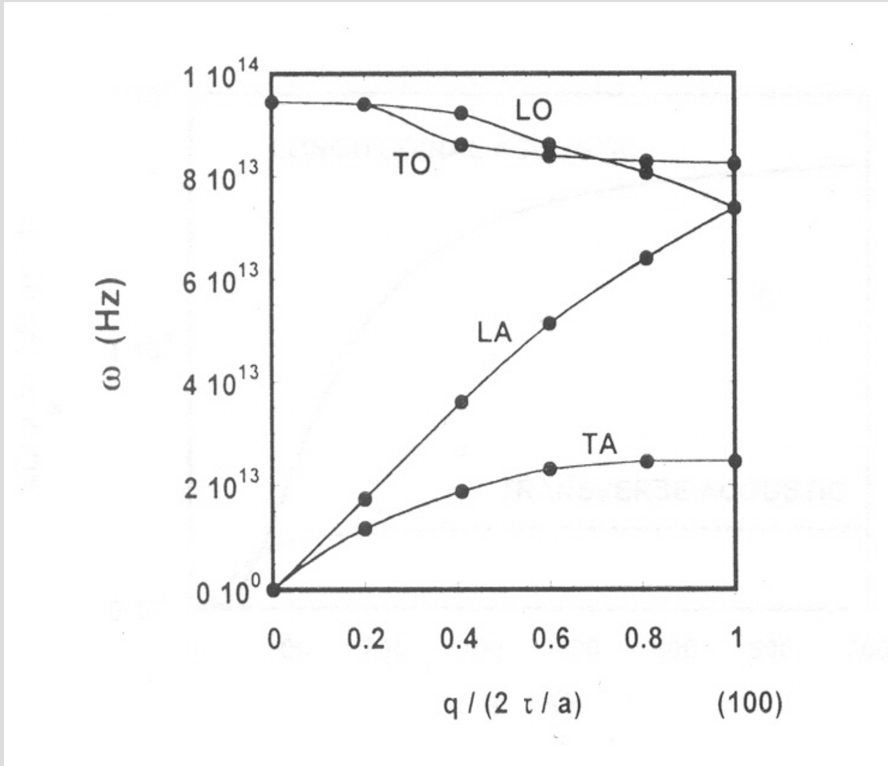


http://www.intel.com/pressroom/archive/releases/20030612tech.htm

Tri Gate

- Phonons are quanta of lattice vibrations.
- Main carriers of energy in semiconductors and dielectrics.
- In many emerging devices, length scales fall in Regime (b)

Heat Transport in Solids

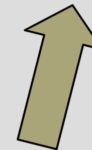


Frequency vs. reduced wave number in (100) direction for silicon

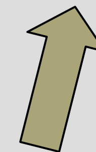
Boltzmann transport equation for phonons:

$$\frac{\partial f}{\partial t} + \nabla \cdot (\boldsymbol{v} f) = \left(\frac{\partial f}{\partial t}\right)_{scat.}$$

$$= \frac{f^0 - f}{\tau}$$



Ballistic term

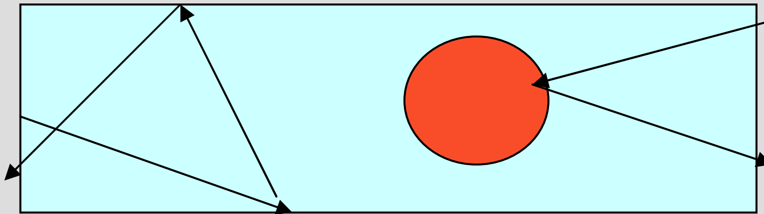
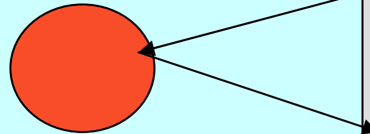
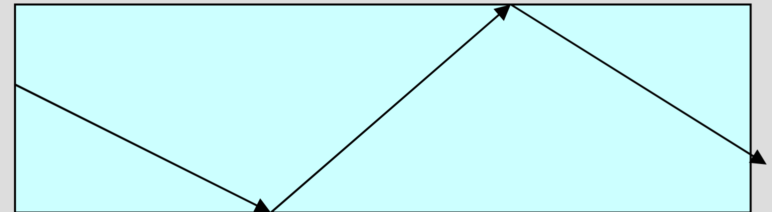


Relaxation time approximation

Phonons are characterized by (**r**, t, **K**) and polarization

What Happens on the Nanoscale?

- Boundary scattering critical as surface to volume ratio decreases
- Scattering retards forward progress and decreases energy transfer from one boundary to another
- Phonon confinement effects decrease phonon group velocity
- Predominance of interfaces increases the important of interface resistance (Kapitza resistance)

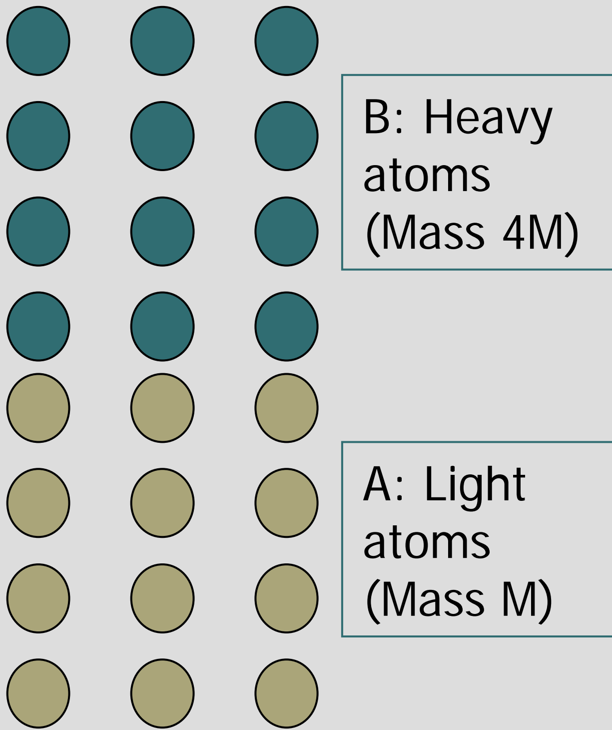




Diffuse boundary scattering

Scattering on impurities

Specular boundary scattering

Interface Physics: Acoustic Impedance



transmission

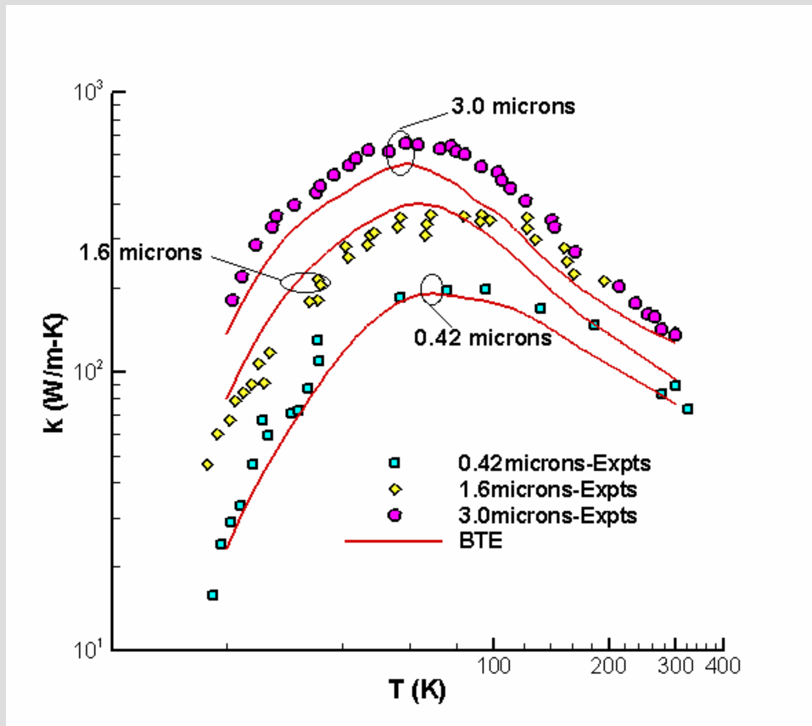
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

0 2 4 6 8 10 12

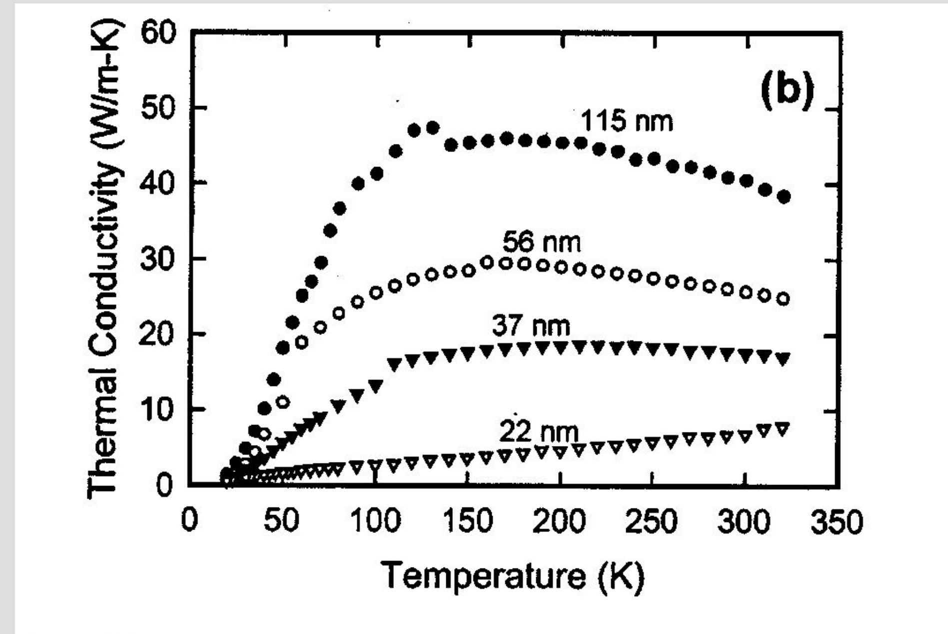
frequency (THz)

Frequency-dependent transmissivity of LA phonons across interface (Lin and Murthy, 2006)

Thermal Conductivity Reduction



Lateral Thermal Conductivity of Silicon Thin Films



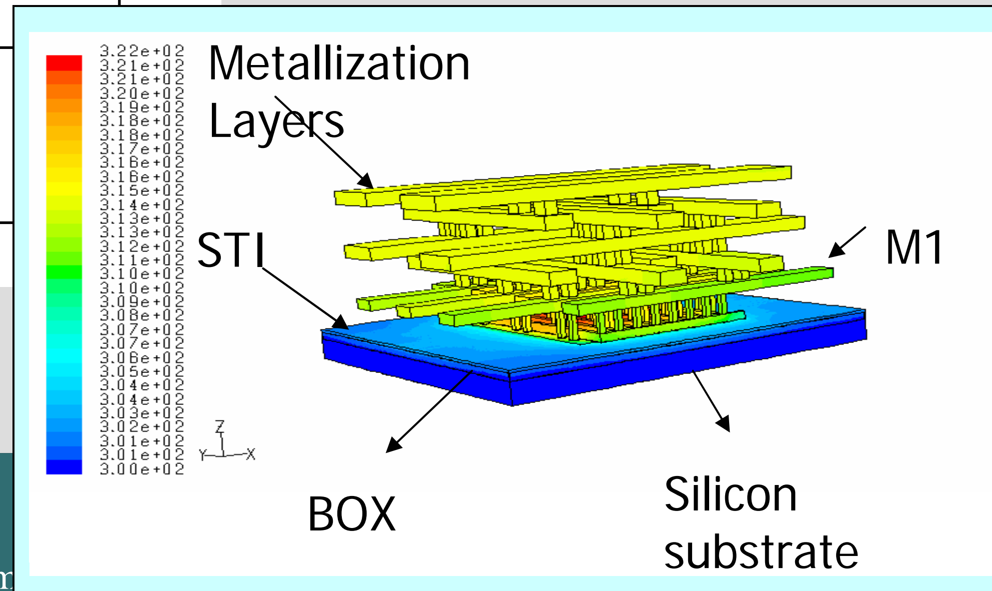
Axial Thermal Conductivity of Silicon Nanowires

Data: Asheghi et al, 2002; Simulation: Narumanchi et al, 2005

D. Li et al (2003)

Temperature Comparison

Computation for *0.15 mW/µm*	Maximum temperature rise
Fourier	*13.25 K*
Gray	*20.85 K*
Non-gray (100 % optical)	*35.29 K*
Non-gray (85 % optical)	*32.33 K*



What's Missing?

- Nearly all available device simulators lack sub-micron thermal physics
- Little attention to interfaces
- Drift-diffusion/Fourier conduction increasingly invalid as channel lengths fall below phonon mean free path (~300 nm)
- Power estimation through drift-diffusion solvers for charge transport
  - hot-spot may be displaced by ~30 nm
- Few self-consistent solvers
- Expensive to compute – how to include into larger-scale models?

Integration of Electrothermal Transport at Larger Scales

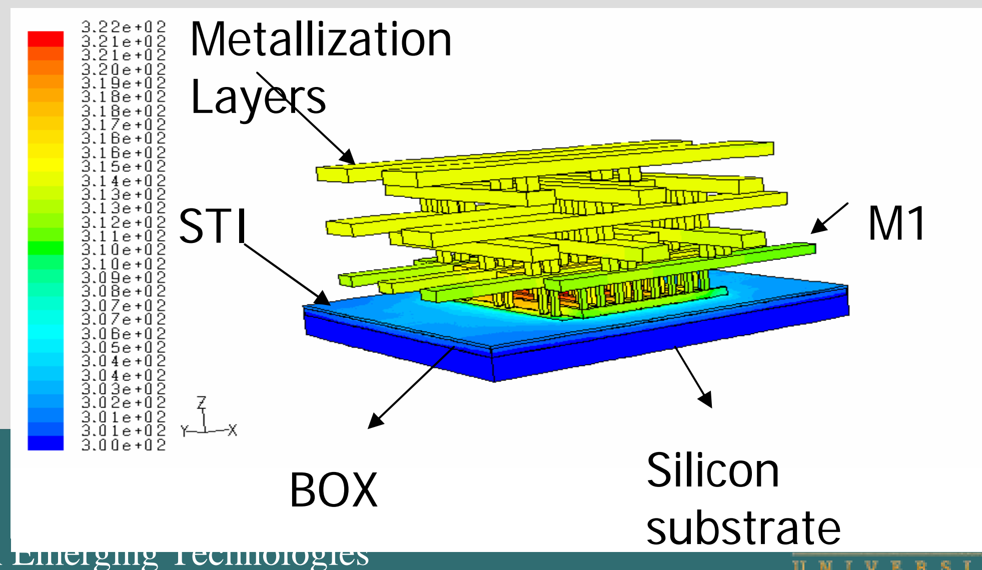
Thermal Runaway: Previous Work

- Thermal runaway calculations based on junction temperature

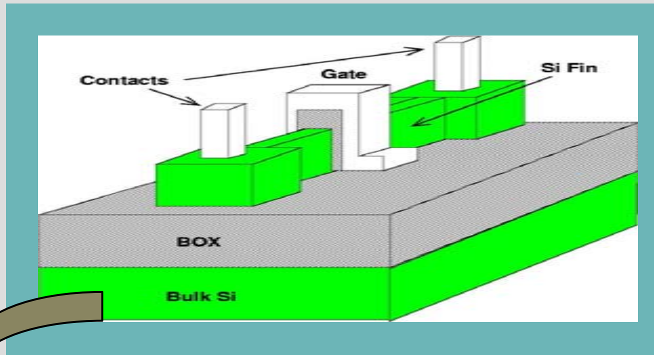
$$T_j = T_a - P_{total}\left(T_j\right)\theta_{ja}$$

- θ_{ja} is a measure of *overall* package resistance
- Not much use in dealing with *local* phenomena
- Can we use more sophisticated (and local) measures of thermal resistance?

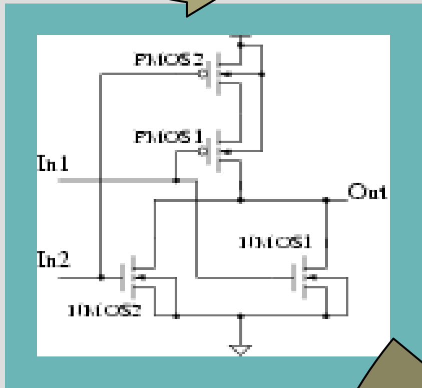
PDSOI nFET using phonon BTE in channel region and Fourier conduction elsewhere



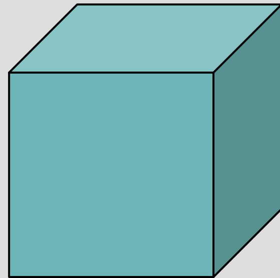
Compact Model Creation



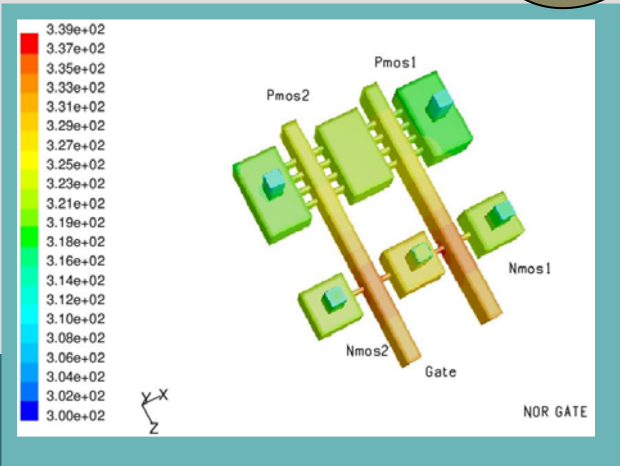
Transistor Level: FinFET



NOR gate composed of PMOS and NMOS FinFETs

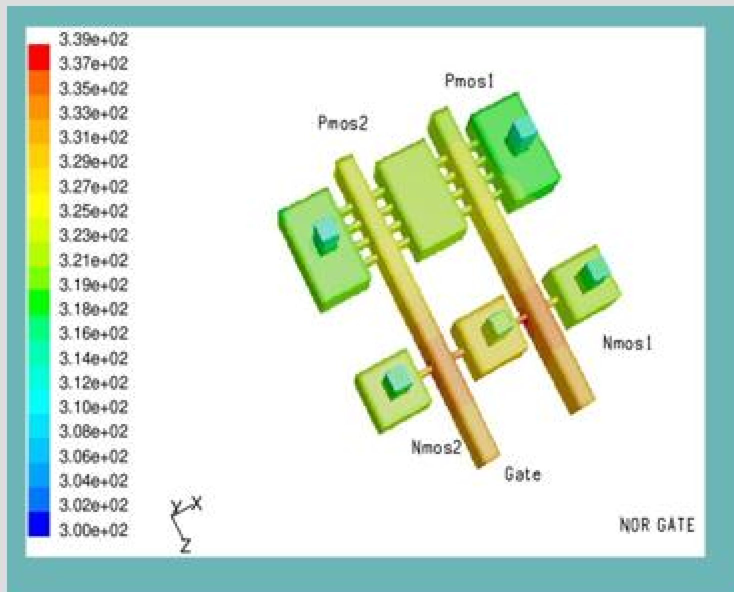


Compact thermal model of NOR gate



Detailed thermal model of NOR gate

Detailed Gate Level Models



- NAND gate, NOR gate and inverter (INV) considered
- 28 nm technology
- Metallic contacts included but not metallization layers
- Source, drain, gate, channel included
- Fourier conduction assumed
- Volumetric heat generation using TAURUS

Cell-Level Compact Thermal Model

- Represent each gate by a cuboidal cell with six given boundary temperatures
- Write cell average temperature as

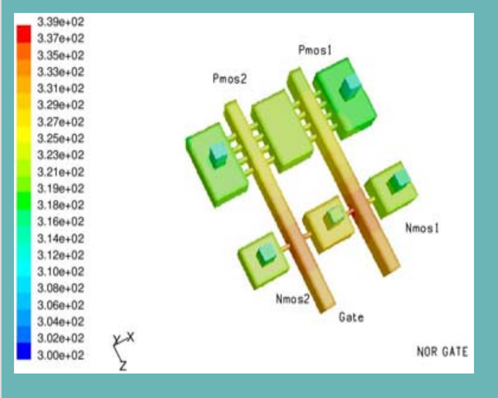
$$T_{avg} = \sum_{f=1}^{6} a_f T_f + a_0 \alpha q$$

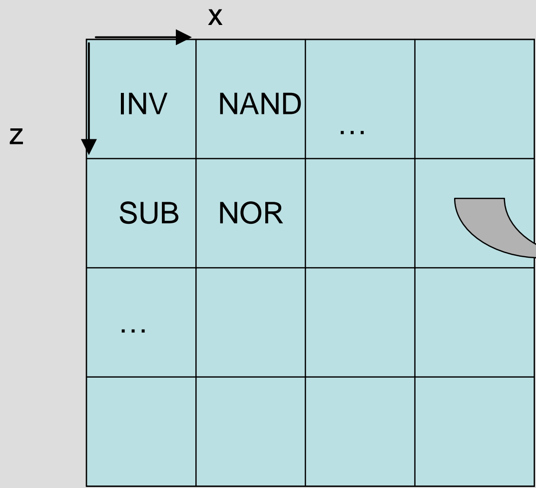
- The six face heat transfer rates also written as

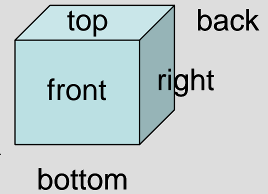
$$q_{bj} = \sum_{f=1}^{6} b_{fj} T_f + b_{0j} \alpha q \quad \text{j=1,2,...6}$$

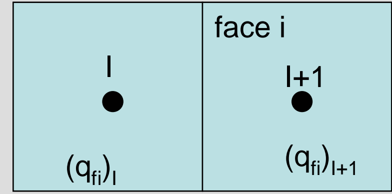
- Determine *a* and *b* coefficients by doing seven runs with seven linearly independent boundary condition sets
- α = activity; q = heat generation rate
- T_f = boundary face temperature

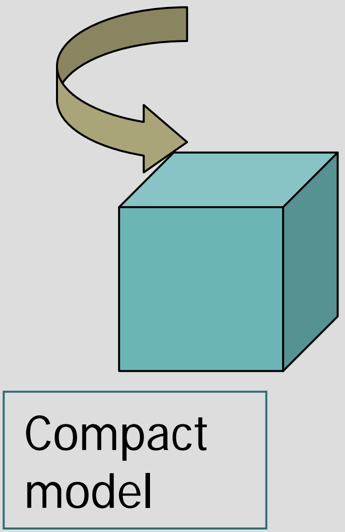
Multiscale Simulation









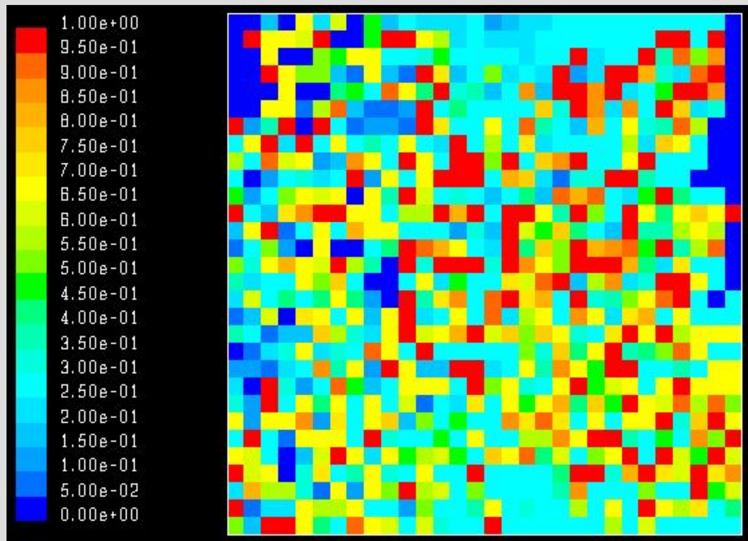


Compact model

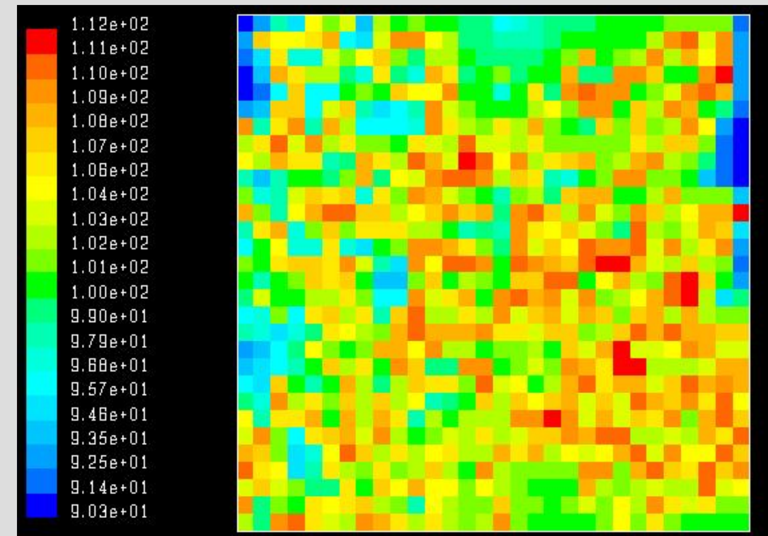
Cooling devices may also be included in thermal floor plan if desired

Cell and face heat balances yield coupled equation set for cell temperatures

X3 Benchmark Circuit



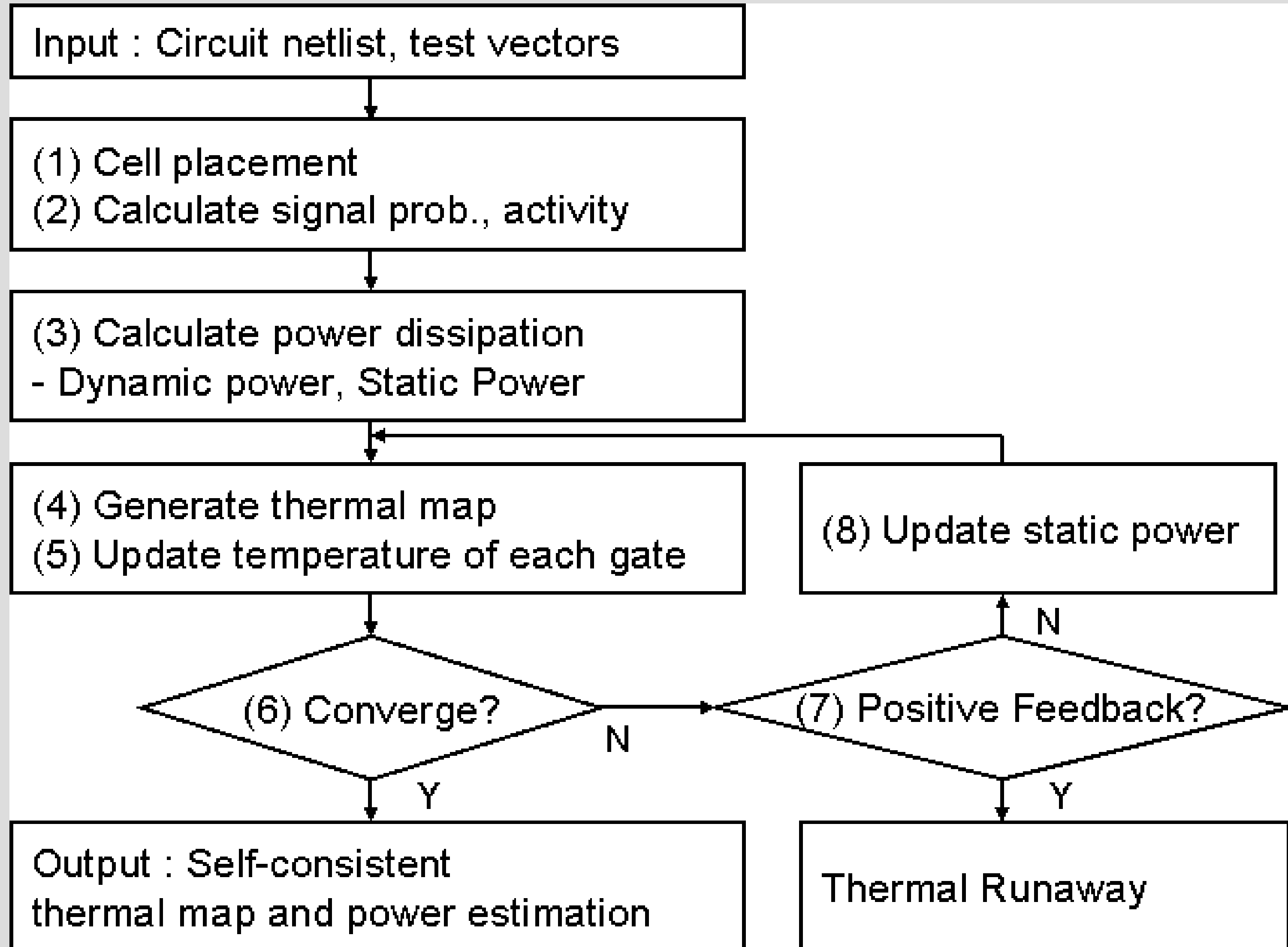
Dynamic Power



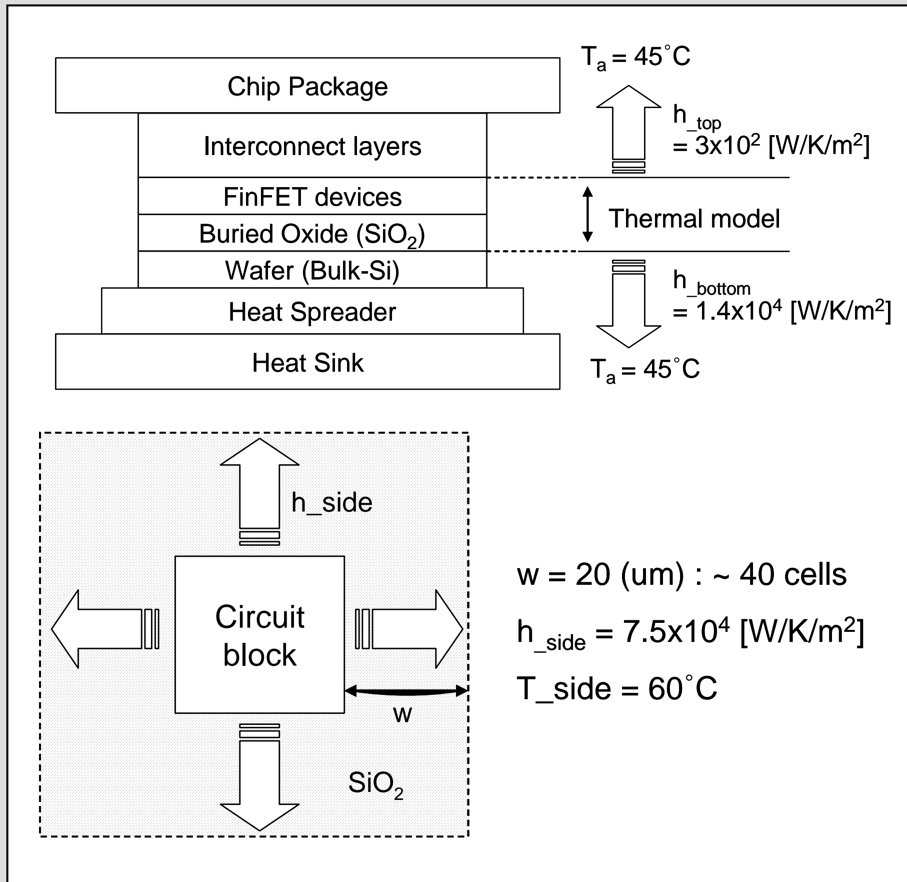
Temperature Map

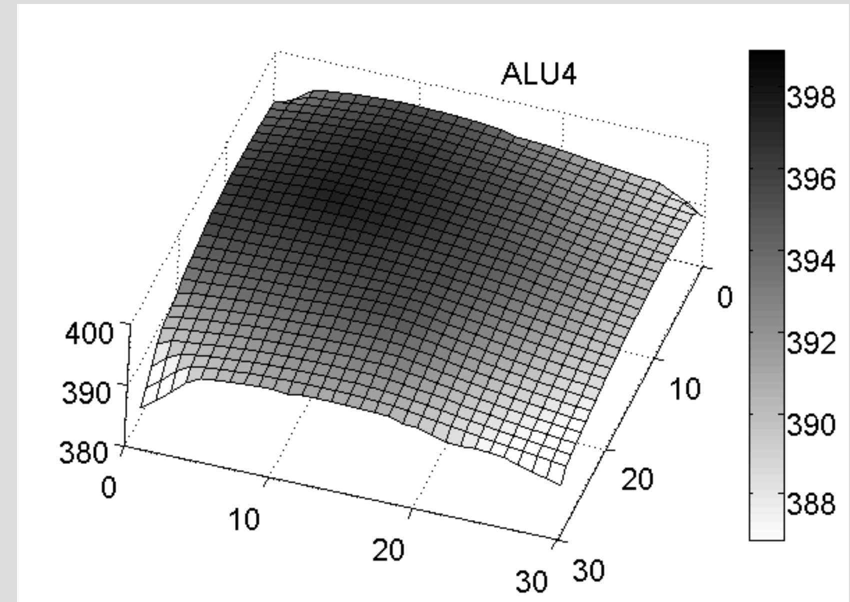
Benchmark circuit contains 900 cells and about 3000-4000 transistors

Self-Consistent Simulation



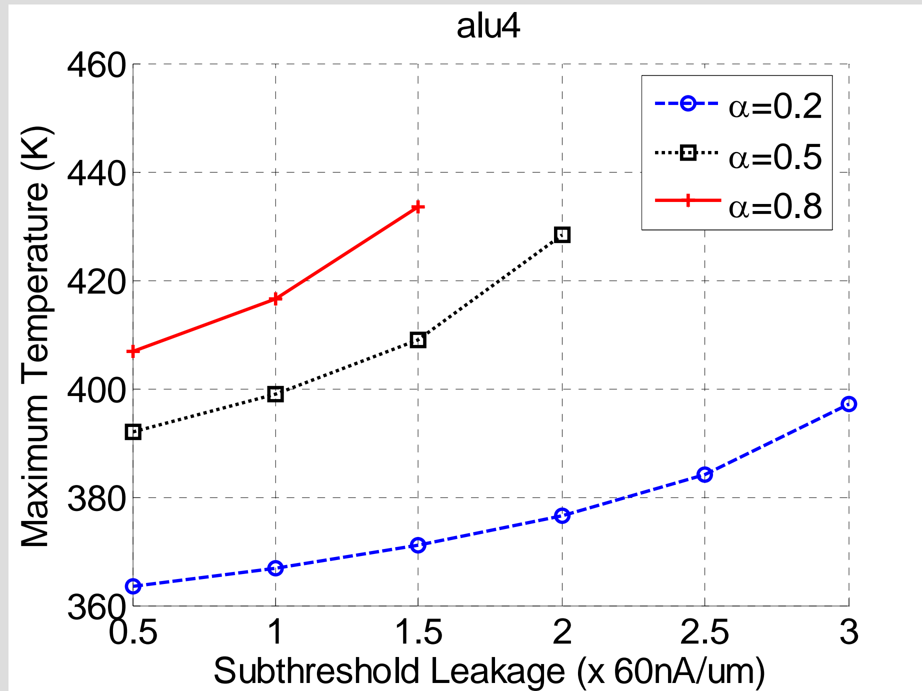
Example: ALU4 Benchmark Circuit





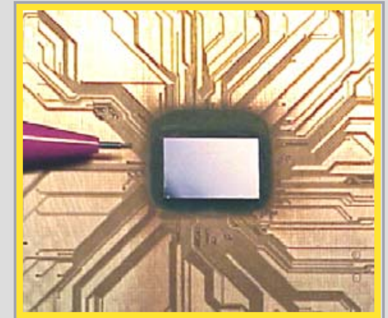
Typical temperature map

Effect of Activity



- Subthreshold leakage value shown is at room temperature
- At $\alpha=0.8$, thermal runaway occurs for I >120 nA/um
- At $\alpha=0.5$, thermal runaway occurs for I>150 nA/um

Current State of the Art



- Sheer geometric complexity
  - Most CAD tools cannot handle
- Sub-micron physics not included
  - Important for device/gate/circuit scale
  - Interface resistance important for local temperature
- Multiscale resolution
  - Impossible to handle all scales
  - "Compacting" at smaller scales essential
  - Take care how tool is used – sub-micron effects important!
- Multiphysics
  - Nearly all available analysis tools are single-domain
  - Some degree of coupling in the electro-thermal domain (power-Fourier conduction)
  - Some degree of coupling of thermo-mechanical phenomena (stress-Fourier conduction)
  - Thermal boundary conditions on die tied to package-level thermals – currently no direct or easy tie to packages such as ICEPAK