

Power Delivery Challenges for The Mobile Platforms

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Mobile Platform Architecture Development

Agenda

- Why Energy Efficiency
 - Power Delivery is an important piece of Energy Efficiency
- Mobile Platform Power Challenges
 - Thermal Design Power Load - 10W Reduction From Previous Generations
 - 45 nm Process Technology
 - Managing Variations and Design Methodology
 - Energy Star and Battery Life Loads
 - Power Delivery Challenges
- Summary and Conclusions

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Premium Price of the Energy Efficiency

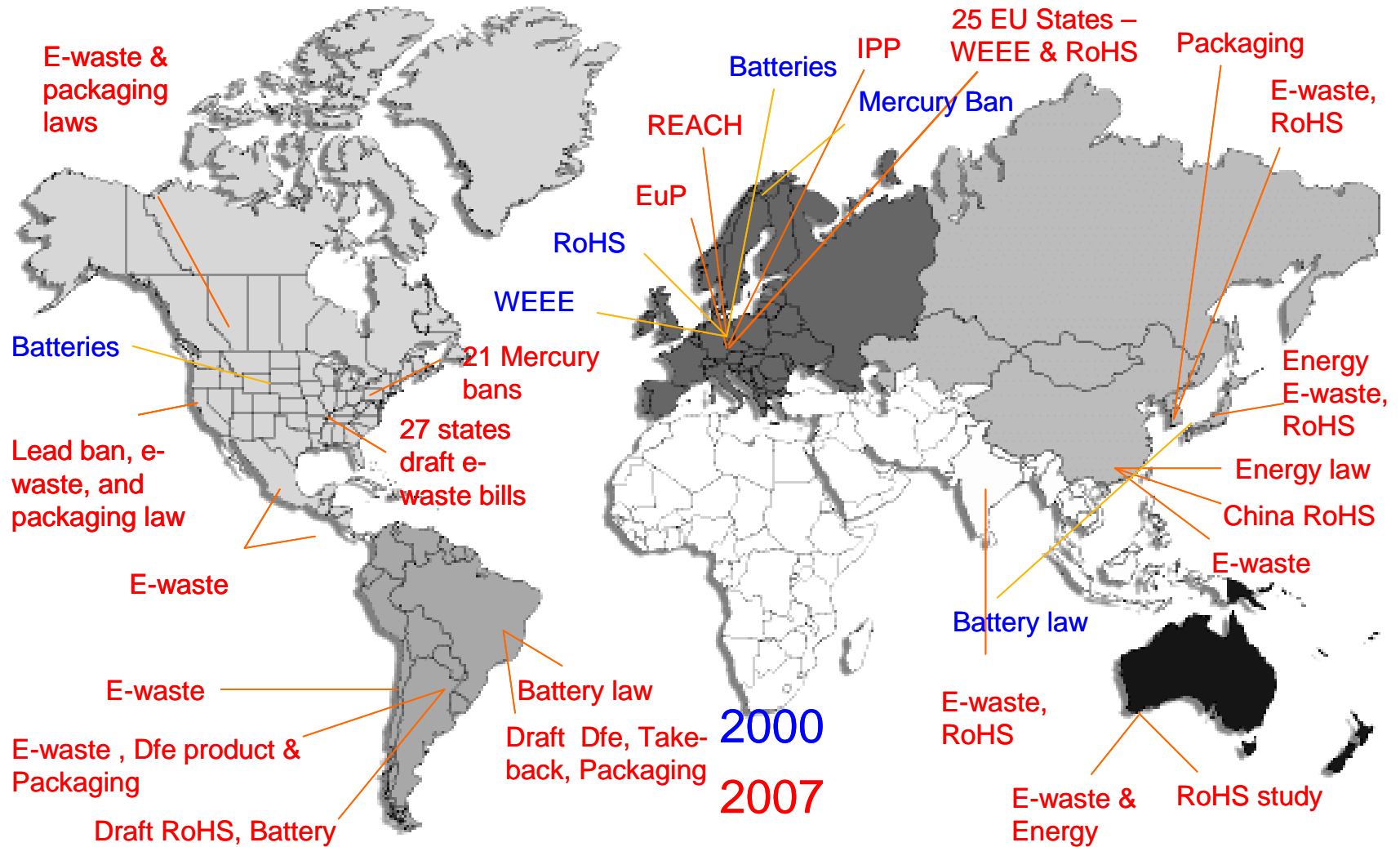
Source: NPD, 2000

Prices of Non-Energy Star vs. Energy Star Appliances

Category	Average Price of Non-Energy Star	Average Price of Energy Star	Energy Star Price Premium
Dishwashers	\$376	\$404	7 %
Air Conditioners	\$257	\$279	9 %
Washing Machines	\$379	\$869	129 %
Refrigerators	\$650	\$1,118	72 %

Energy Star appliances command premium prices. In spite of the premium, the study indicates consumers are shopping for energy efficiency.

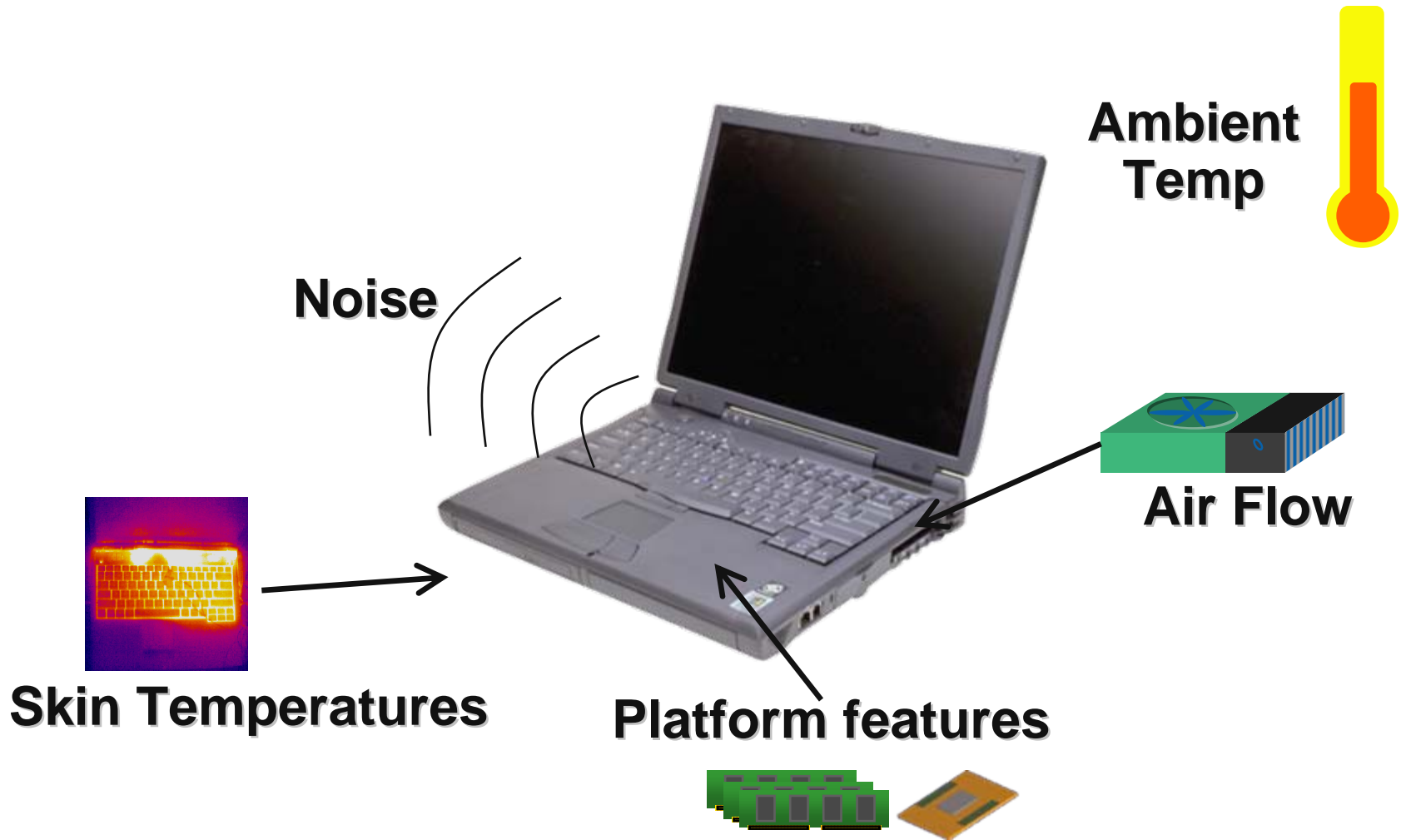
Regulation explodes – EU leading



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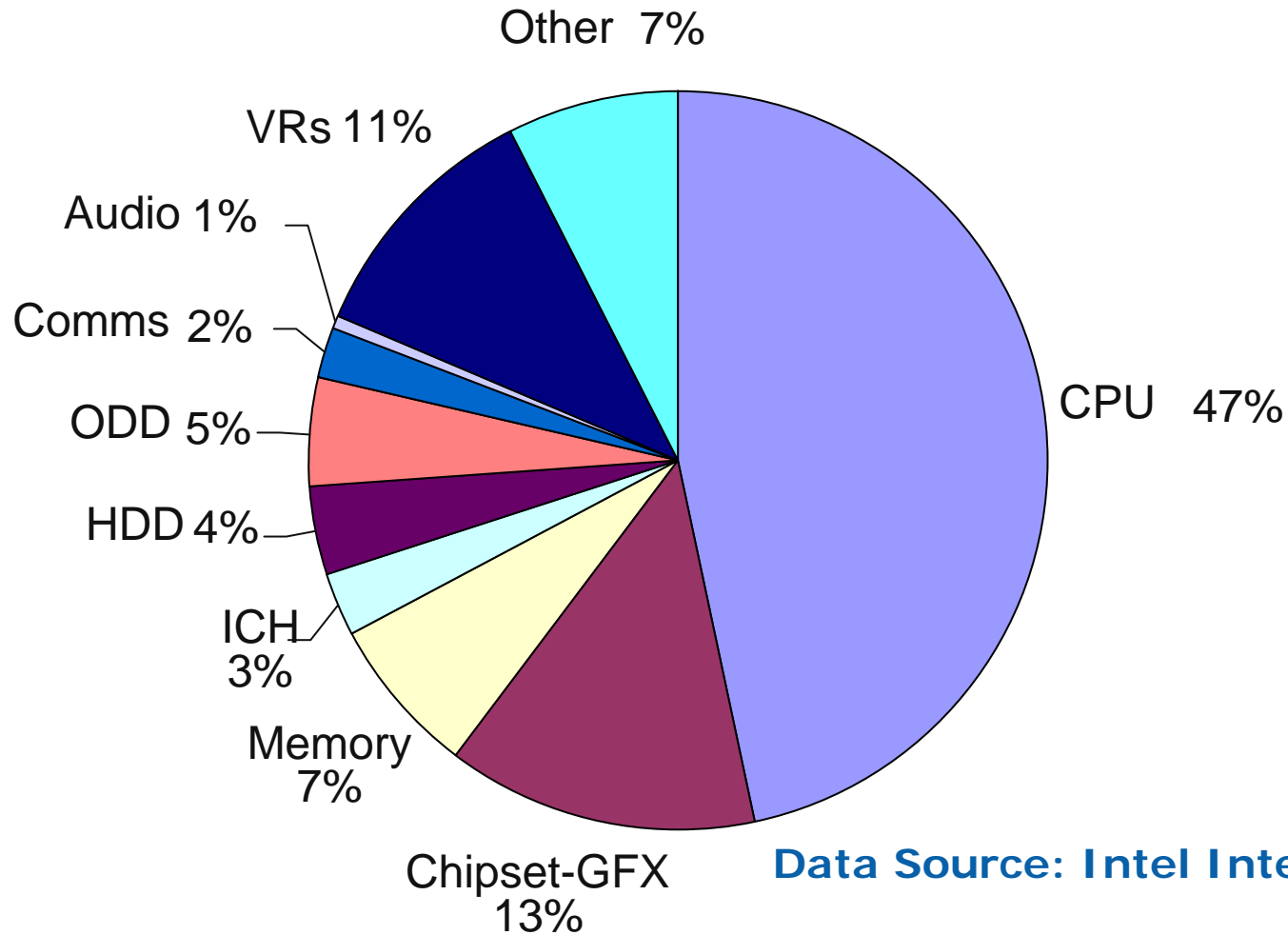
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Cooling Thermal Design – Balanced Platforms



In a Well Balanced Platform, All Limits are Reached Equally

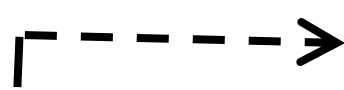
Thermal Design Power For a Typical Platform



CPU is Major Component In Determining Thermal Impedance

Platform Drives Component Power Targets

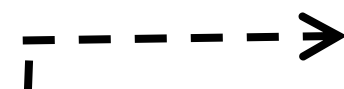
- Heat Removal



**Thermal Impedance
Cost, and Form Factor**

$$T_j = T_a + \theta_{ja} P$$

- Power Delivery



**Electrical Impedance
Cost, Form Factor
Impact**

$$V_j = V_{id} - Z_e I$$

Two Platform Impedances Drive Component Power Targets

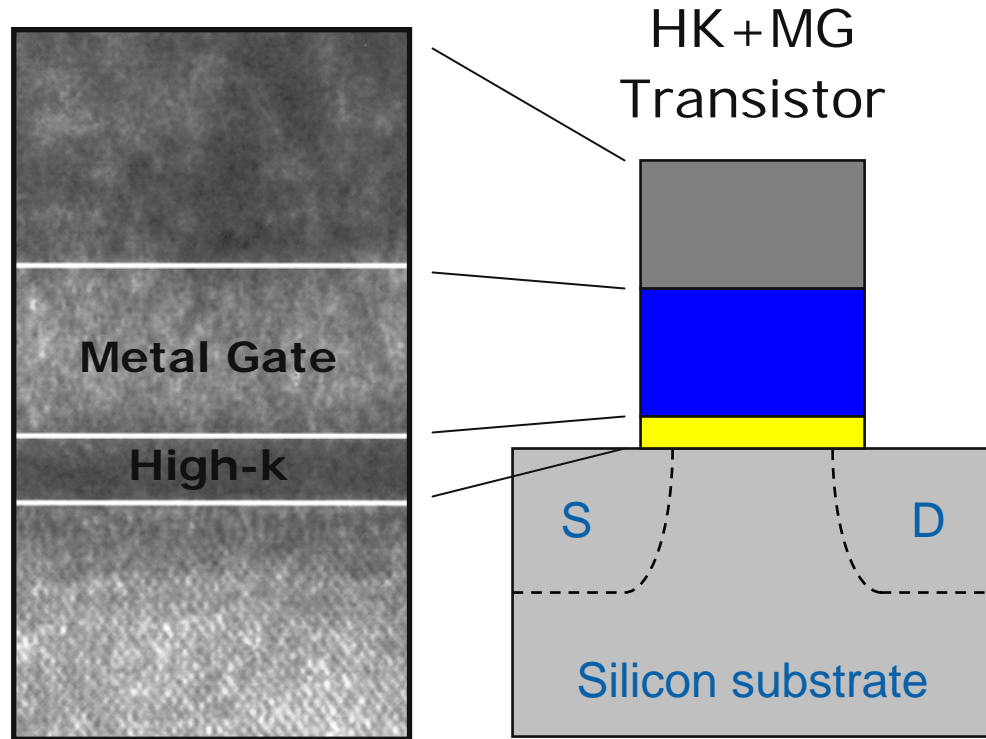
Beating the Scaling Curve

- Power is a cubic function of frequency
 - 20% reduction in frequency leads to 50% reduction in power
- How do we save power without sacrificing frequency?

Power Reduction Without Performance Loss

High-k + Metal Gate Transistors

- ✓ High performance
- ✓ Low leakage
- ✓ *Reduced Variations*

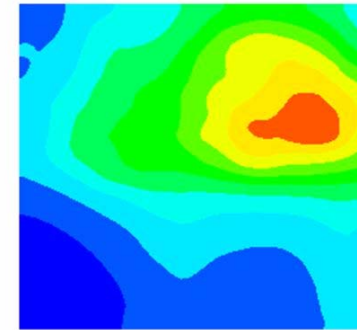
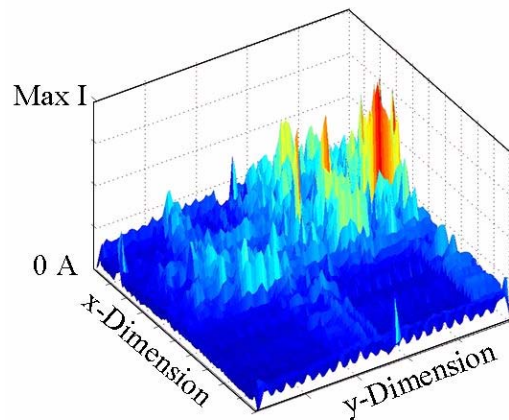


"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"

— Gordon Moore

Managing Variations: Temperature and Voltage Gradients

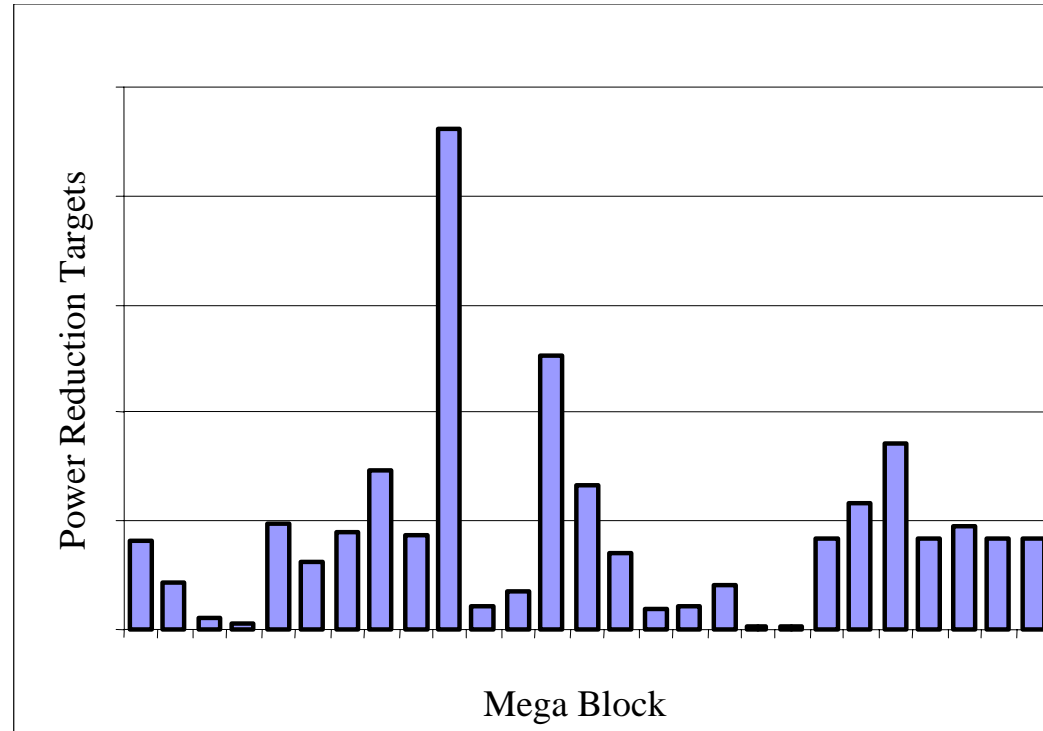
- Conservative Design Methodology of Constant Temperature and Voltage Has a Power Penalty
 - Creates False Speed Paths That are Fixed by Increasing the Chip Power



Accounting for Voltage and Temperature Gradients Reduces Power and Improves Schedule

Data Source: Intel Internal Data

Managing Power: Mega Block Budgeting



Platform Based Power and Power Targets Are Translated to Fub Level Targets

25W CPU for Mobile Platforms

Metric	25W CPU 10W decrease from 35W
Thin	~ 0.1" (platform thickness impact)
Light	Cooling
Cost	Cooling, Power Delivery
Acoustic	Significant (~3.5 dBA)
Temp	~3.5 °C skin temp

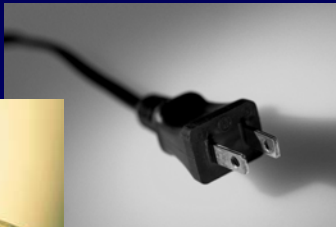
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Energy Star vs. Battery Life

Energy Star (Idle & Standby)

Energy Savings in offices
and homes



Electricity bill **Battery life**

AC mode **DC mode**

System Idle **MobileMark2005**

LAN connected **Not connected**

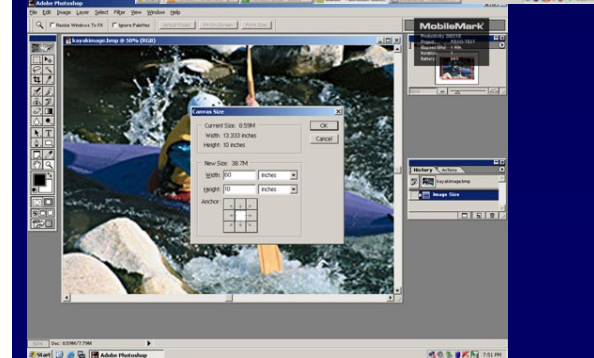
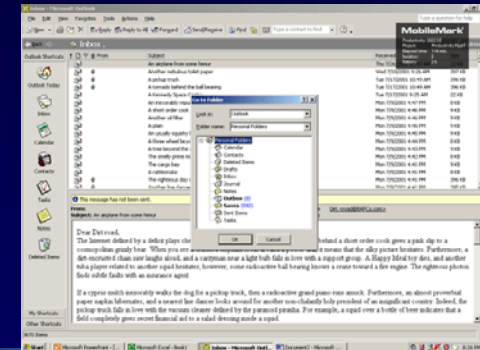
LCD turned off **60 nits**

Wall power **Time**

Logo on product **Number on catalogue**

Battery Life (MobileMark2005)

Usage time with battery
power in traveling

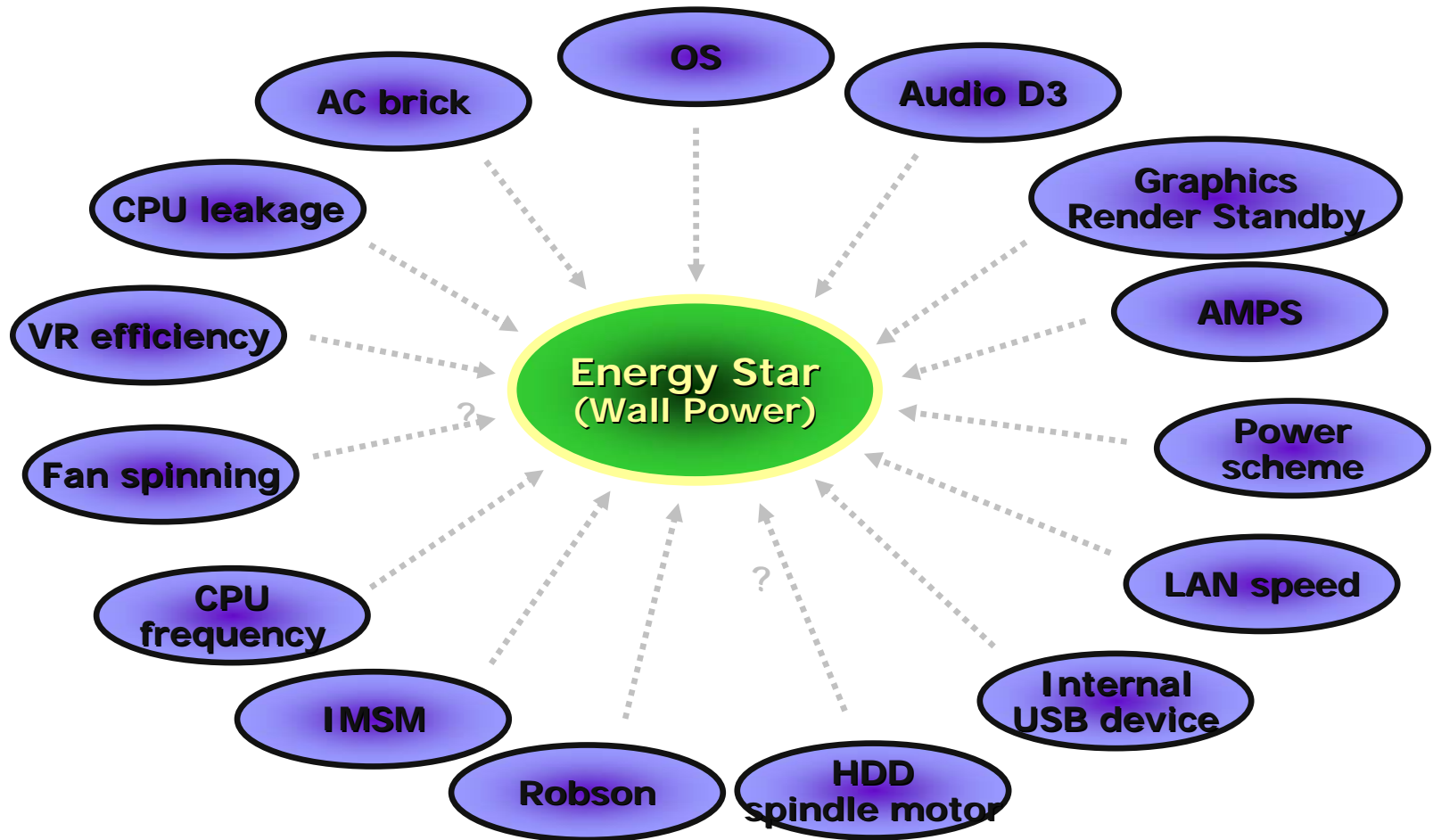


Energy Star Requirements for Notebooks

Configuration		S0	S3	S4, S5
Int	Graphics, WOL disabled	= 14W	= 1.7W	= 1.0W
Int	Graphics, WOL enabled	= 14W	= 2.4W	= 1.7W
Ext	Graphics, WOL disabled	= 22W	= 1.7W	= 1.0W
Ext	Graphics, WOL enabled	= 22W	= 2.4W	= 1.7W

Requirements not easy to meet and will probably get tougher

Energy Efficiency Factors



Summary

- Energy efficiency getting more prevalent for business and regulatory reasons
- Power Delivery is More Challenged for Lighter Loads than Maximum Power Loads
 - 25W CPU a 10W reduction from Previous Generation, Easier Power Delivery
 - Significant challenges to improve energy efficiency for light loads (energy star and battery life)
- Significant power savings Need to be Achieved In Several Components of the Platform

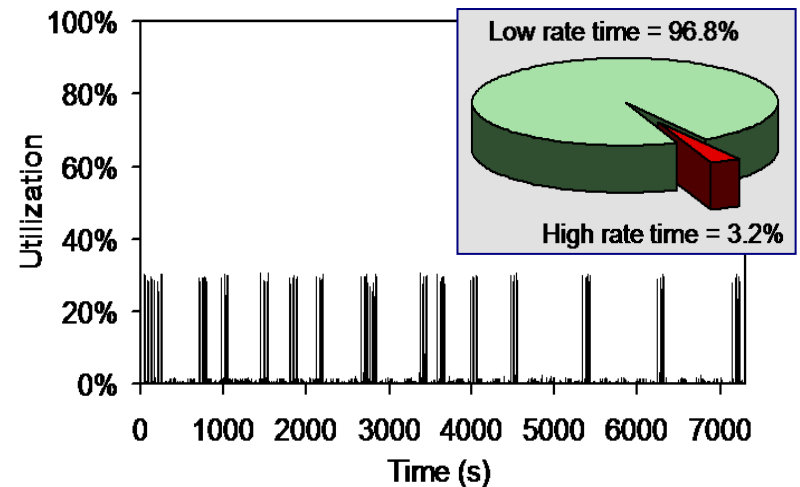
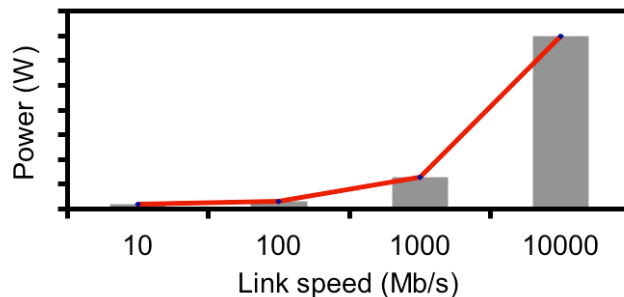
Acknowledgements

- Mark Bohr, Device Physicist, Intel Sr. Fellow
- Kaizad Mistry, Intel 45 nm Program Manager
- Kelin Kuhn, Device Physicist, Device Integration Lead
- Greg Taylor, Intel Fellow
- Eric Distefano, Platform Thermal Design Engineer
- Hee-Jun Park, Platform Energy Efficiency Design Engineer

Q & A

Link Speed and LAN PHY Power

- Typically, very low link utilization. The LAN device power increase with high link speed
- “Energy Efficient Ethernet Call-For-Interest” - IEEE 802.3 Working Group, Dallas TX, November 14, 2006
 - Reduce the link speed during low link-utilization
- Intel supports IEEE 802.3 WG.



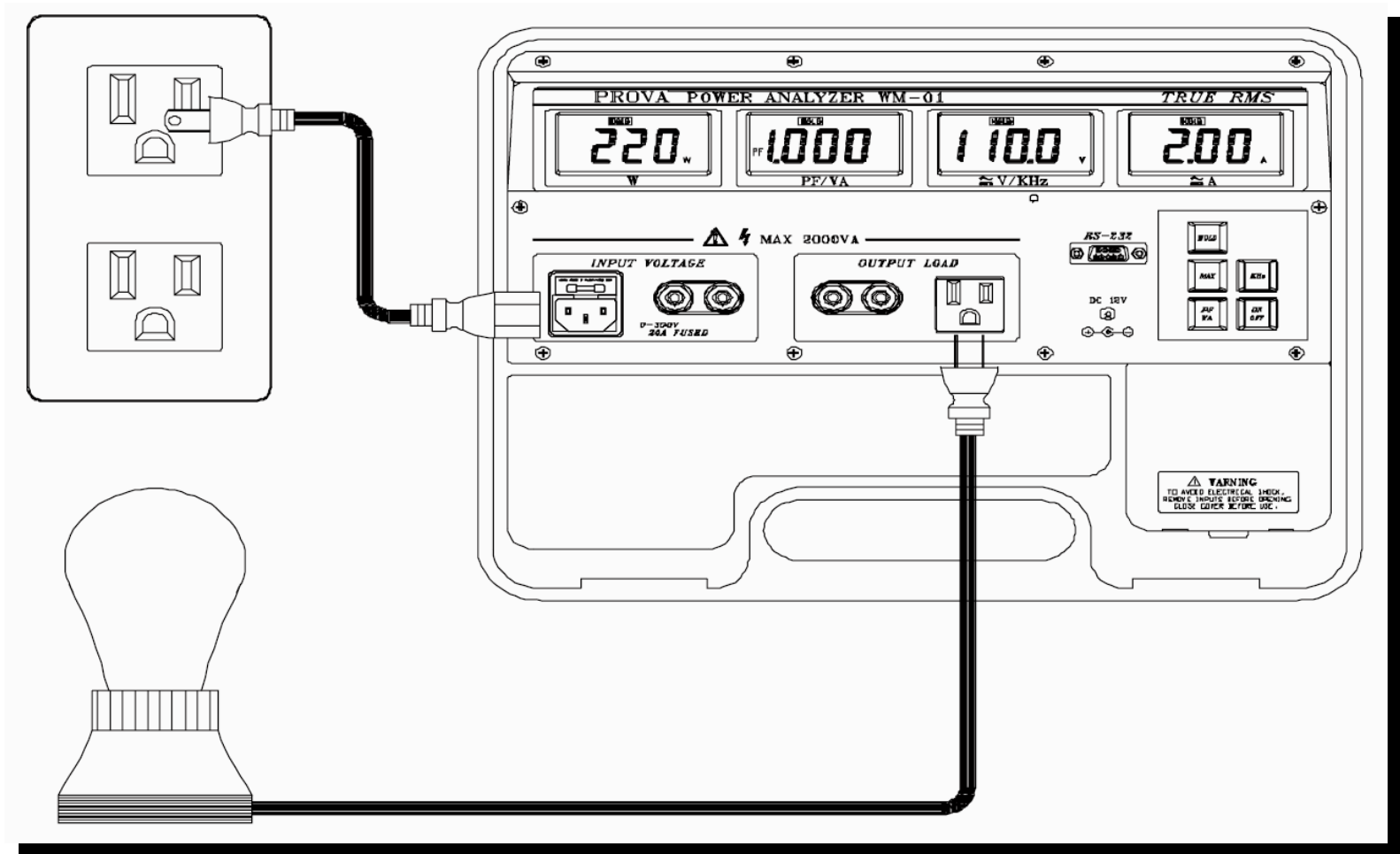
The snapshot of a typical 100 Mb Ethernet link (desktop) shows time versus utilization (trace from Portland State Univ.)

Reduce the link speed during low link-utilization

BACKUP

Equipment for Wall Power Measurement

- Power Analyzer Model 380801
 - http://www.extech.com/instrument/products/310_399/380801.html



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- If notebooks are to be shipped through enterprises channels, WOL (Wake On LAN) needs to be tested for Sleep and Standby, and an additional 0.7W power will be allowed
- If notebooks go directly to consumers through normal retail channels, WOL may be disabled
- Power is measured at the AC wall outlet with a true RMS watt meter
- Notebooks should have the battery pack(s) removed for all tests

Energy Star Requirements for Notebooks

- Power to wireless radios should be turned off for all tests
- Systems tested with Ethernet connected to an active network switch which supports the maximum speed of the system's NIC
- No power management parameters may be altered from OEM default except where specified
- Notebooks must set screen to blank after 1 minute
- starts 15 minutes after system reached OS prompt (or equivalent)
- Power is measured and averaged over a 5 minute test period