Design and Modeling of Through-Silicon Vias for 3D Integration

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Forschungsschwerpunkt
Technologien der Mikroperipherik

- Motivation
- Quantification of Some EMR Problems caused by TSVs
- Methods for Enhancing RF Performance of TSVs in Low Resistivity Silicon
- On-going Activities to Overcome TSV Design & Fabrication Challenges

- **Motivation**
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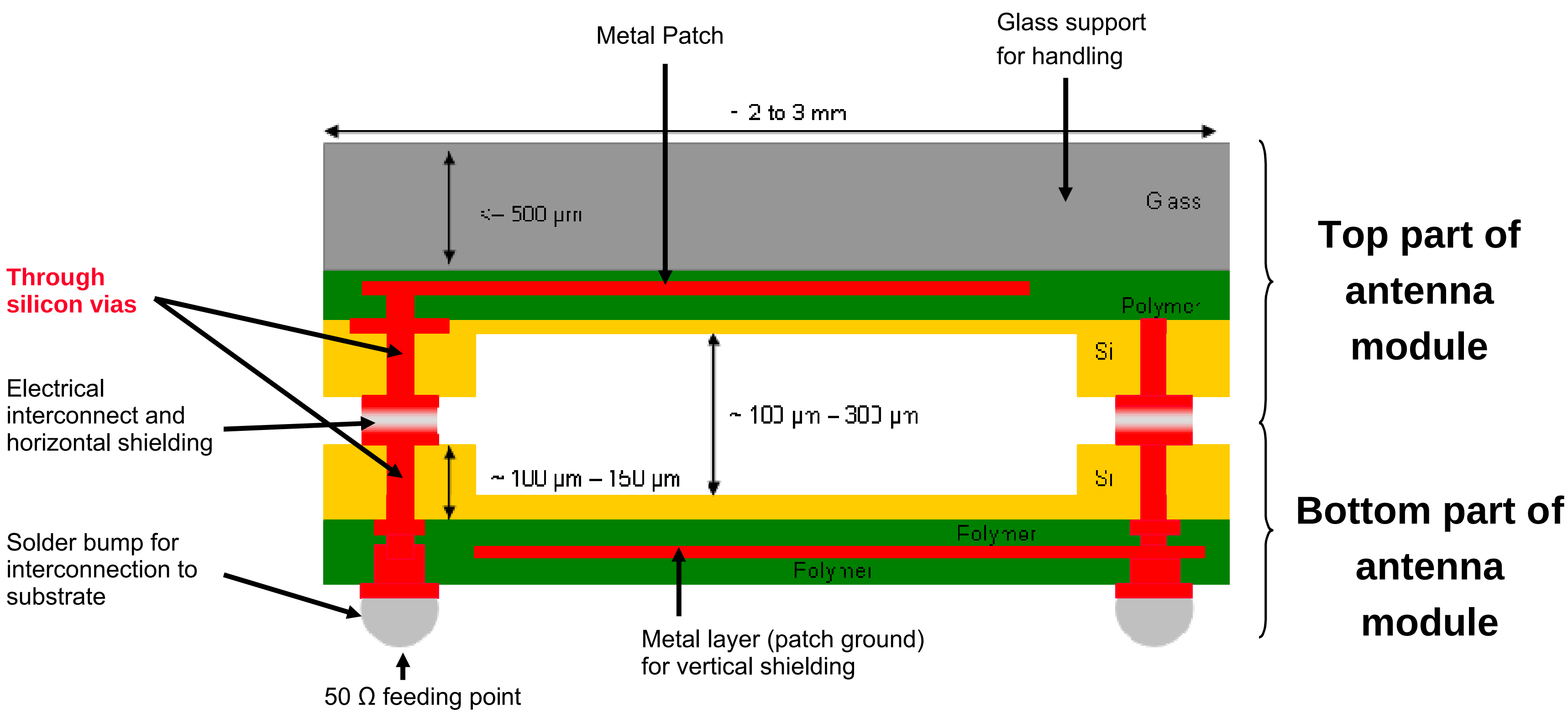
- To meet consumer demands for miniaturized, high-performance and low-cost products, 3D chip-stacked packages are needed.
- TSVs offer many advantages over conventional bonding techniques in facilitating 3D integration.
- A range of applications are emerging in which TSVs will be implemented to develop stacked and miniaturized electronic systems.

Example of Application: 60 GHz Antenna Module for WLAN Applications based on Wafer Level Packaging



Source: 3DASSM Consortium

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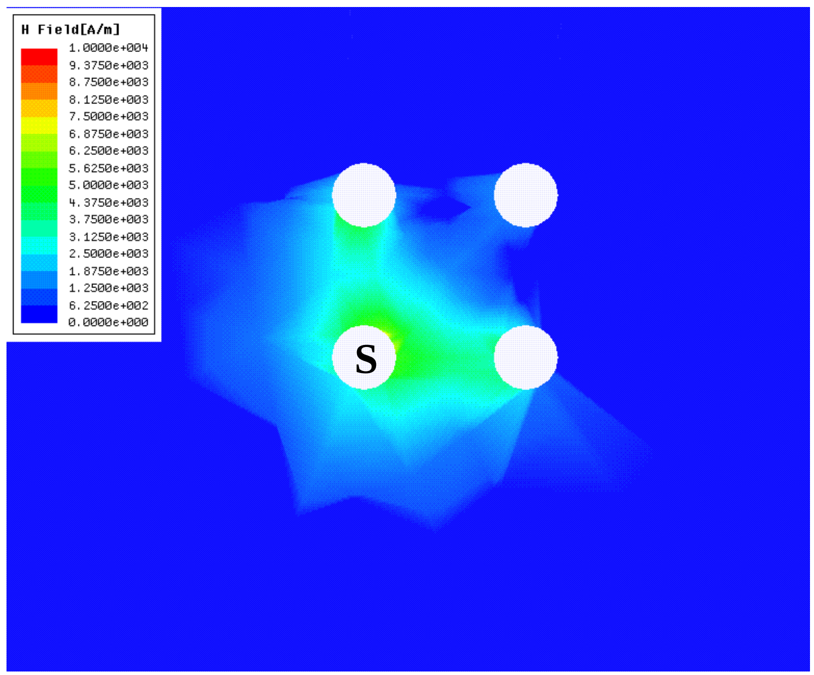
- **Electromagnetic Reliability (EMR) Problems due to Lossy Nature of Silicon**
  - **At microwave frequencies, lossy nature of Si leads to severe signal attenuation and other signal/power integrity issues as well as EMI problems.**

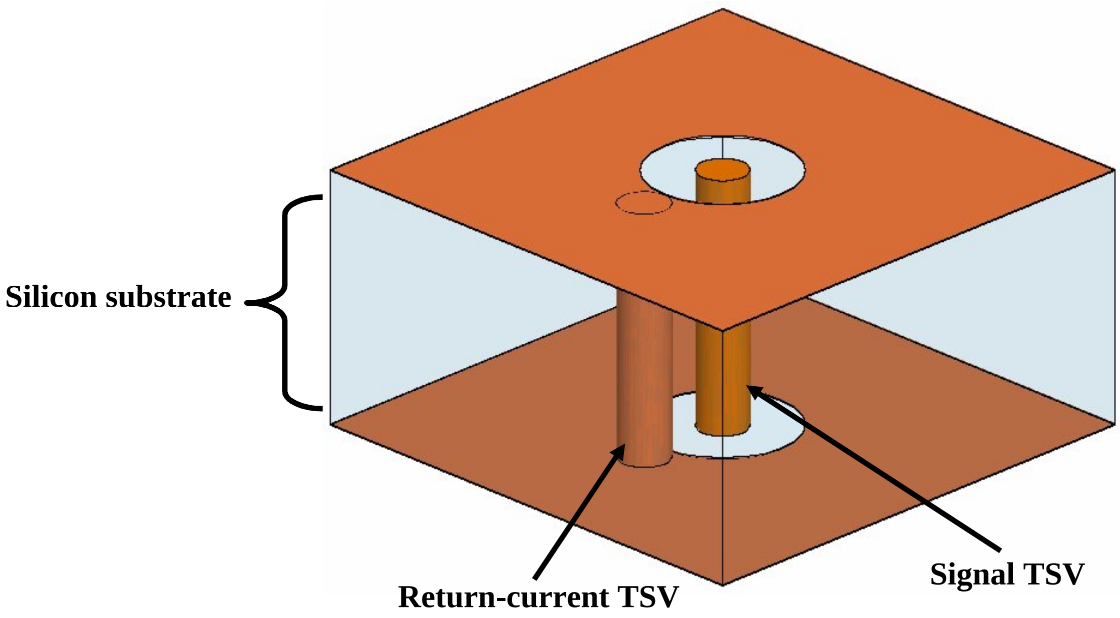


Si Conductivity from which Si Losses Dominate Conductor Losses – 1/4

Geometrical and Material Parameters Considered

- TSV diameter = separation distance between signal TSV and ground TSV = 40 µm; Er = 11.9, bulk conductivity = VARIABLE

Used Analytical Approximations and 3D full-wave Simulations

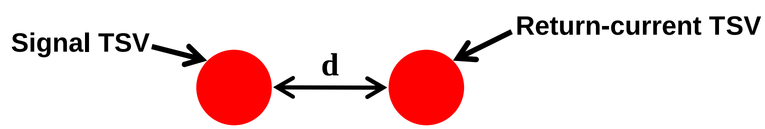


3D model of signal and return-current TSVs

Si Conductivity from which Si Losses Dominate Conductor Losses – 2/4

Using Analytical Approximations

- Signal & return-current TSVs can be approximated as 2 conductor TML



- Per-unit length parameters are given as

$$R' = \frac{R_s}{\pi a} \qquad L' = \frac{u}{\pi} \ln\left((d/2a) + \sqrt{(d/2a)^2 - 1} \right) \qquad G' = \frac{\pi \sigma}{\ln\left((d/2a) + \sqrt{(d/2a)^2 - 1} \right)}$$

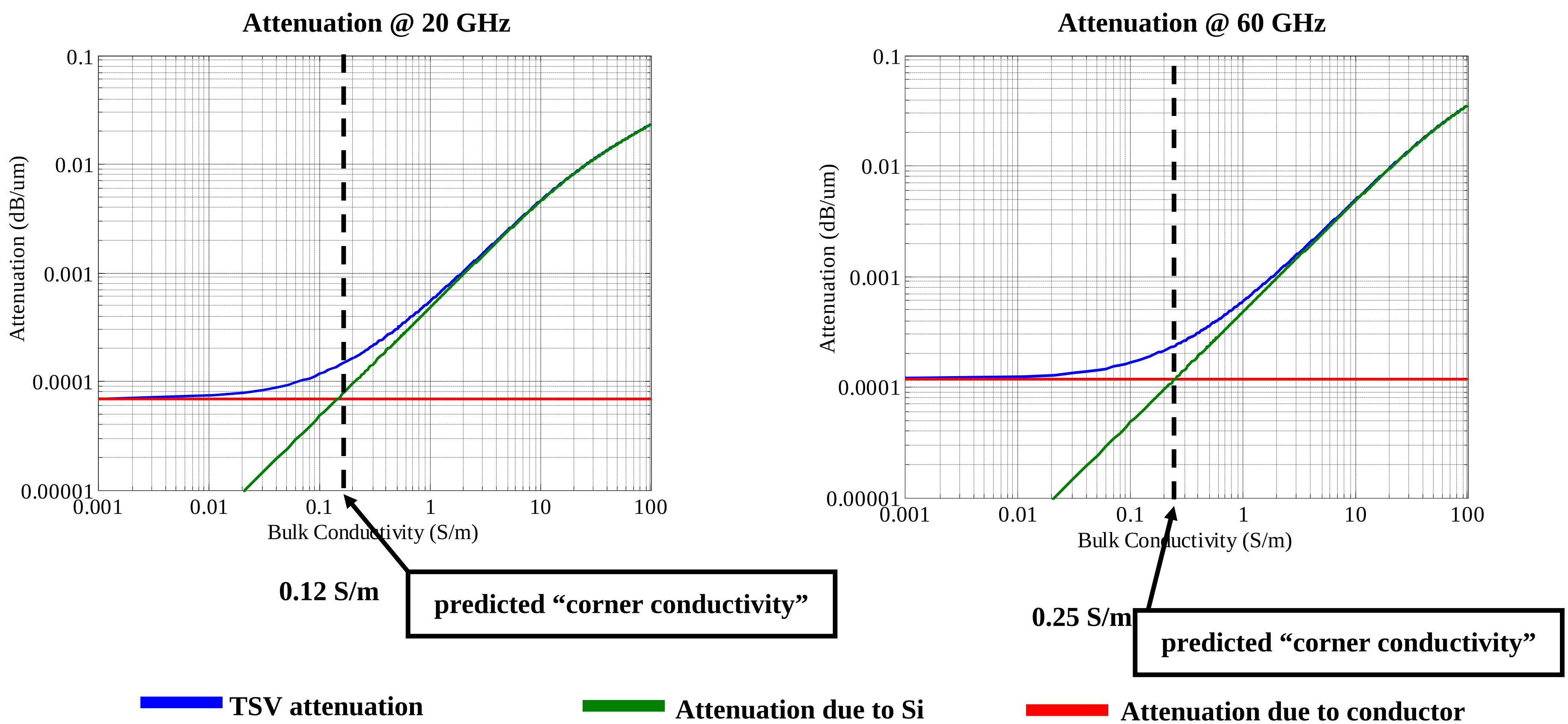
$$C' = \frac{\pi \varepsilon}{\ln\left((d/2a) + \sqrt{(d/2a)^2 - 1} \right)} \qquad \alpha = \sqrt{(R' + j\omega L')(G' + j\omega C')}$$

- By setting G=0 & neglecting losses due to radiation & proximity effect, signal attenuation due to conductor & dielectric may be approximately considered separately.

Si Conductivity from which Si Losses Dominate Conductor Losses – 3/4

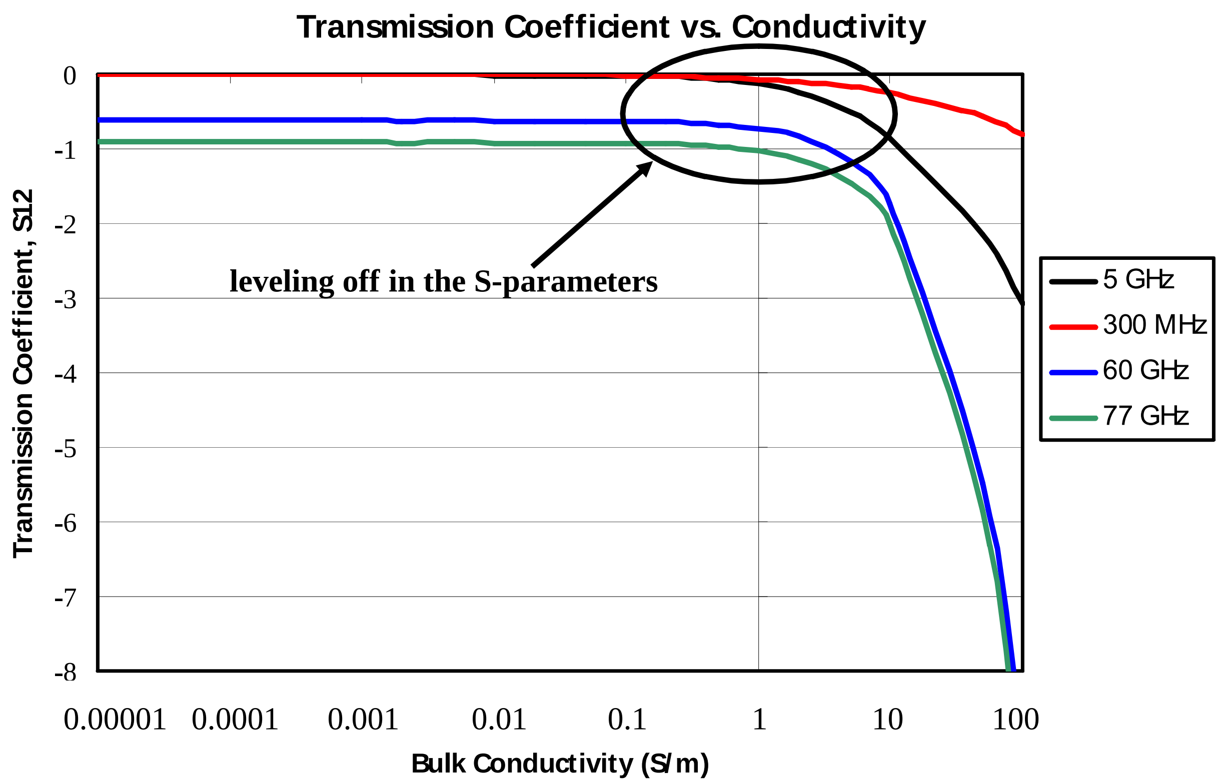
■ Using Analytical Approximations

- **Signal & return-current TSVs can be approximated as 2 conductor TML**



Si Conductivity from which Si Losses Dominate Conductor Losses – 4/4

Using Full-wave Simulations



- The Insertion loss obtained using full-wave simulations shows same effect as predicted with analytical approximations

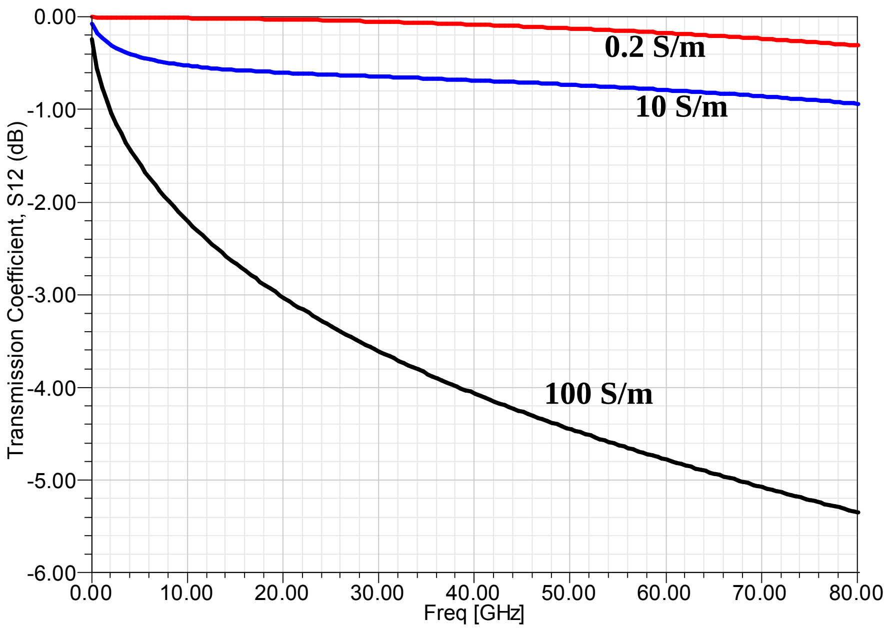
Impact of Resistivity on RF Performance of TSVs – 1/2

- **Intensity of EMR Problems caused by TSVs depends on Si Resistivity**
  - **Approximate range obtained from vendors**
    - Low Resistivity Silicon (LRS) = > 100 S/m, (< 1 Ohm cm)
    - Medium Resistivity Silicon (MRS) = 5 – 10 S/m, (10 – 20 Ohm cm)
    - High Resistivity Silicon (HRS) = < 5 S/m, (> 20 Ohm cm)
  - **LRS is far more cheaper than MRS & HRS**
  - **Values considered**
    - **LRS = 100 S/m**
    - **MRS = 10 S/m**
    - **HRS = 0.2 S/m**

Impact of Resistivity on RF Performance of Unshielded TSVs – 2/2

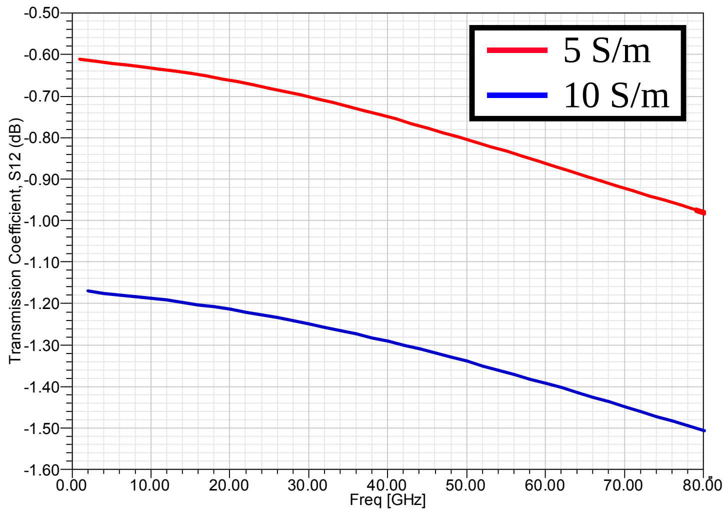
Geometrical Parameters Considered

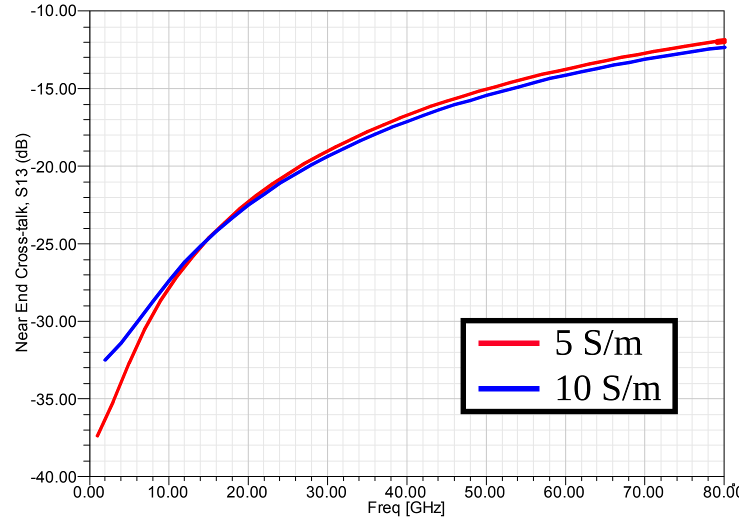
- TSV diameter = separation distance between signal TSV and ground TSV = 40 µm; TSV length =200 µm
- Insertion Loss considered as example



Challenge: To use LRS (which is far more cheaper than MRS & HRS, but extremely lossy) to design high performance silicon-based system modules

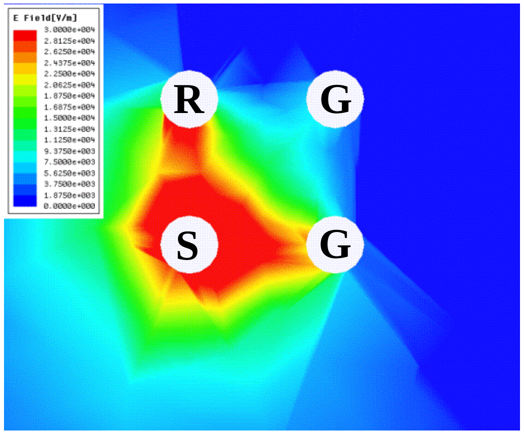
Cross-talk in TSVs





- Decrease in the conductivity of the silicon results in:
  - A nearly 50% decrease in the losses
  - <u>BUT</u>, nearly no change in the cross-talk

TSV Cross-talk continues to be a problem, even when losses are manageable.



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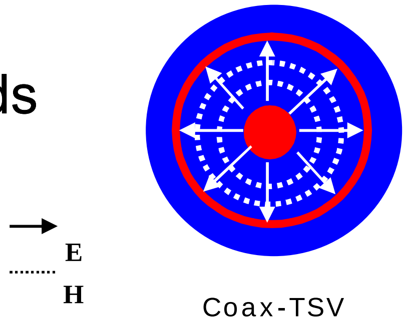
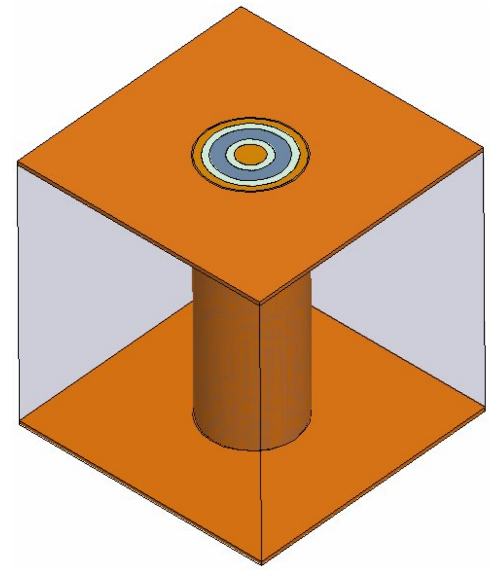
Concept of Coax-TSVs

$$P_t = \frac{1}{2}\oint_s S.ds$$

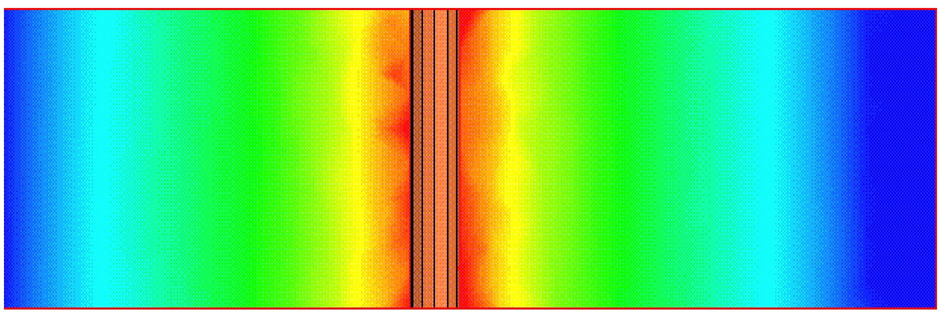
$$S = E \times H^*$$



Coax-TSV



3D model of Coax TSV



H-field intensity in Si around Coax-TSV from

10MHz to 1 GHz

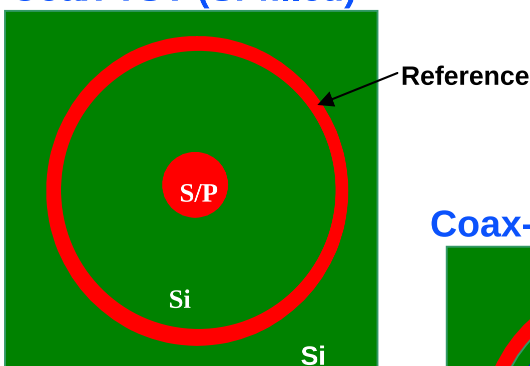
Enhancing RF Performance of TSV in Low Resistivity Silicon – 2/4

- **Coax-TSV (Si-filled) Vs Coax-TSV (Mixed-filled)**

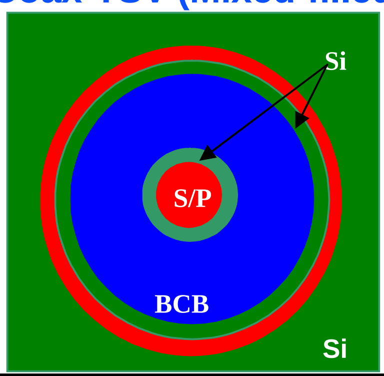
  - **Coax-TSV (Si-filled): If Si is used as dielectric, there will be no improvement in RF performance**

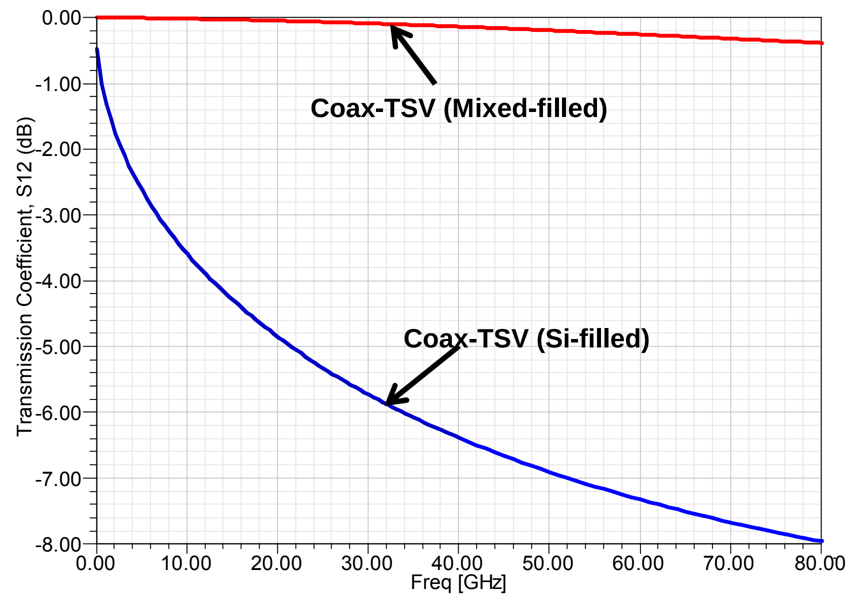
  - **Coax-TSV (Mixed-filled): RF Performance is greatly enhanced if Si is partly replaced by low-loss dielectric e.g., BCB**

Coax-TSV (Si-filled)



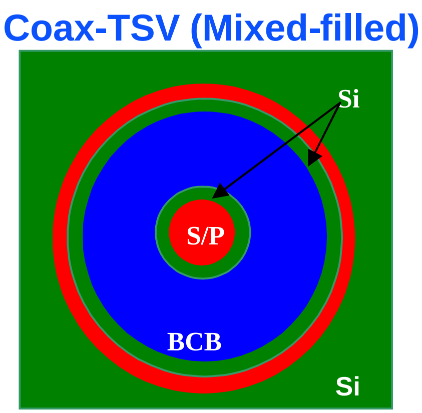
Coax-TSV (Mixed-filled)

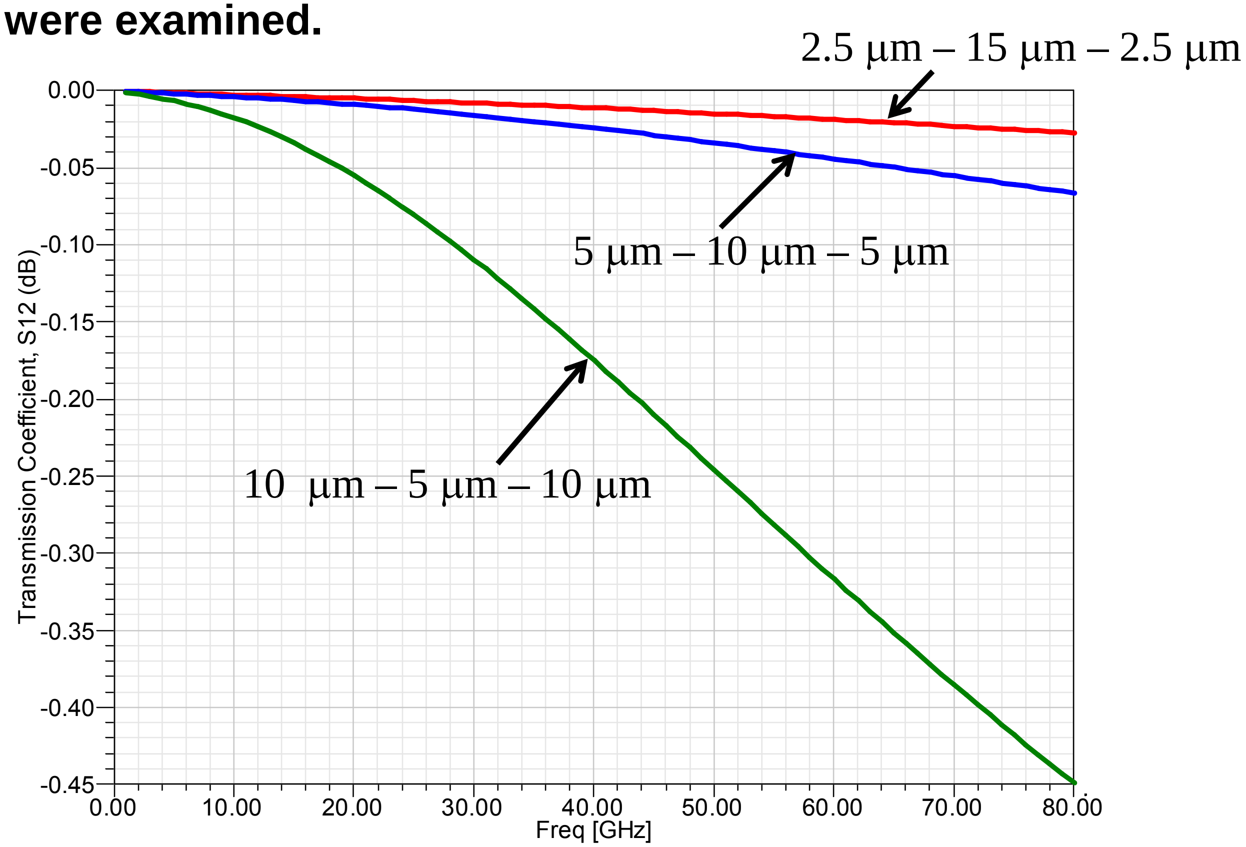




Enhancing RF Performance of TSV in Low Resistivity Silicon – 3/4

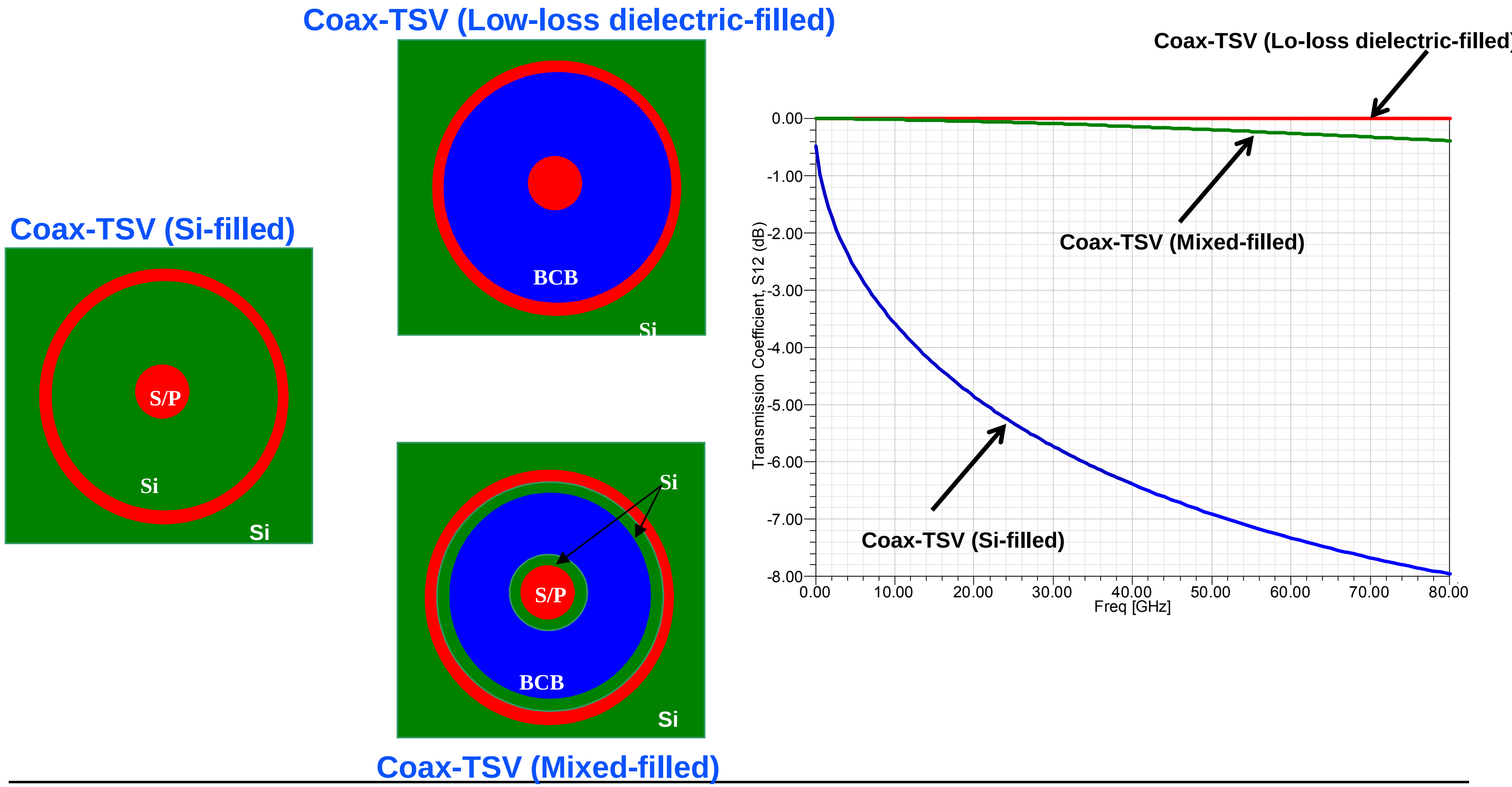
- **Coax-TSV (Mixed-filled)**
  - **Enhancement of RF performance depends on ratio of Silicon to BCB**
  - **3 different ratios were examined.**





Enhancing RF Performance of TSV in Low Resistivity Silicon – 4/4

- Coax-TSV (Low-loss dielectric-filled)



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Consortium on 3D All Silicon System Module (3DASSM)

Goal of 3D ASSM

- Miniaturization of the entire electronic system using Si for ICs, packages, and boards. This approach is expected to result in high system performance at low cost and high reliability.

Academic Partners

- Georgia Tech (USA)
- KAIST (Korea)
- Fraunhofer IZM (Germany)

Proposing 20+ Projects & 3 Test Vehicles

Thrusts

- Electrical Design & Test
- Silicon Substrate with Multilayer Wiring
- Low-cost TSV & Stack Bonding
- Embedded Thin Film Actives & Passives
- System Interconnects

More Information: http://www.prc.gatech.edu/events/3dassm/index.htm

Consortium on 3D All Silicon System Module (3DASSM)

Electrical Design & Test Thrust

■**Objectives:** **Explore and develop design methodologies to enable ultra-miniaturization and low cost hetero-integration addressing the challenges with the electrical properties of silicon.**

Project	Previous Approach	Proposed Approach
Project A-1: Design of Interposer with Zero SSN	Minimize Noise using decaps and planes	Eliminate noise with power trans. lines and TSV
Project A-2: Design of Stack Bond with Vertical Shielding	Non-coaxial TSV CPW	Coaxial TSV SWLS Magnetic Film
Project A-3: Hybrid Equalization for over 10Gbps High Speed Channel	Either active or passive	Active and passive

Fraunhofer IZM · Georgia Tech Microsystems Packaging Research Center · KAIST

Thank you very much

for your attention!