Design Considerations for Highly Integrated 3D SiP for Mobile Applications

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Contents

Ubiquitous Mobile Life

Physical World

Mobile Platform

Player

Brain

Product

Robot

Auto-mobile

Wired

Wireless

Computing

Communication

Sensing/Cognition/Identification

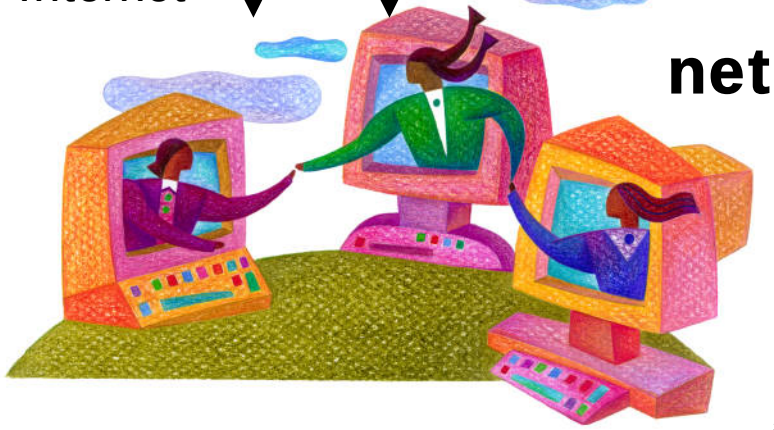
Entertainment

Medical/Welfare service

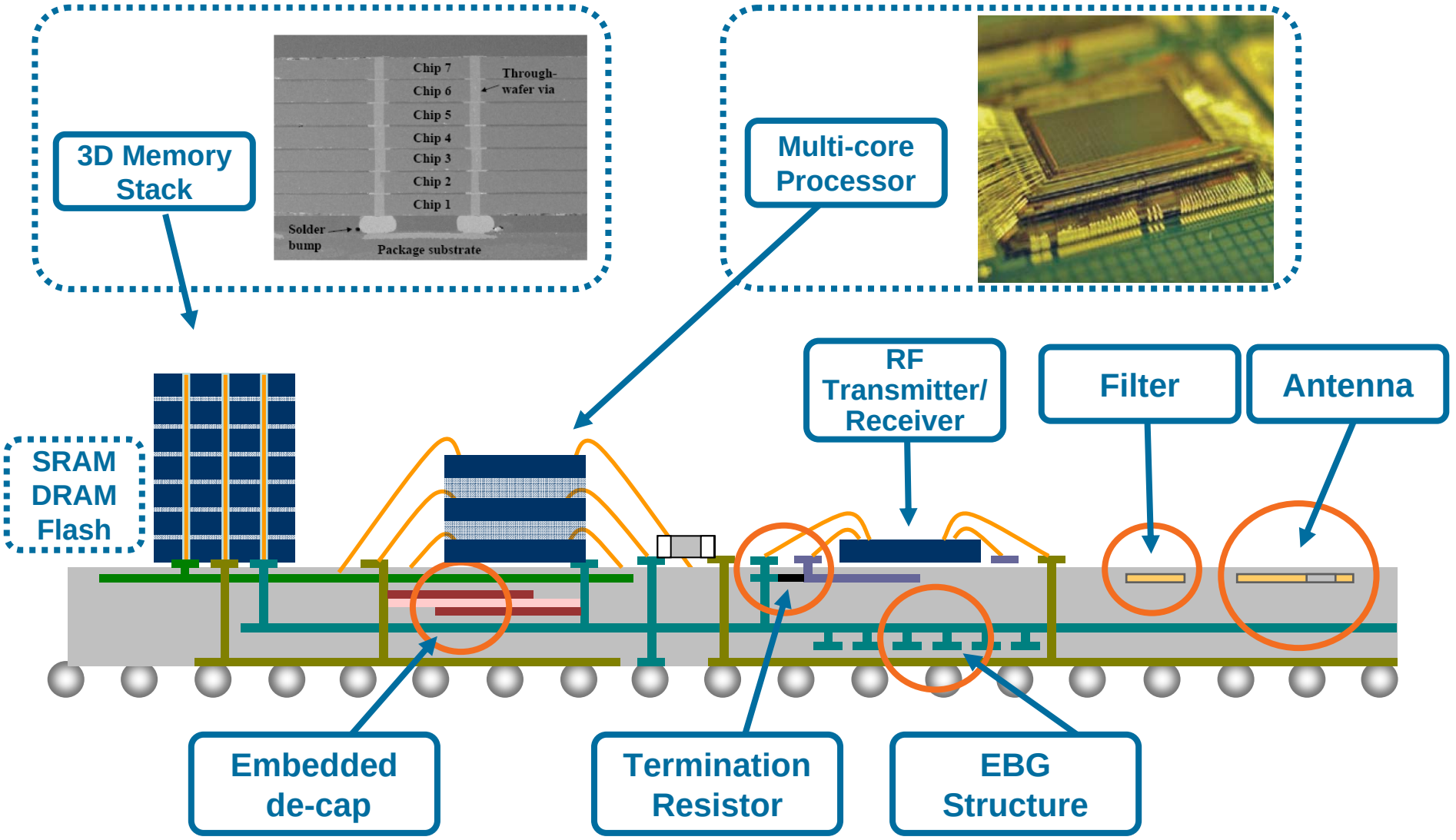
Internet

Telephony

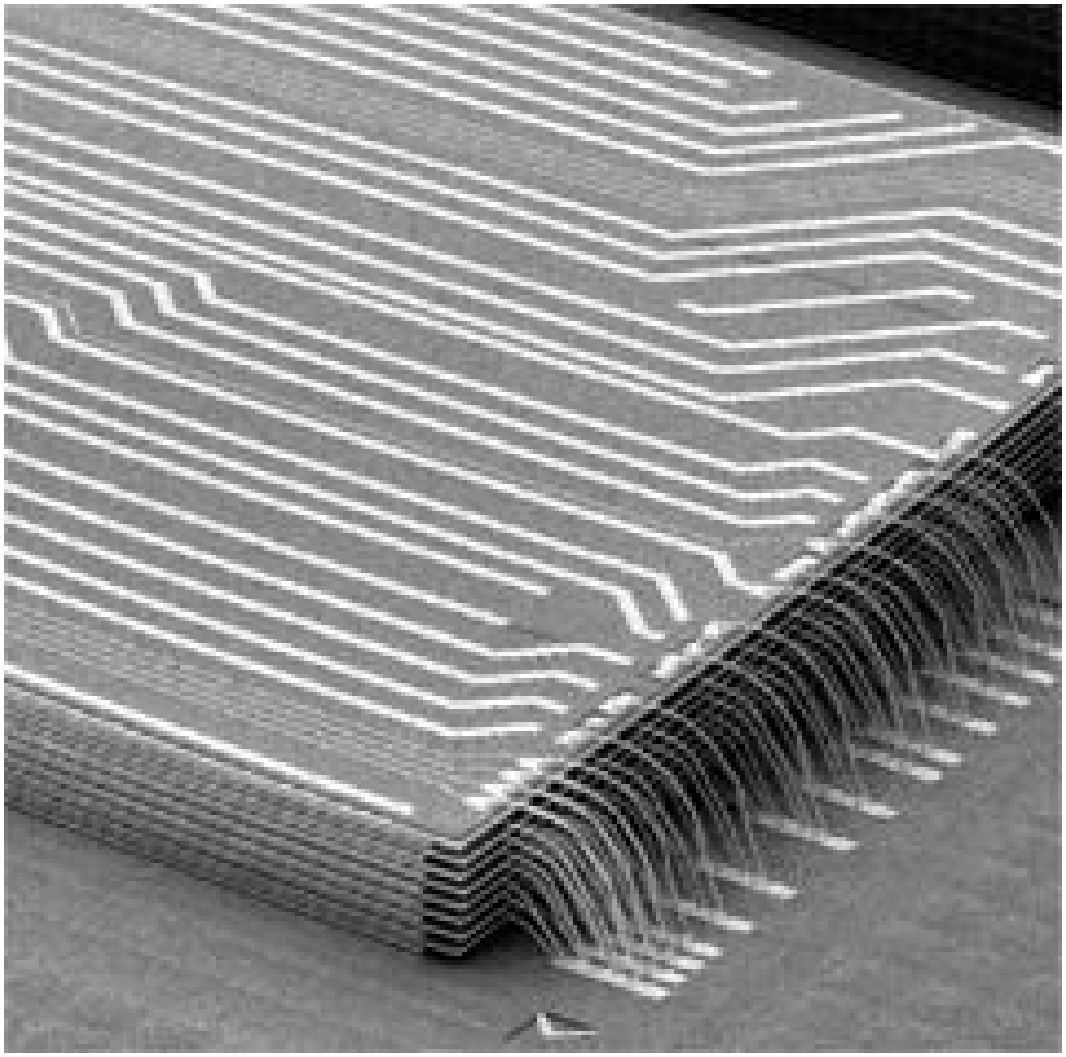
network



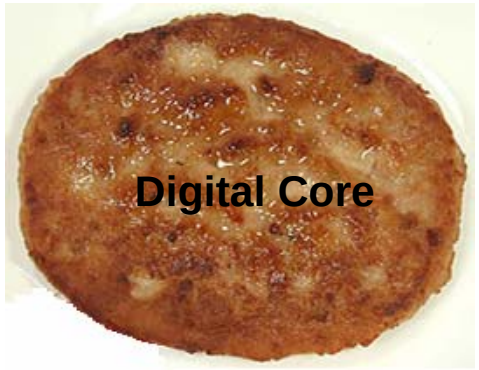
3D System In Package



16GB Samsung NAND Flash, 8Gbx16



3D Hamburger

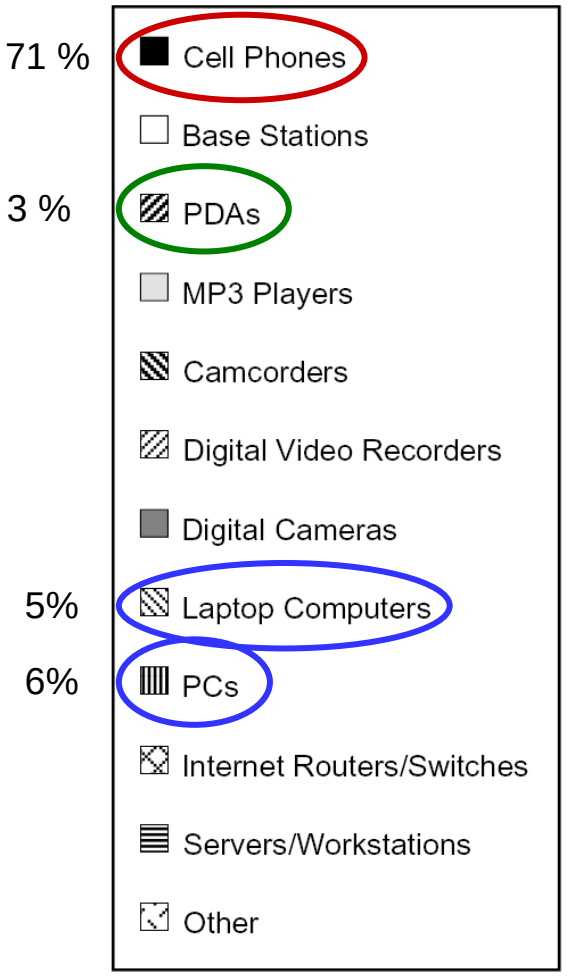


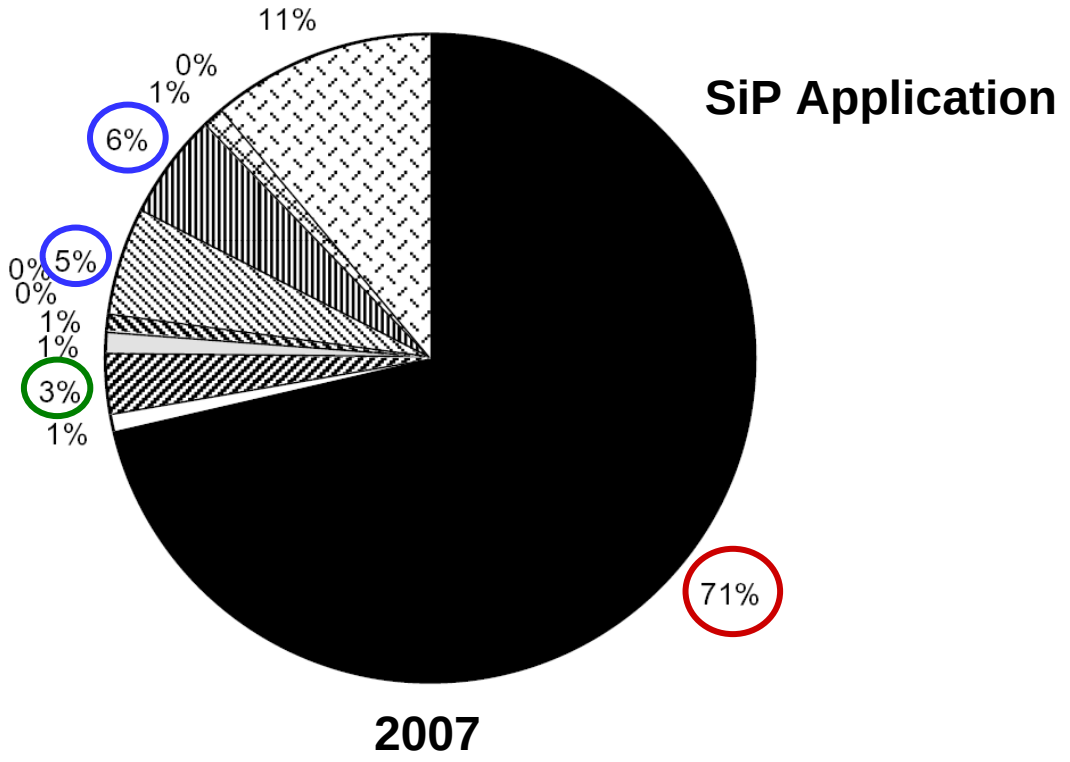
Advantages of 3D SiP approach

- Small form factor
- Fast time to market
- Inhomogeneous device integration
- Integration of passive devices, filters, and antenna
- Suitable for RF mobile communication systems
- Low cost

Applications for SiP

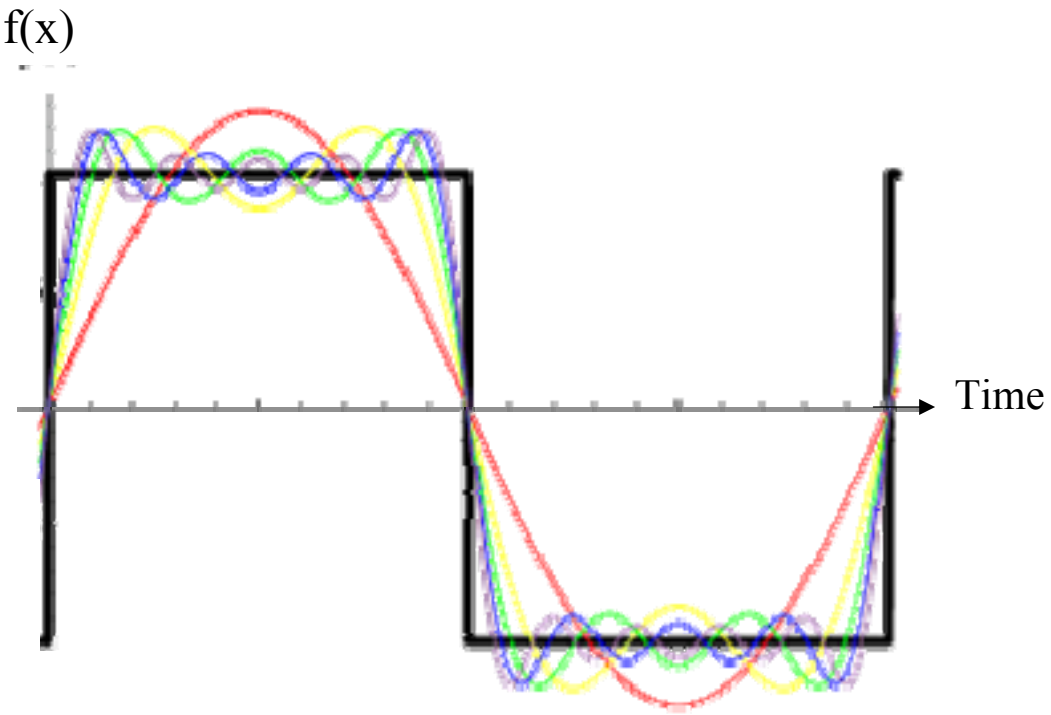
Concentrate on Multi-Function Light Weight Device Application
- Short Product Life Cycle (PLC)



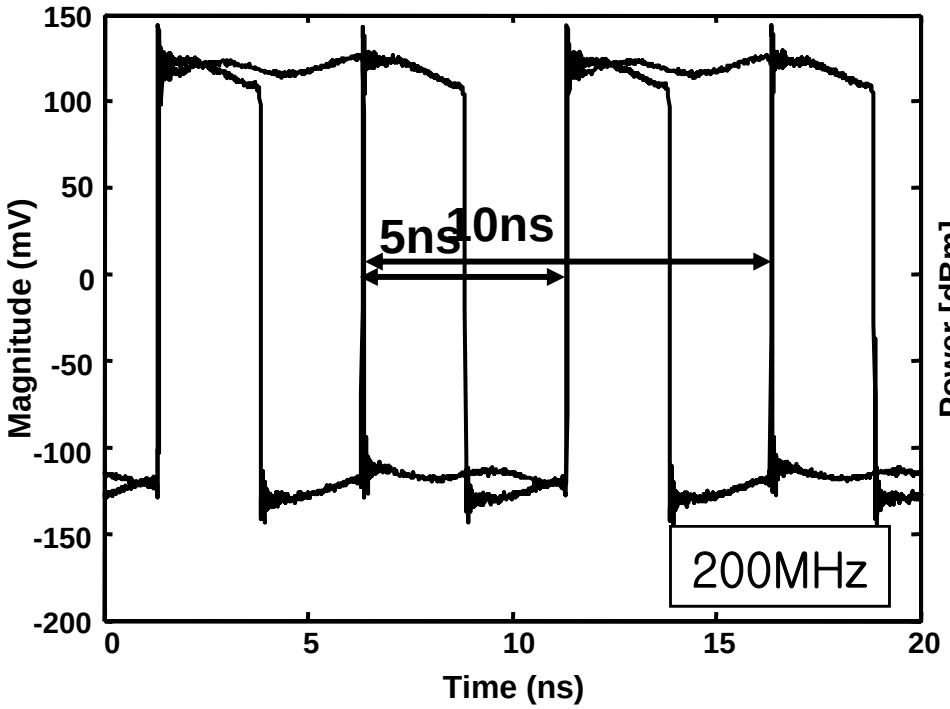


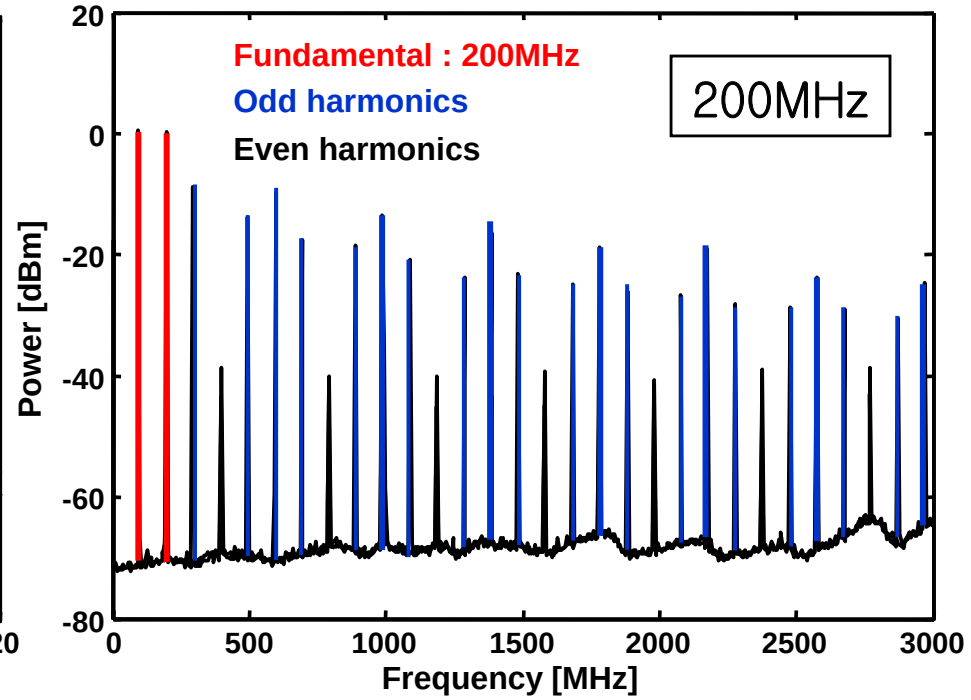
Source: Advanced IC Packaging (2007 Edition)

Frequency Spectrum of Digital Clock Waveforms

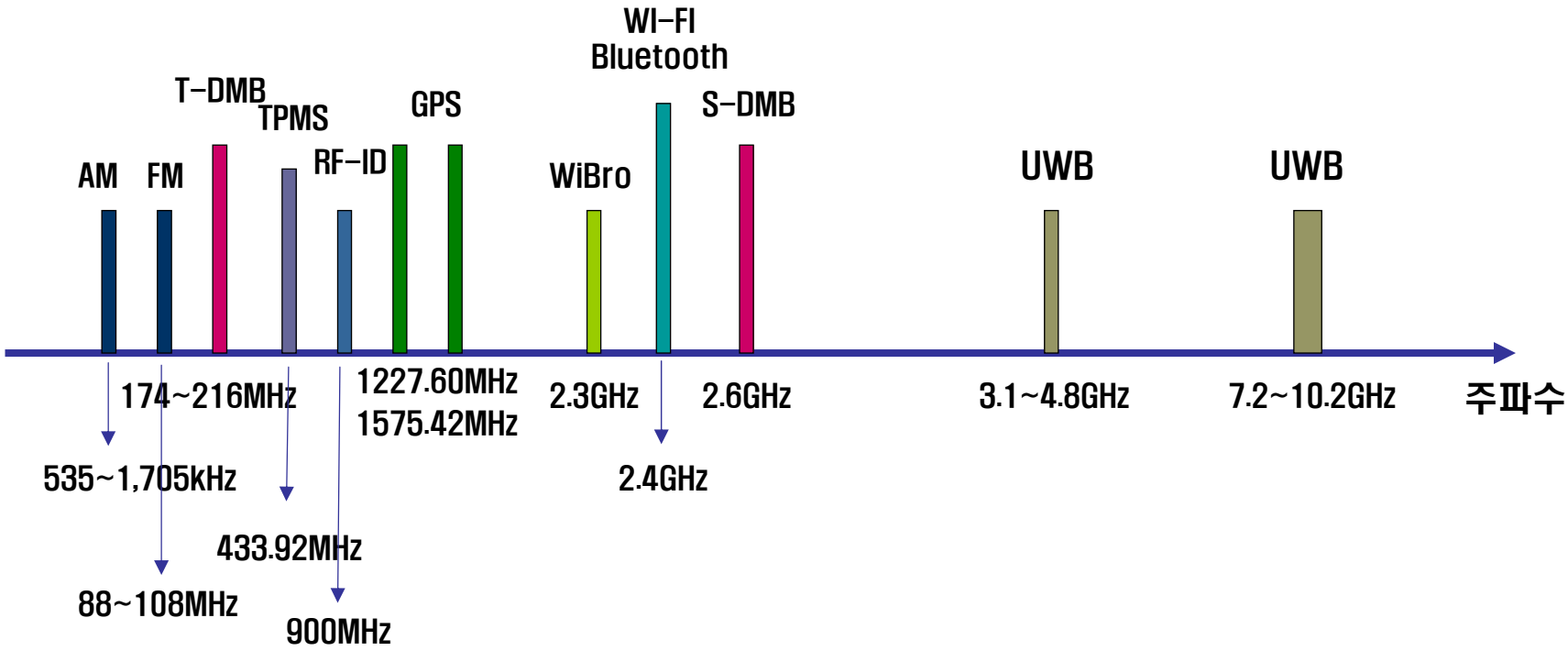


Waveform and Spectrum of Clock Signal





Spectrum of Wireless Mobile Communication Systems



Noise coupling path from digital circuits and RF circuits

- Noise coupling Paths:

- ❑ Wire, Traces, slot, and Balls
- ❑ Via transitions
- ❑ Return current path discontinuities
- ❑ Power and ground pane cavities

- Results:

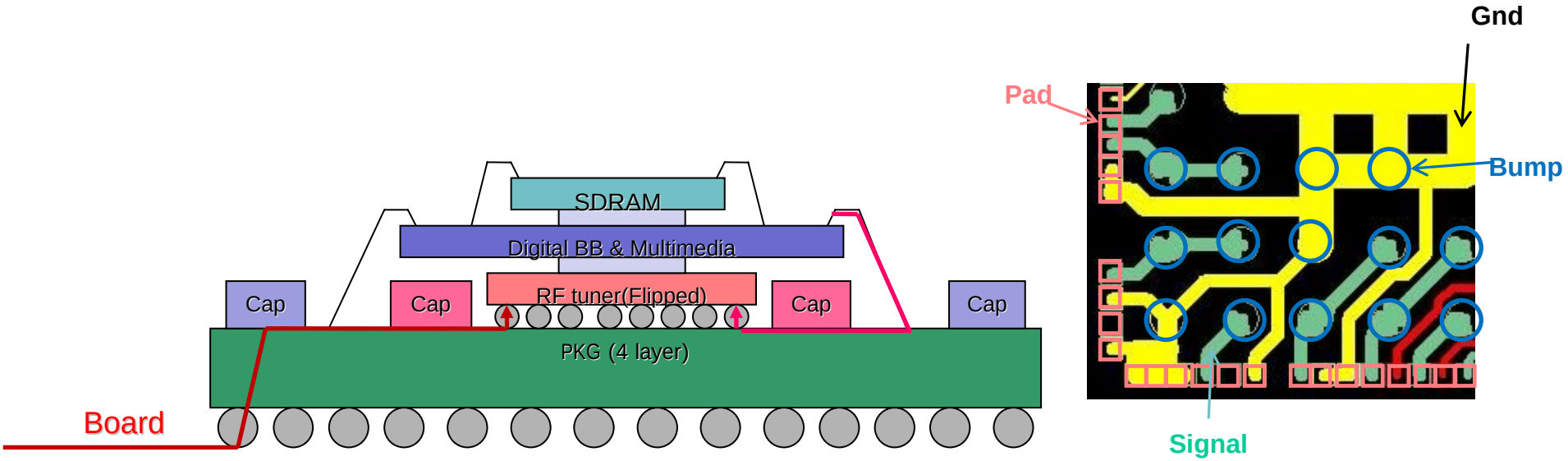
- ❑ Timing and voltage margin violation at receiver
- ❑ Degradation of receiver sensitivity and BER

Signal Integrity Concerns at SiP design

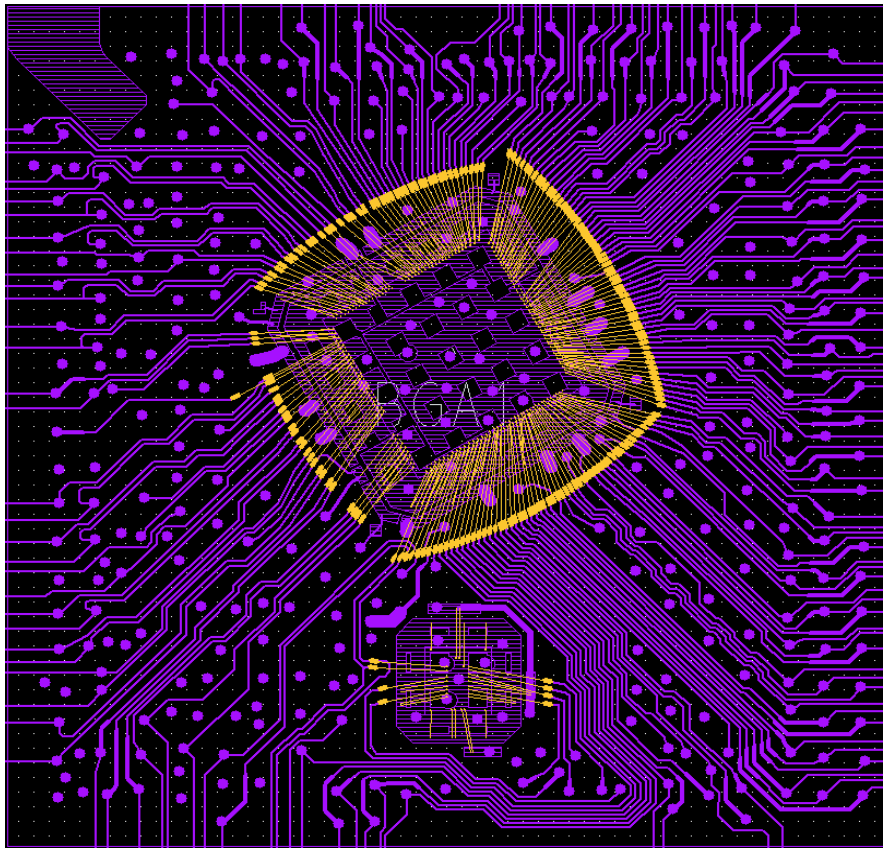
- Reflections and resonances by impedance mismatches: source end termination, line impedance, and receiver end termination
- Reflections and resonances by impedance discontinuities: via, pad, wire, connectors, cables.
- Reflections and resonances by return current path discontinuities
- Common return current path and non-zero return current path impedance
- Channel loss by skin effect loss and dielectric loss

Impedance discontinuities at package

- wire, pad, via, trace, ball
- Channel of chip-to-chip link : A package is becoming a major bandwidth restraint.

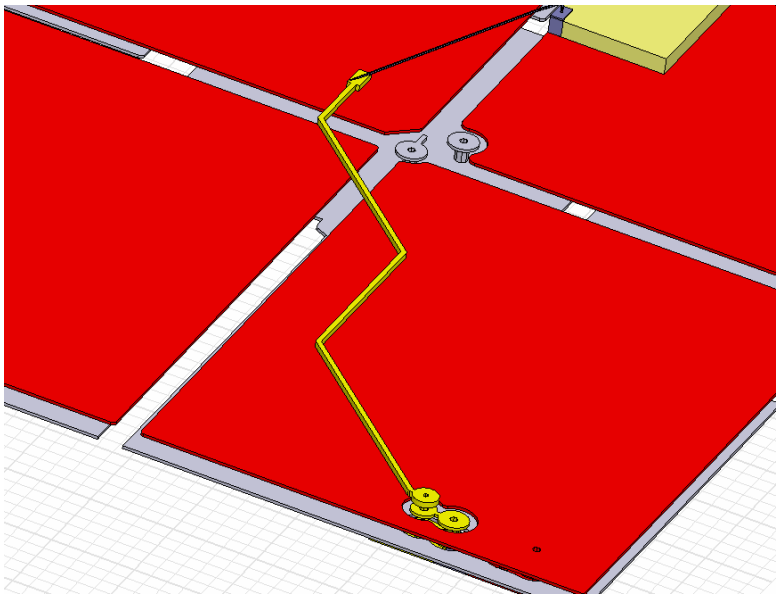


Transmission Lines on SiP

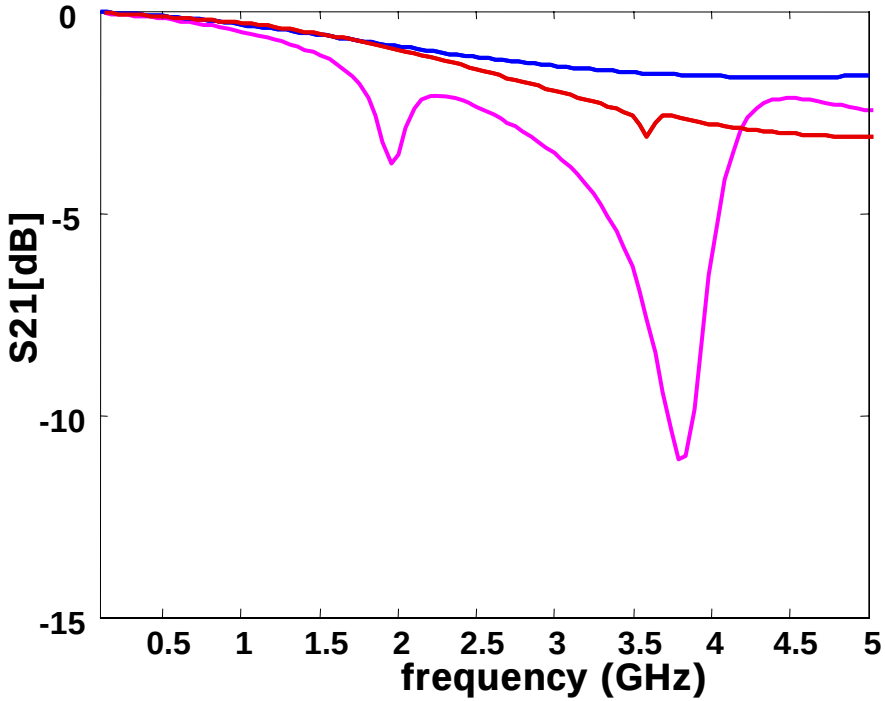


- **Package Type : PBGA**
- **No. of Layers : 4**
- **Package Size : 23 x 23mm**
- **Ball Array**
  - 22x22 Ball Array, 384 Balls
- **Power/Ground Plane Split**
  - 5 Ground / 7 Power
- **Die Size**
  - 5 x 5mm, 1.6 x 1.8mm
- **Line Width : 60um**
- **Ball pitch, size : 1mm,0.6mm**
- **Via : 300um, Drill : 150um**
- **Finger length : 300um**
- **Finger pitch : 140~150um**
- **Finger spacing : 25um**
- **A1 placement : no routing**

Insertion Loss of 900MHz Single Line



900MHz	
Case	**S21(dB)**
No split / no ref change	**-0.29**
No split /ref change	**-0.29**
Split / no ref change	**-0.34**

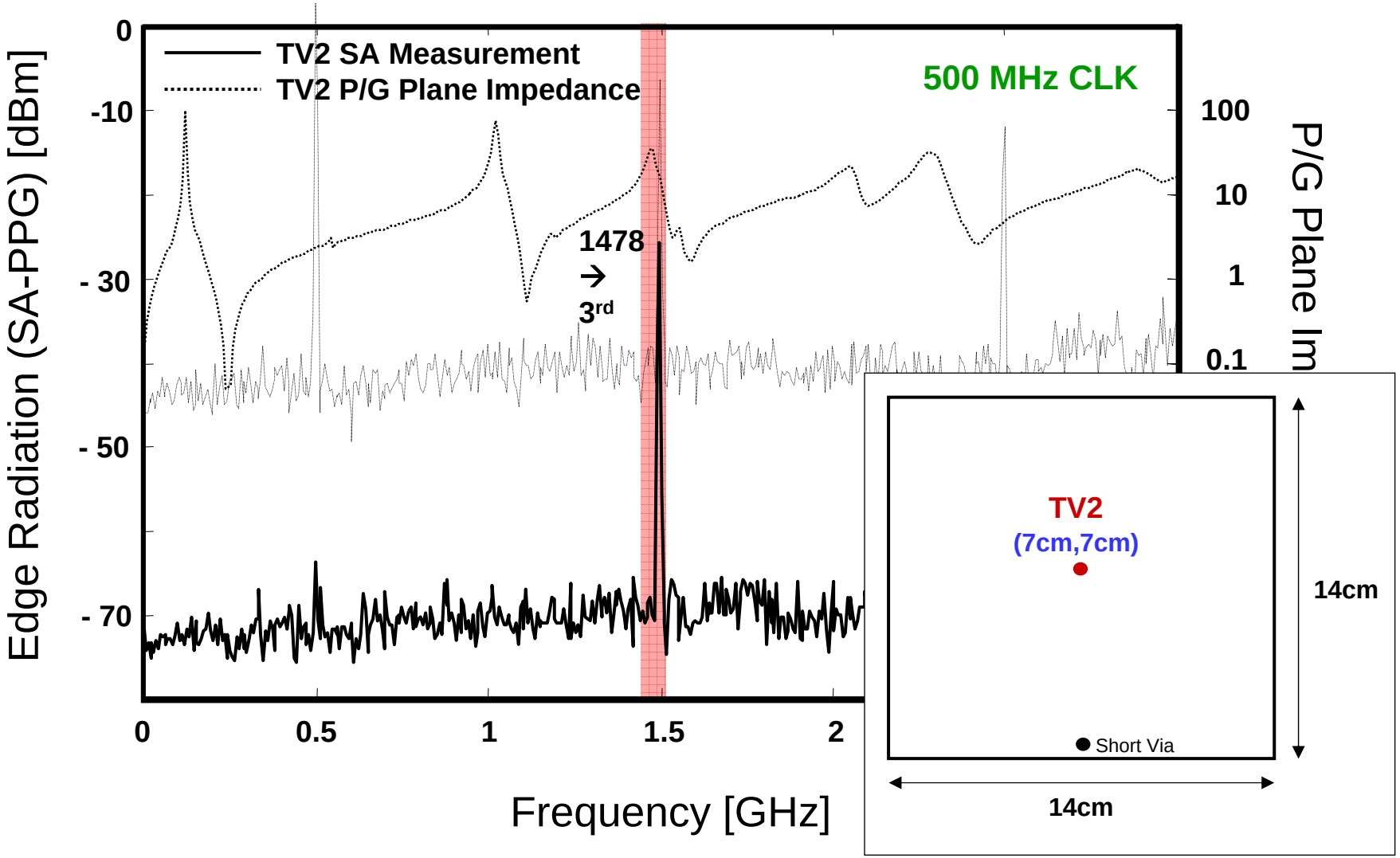


No split & no reference change

No split & reference change

Split & no reference change

Spectrum Analyzer Measurement of P/G Plane Edge Radiation from TV2 (Center Via) with 500MHz Clock Excitation



Resonances in SiP Substrate

- Multiple reflections
- Power/Ground plane cavity
- Interactions between via inductance, wire inductance, and ESL of decoupling capacitors with off-chip decoupling capacitors, on-chip decoupling capacitors, and power/ground plane capacitance
- Slots

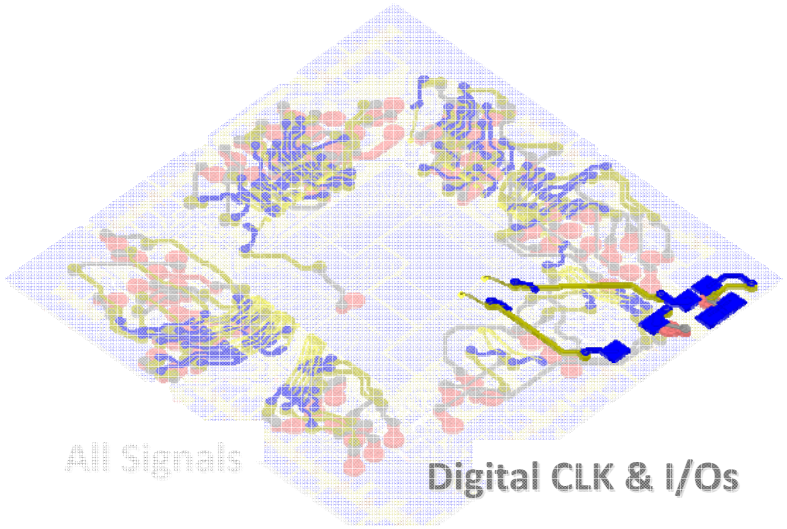
Digital noise isolation in SiP

- Balancing
- Secure return current
- Filtering
- Shielding
- Separations

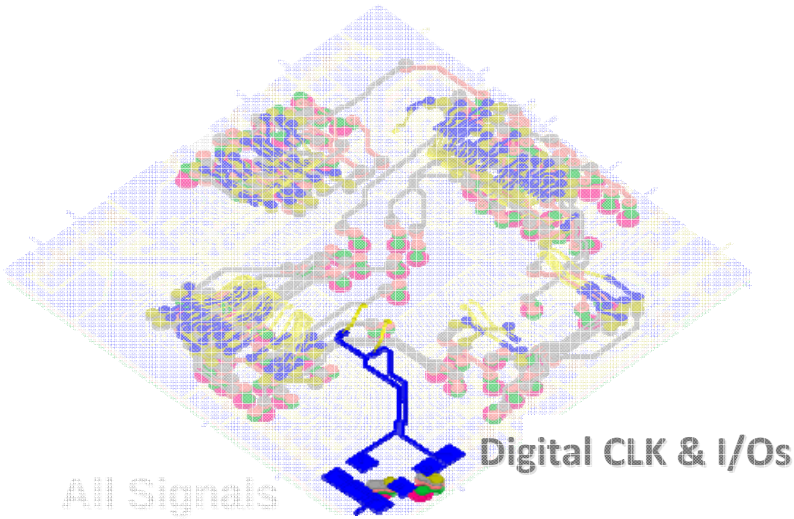
Separation Between Digital Signals and RF Signals

- A digital clock or digital I/O can be an aggressor signal to an RF signal, while an RF signal can be a victim.

- Digital clocks or I/Os should be spatially separated from RF signals.

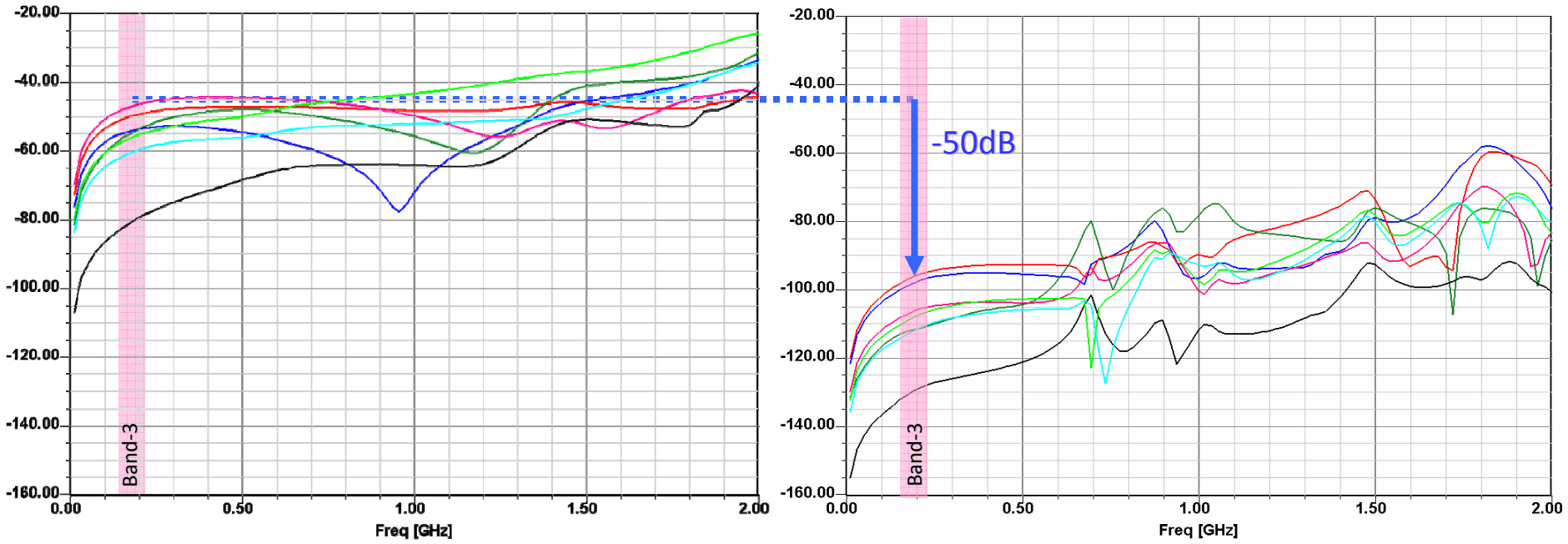


Sensitive RF Signals

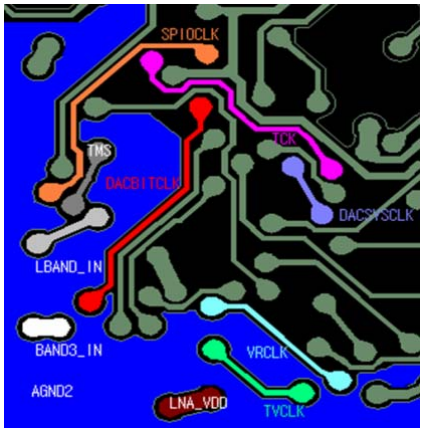


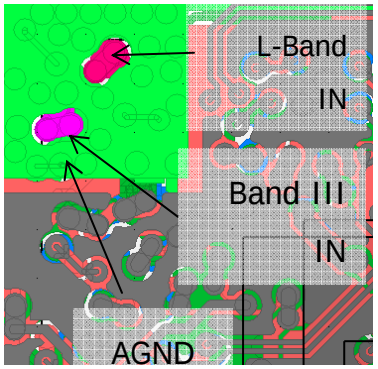
Sensitive RF Signals

Coupling Between Signal Line & Digital Clocks : T-DMB Case



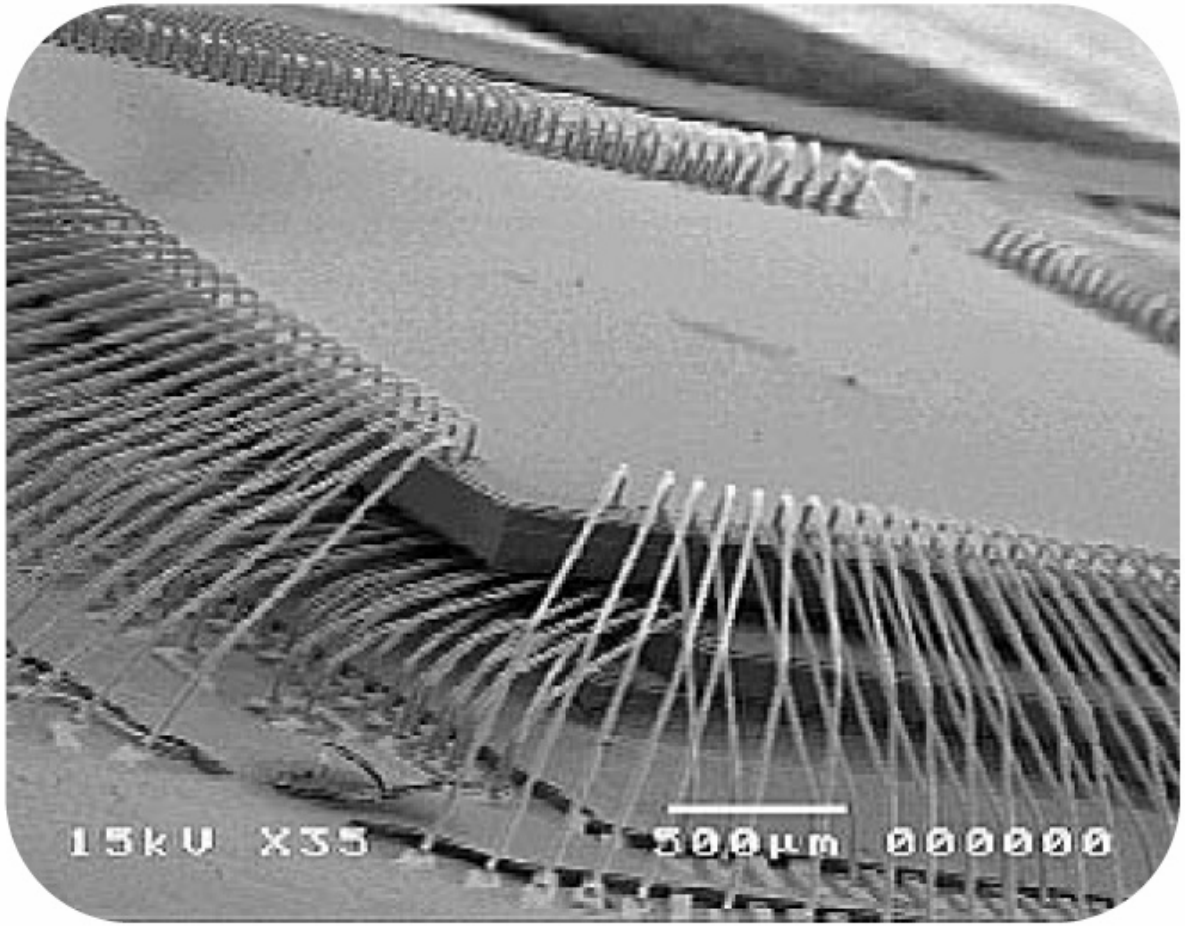
Band-3



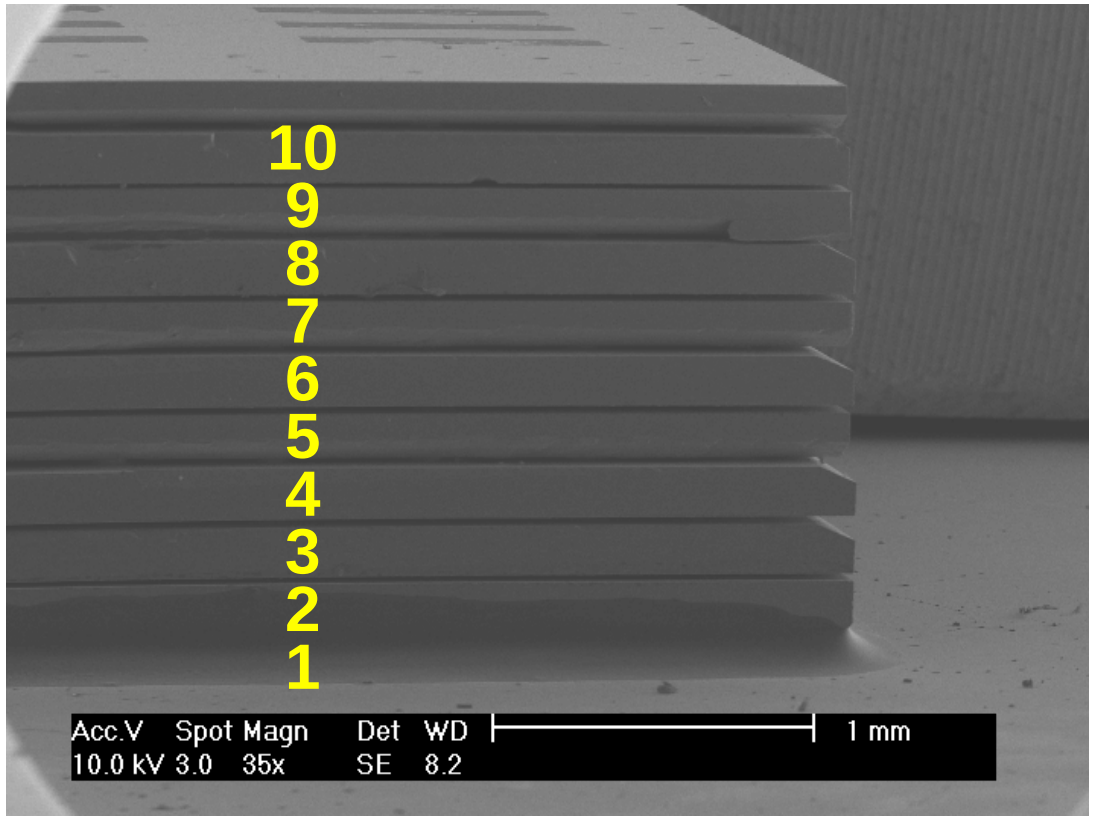


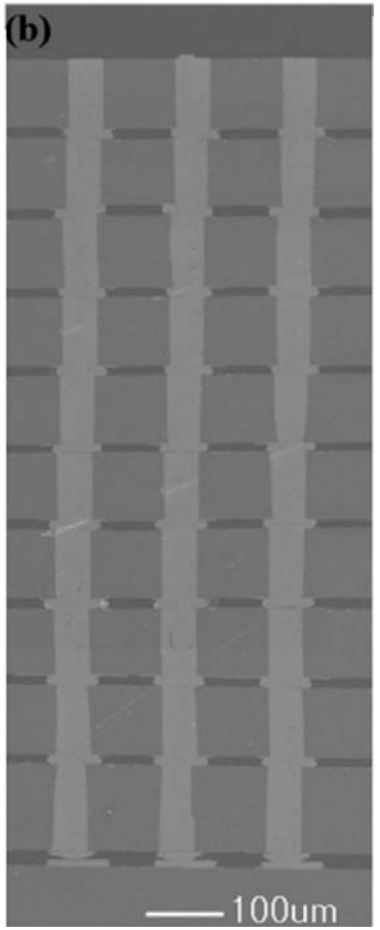
Clock Name	Operation Voltage	Operation Frequency
DACBITCLK	3.3V	2MHz
DACSYSCLK	3.3V	12MHz
SPIOCLK	3.3V	16MHz
TCK	3.3V	350kHz
TSCLK	3.3V	4MHz
TVCLK	3.3V	27MHz
VRCLK	3.3V	27MHz

Coupling in Wires for Stacked SiP



10 chip stacked Package by KAIST

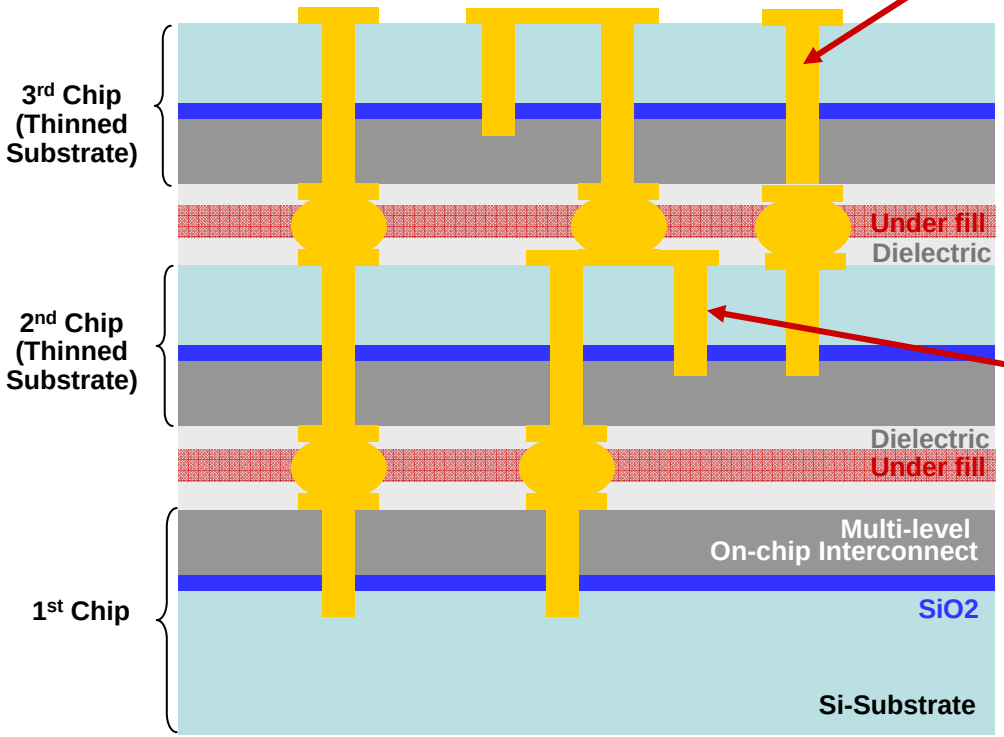




55 μm TSV diameter

150 μm Pitch

Key Technology : TSV (Through Silicon Via)

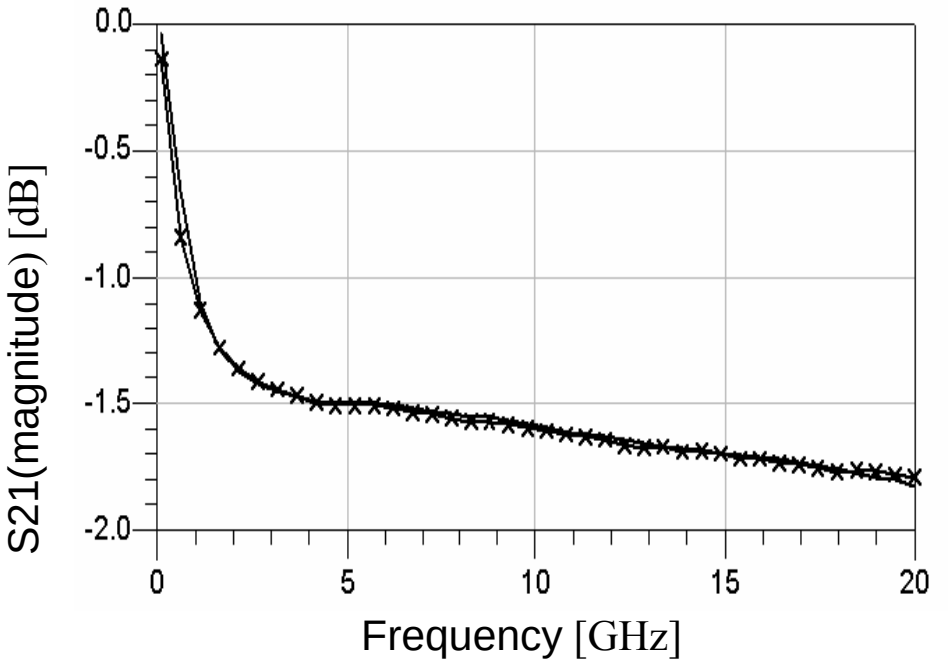


3D TSV Stacked IC

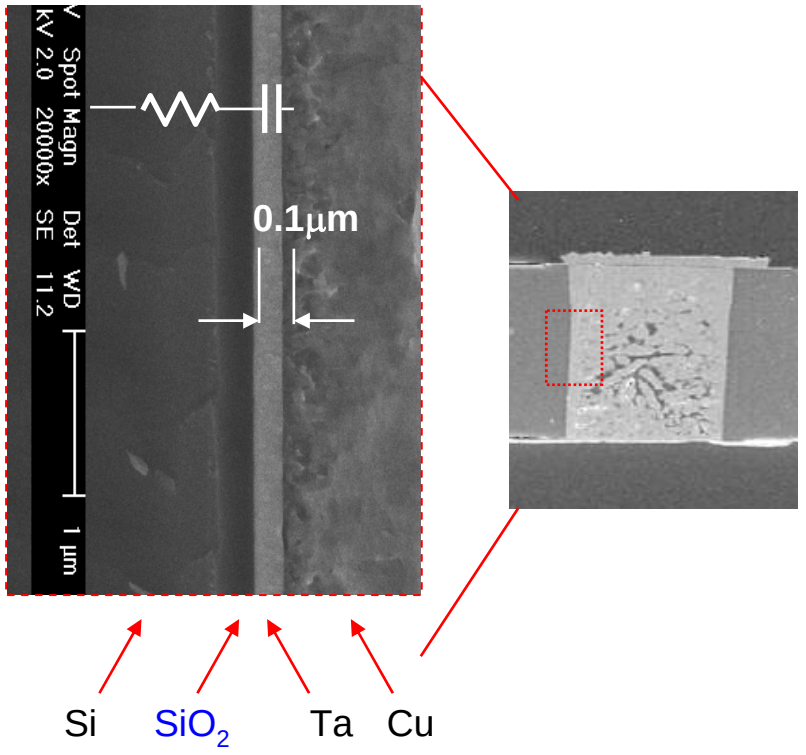
- **Short Interconnection**
  - → Reduced RC Delays
  - → Low Impedance for Power Distribution Network
  - → Low Power Consumption
  - → Heat Dissipation Through Via
- **No Space Limitation for Interconnection**
  - → High Density Chip Wiring
  - → No Limitation of I/O Number
  - → No Limitation of I/O Pitch
  - → Small Area Package

Background(1): High-frequency Channel Loss in TSV

-Significant high-frequency signal loss occur at Signal Transmission Through TSV
-The signal loss through TSV is caused by substrate leakage and coupling



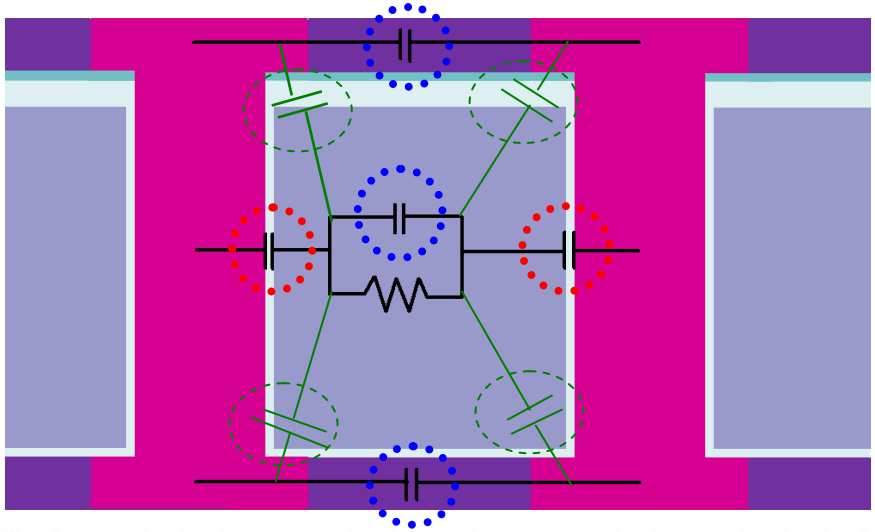
Magnitude of S21

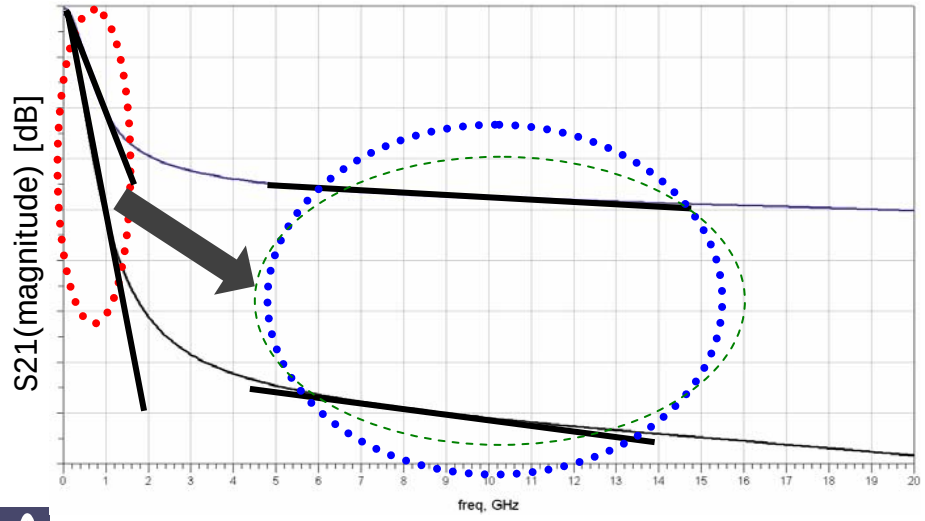


Close up of through wafer via

Loss characteristics of single-ended signal TSVs

➢ Electrical characteristics of signal TSVs: ① ***Capacitance***





C ∝ area , 1 / (distance)

Capacitance bet. metal & SiO2

Capacitance bet. metal & Silicon sub.

# of stacks ↑
Via diameter ↑
Bump diameter ↑

SiO2 thickness ↓

area ↑
distance ↓

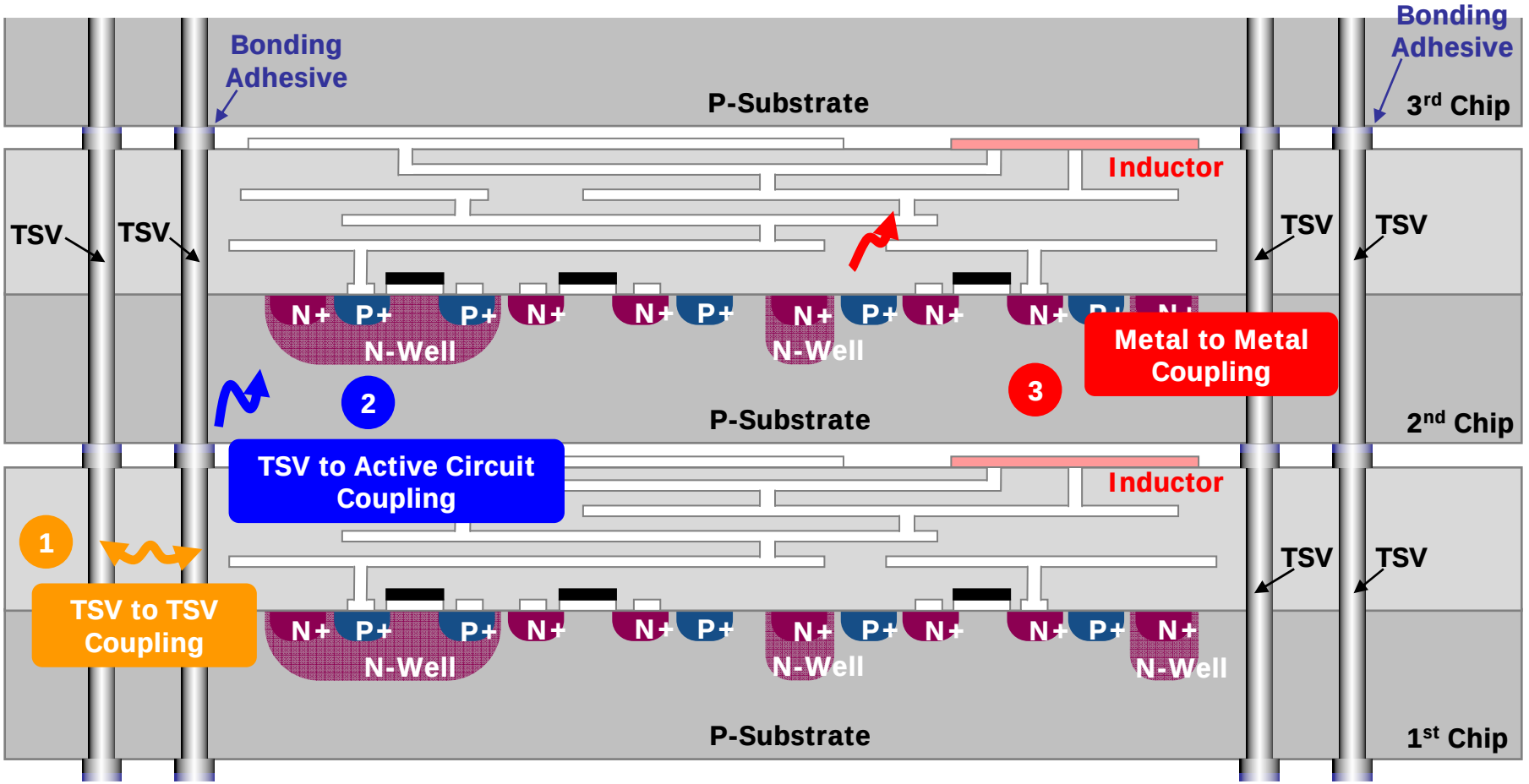
S21 slope ↑

Pitch bet. TSVs ↑

distance ↑

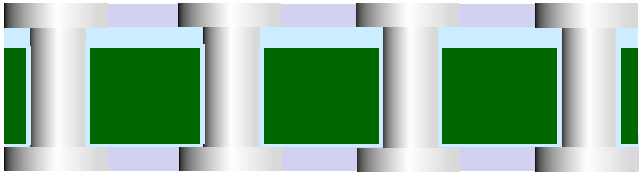
S21 slope ↓

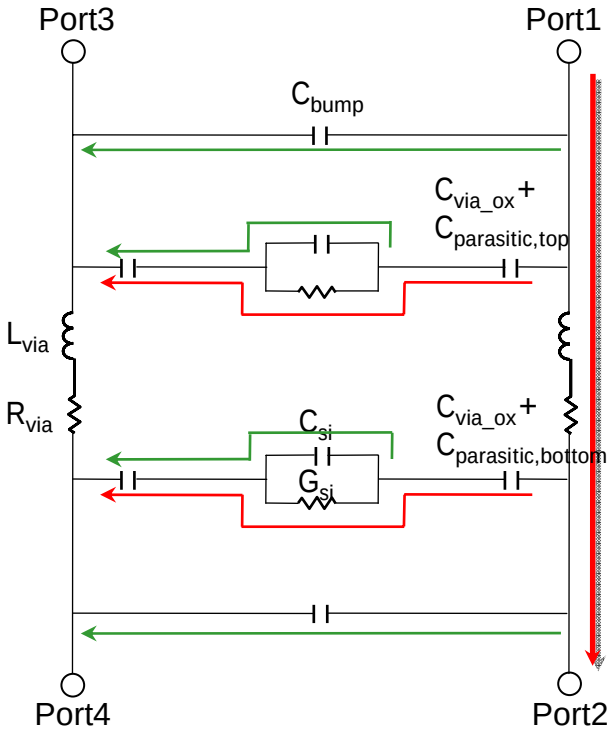
Coupling Issues in Stacked Dies using TSV

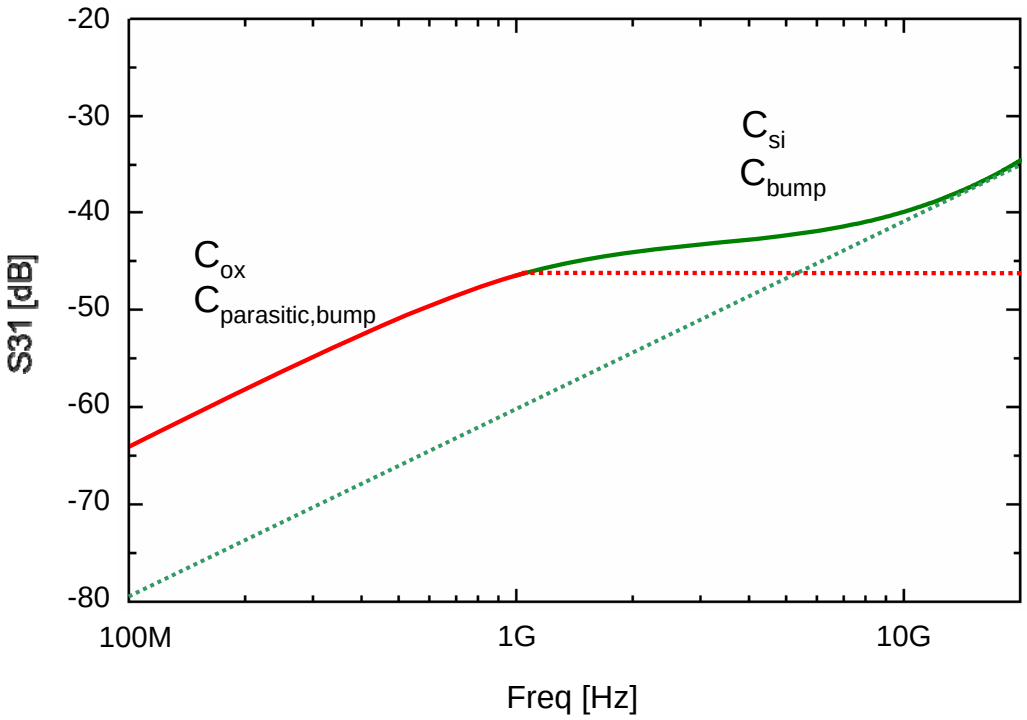


< CROSSSECTIONAL VIEW >

Crosstalk Mechanism Between TSV's





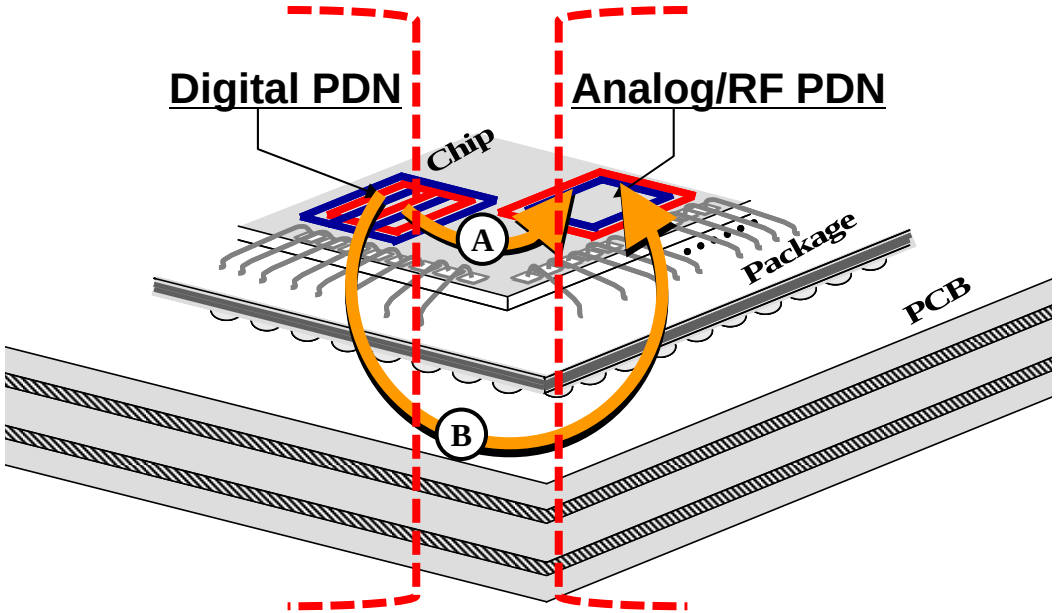


- Very small parasitic capacitances, C_{bump}, $C_{SiO2,top}$, $C_{SiO2,bottom}$ start to be in effect over GHz range
- R_{via}, L_{via} have very little effect on near & far end coupling

SSN coupling paths in SiP

- Wires of RX front end near digital power/ground wires
- Vias though digital power/ground planes
- Traces near digital power/ground traces
- Embedded passive components of RX front end : Balun, filter, coupler, and antenna

PDN Noise Isolation Methods



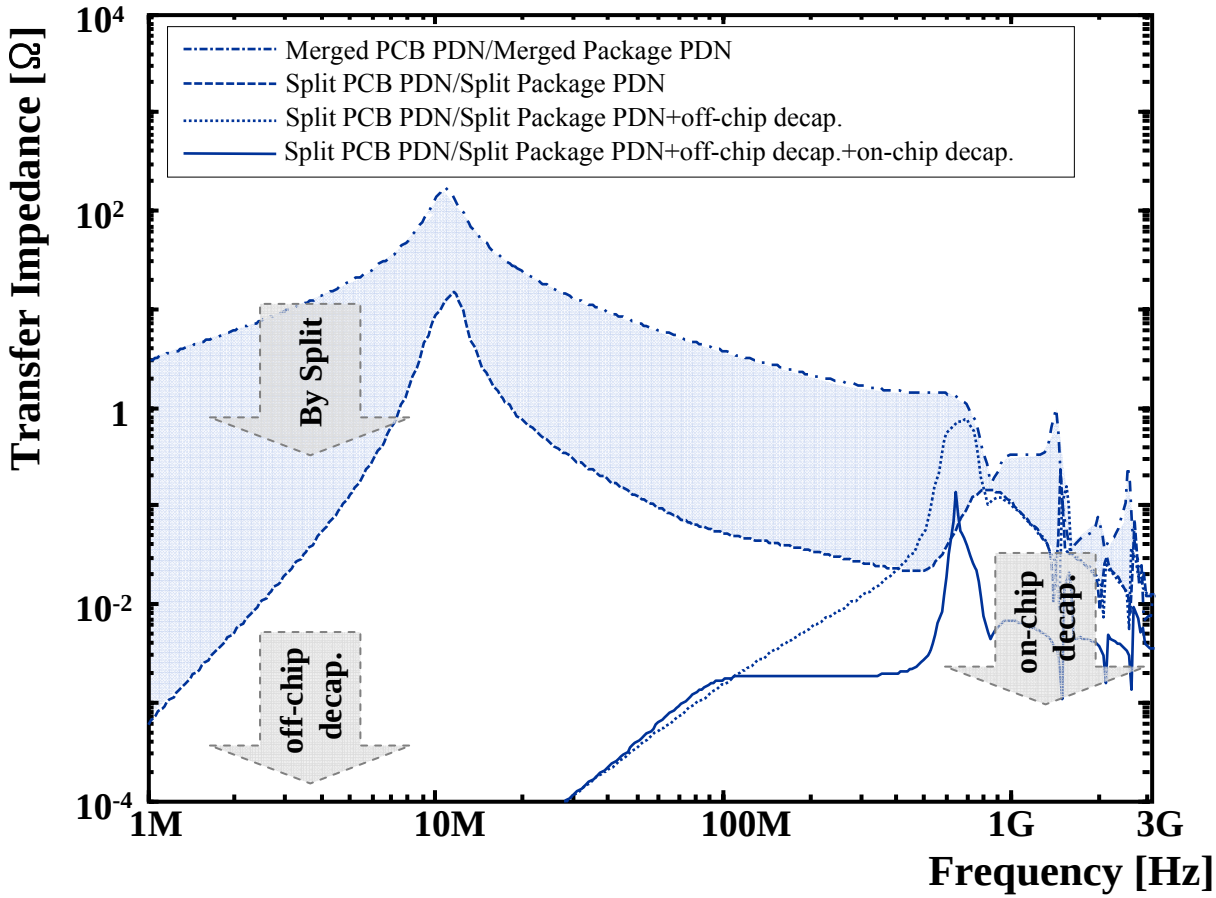
Ⓐ Chip Level
- Split On-chip Metal PDN Bus
- Guard Ring (P+/ N+/ Deep-Nwell type)
- On-chip Decoupling Capacitor
- Internal Voltage Regulator

Ⓑ Package/PCB Level
- Split Power/Ground Planes
- On-Package/PCB Decoupling Capacitor (Discrete type, Embedded type)
- Electromagnetic Band Gap (EBG)

→ **Frequency dependency of noise isolation**

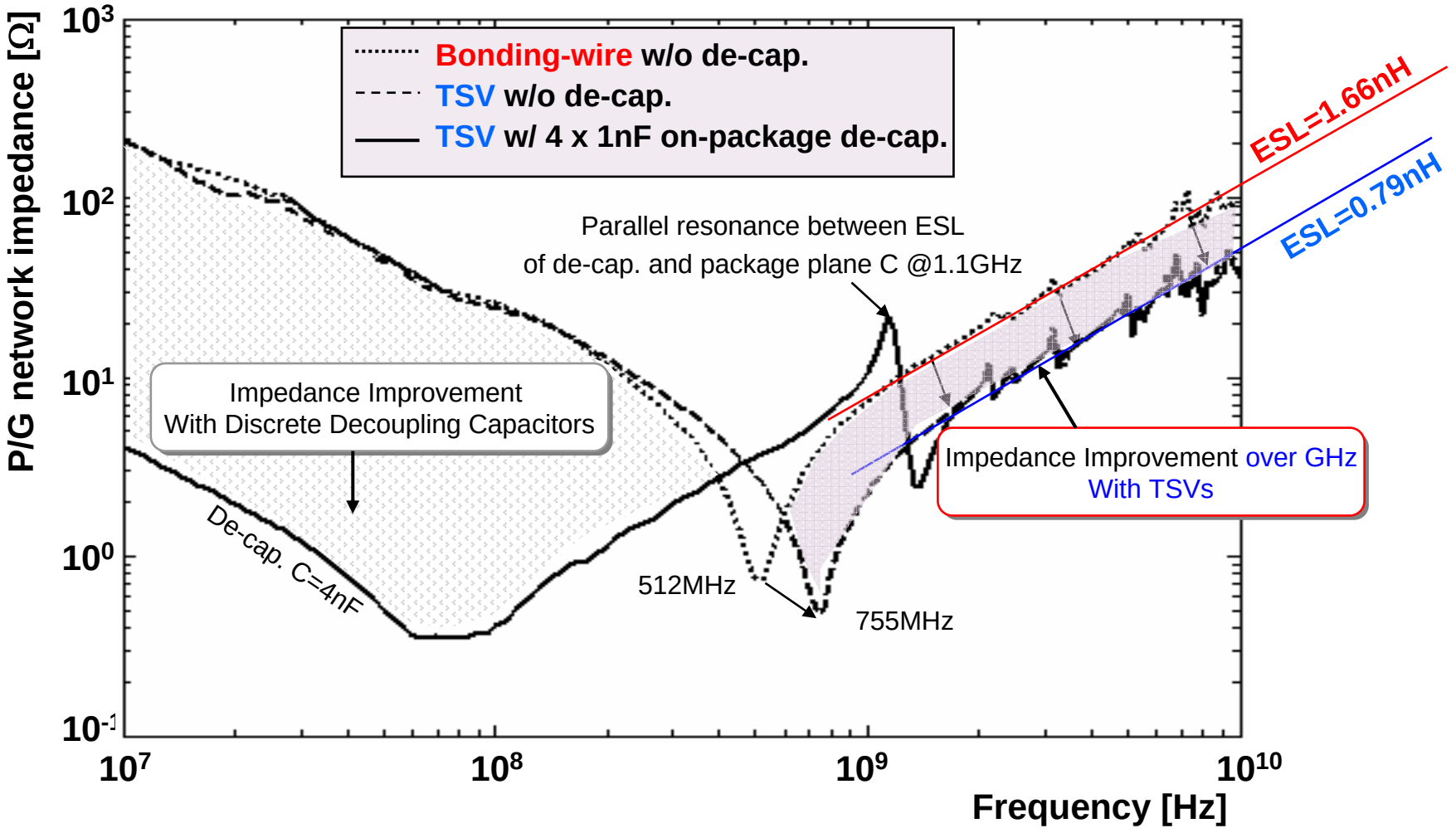
→ **Z21 analysis in the frequency domain**

The isolation methods of each hierarchical PDN



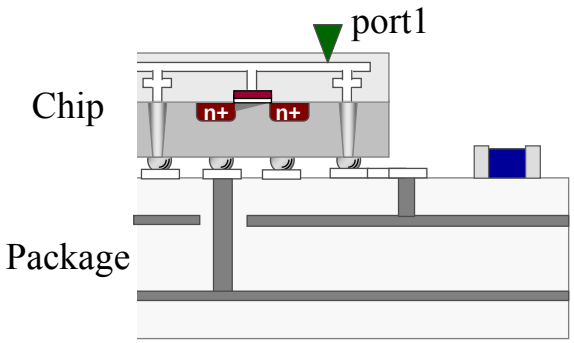
• By split of PCB and package level PDN,
the PDN transfer impedance can be suppressed except around 10MHz.
• By adding on-/off-chip decoupling capacitor,
the PDN transfer impedance can be suppressed in both low and high frequency region.

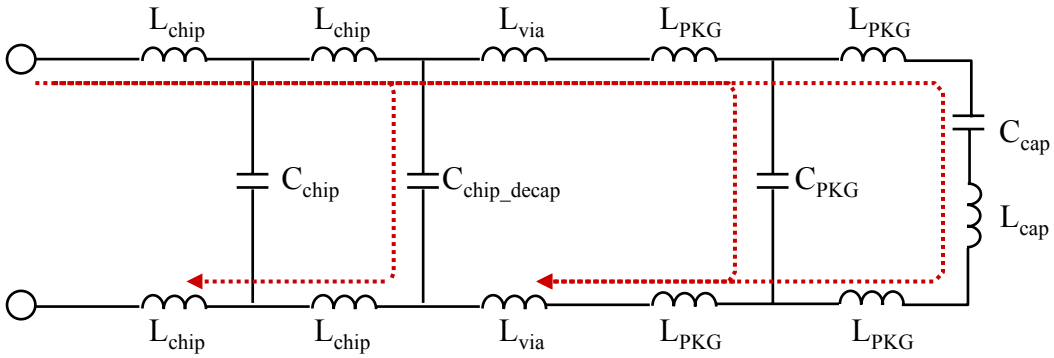
Measured PDN Impedances between TSV PKG and Bond-Wire PKG

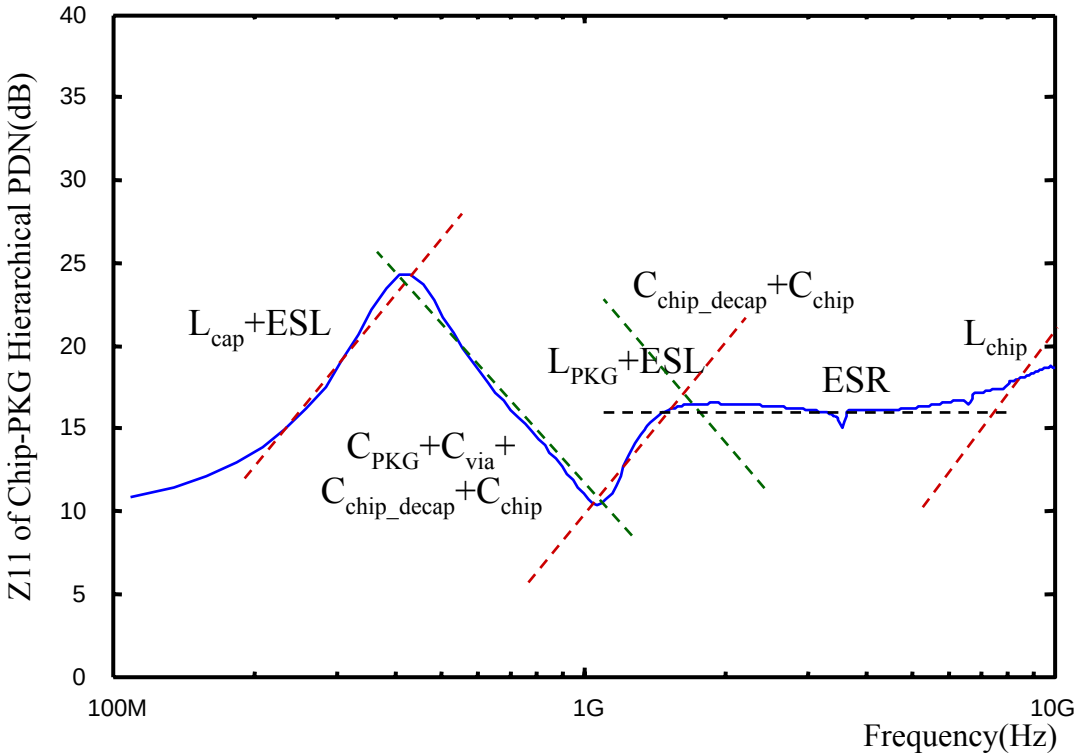


- Discrete on-package de-cap provides low impedance at the low frequency range (Large Capacitance)
- TSV reduces impedance over GHz range (Small ESL of TSV)

Characterization [3] : Chip-PKG-TSV







Cell Partitioning in EBG Structure with Embedded Film Capacitor

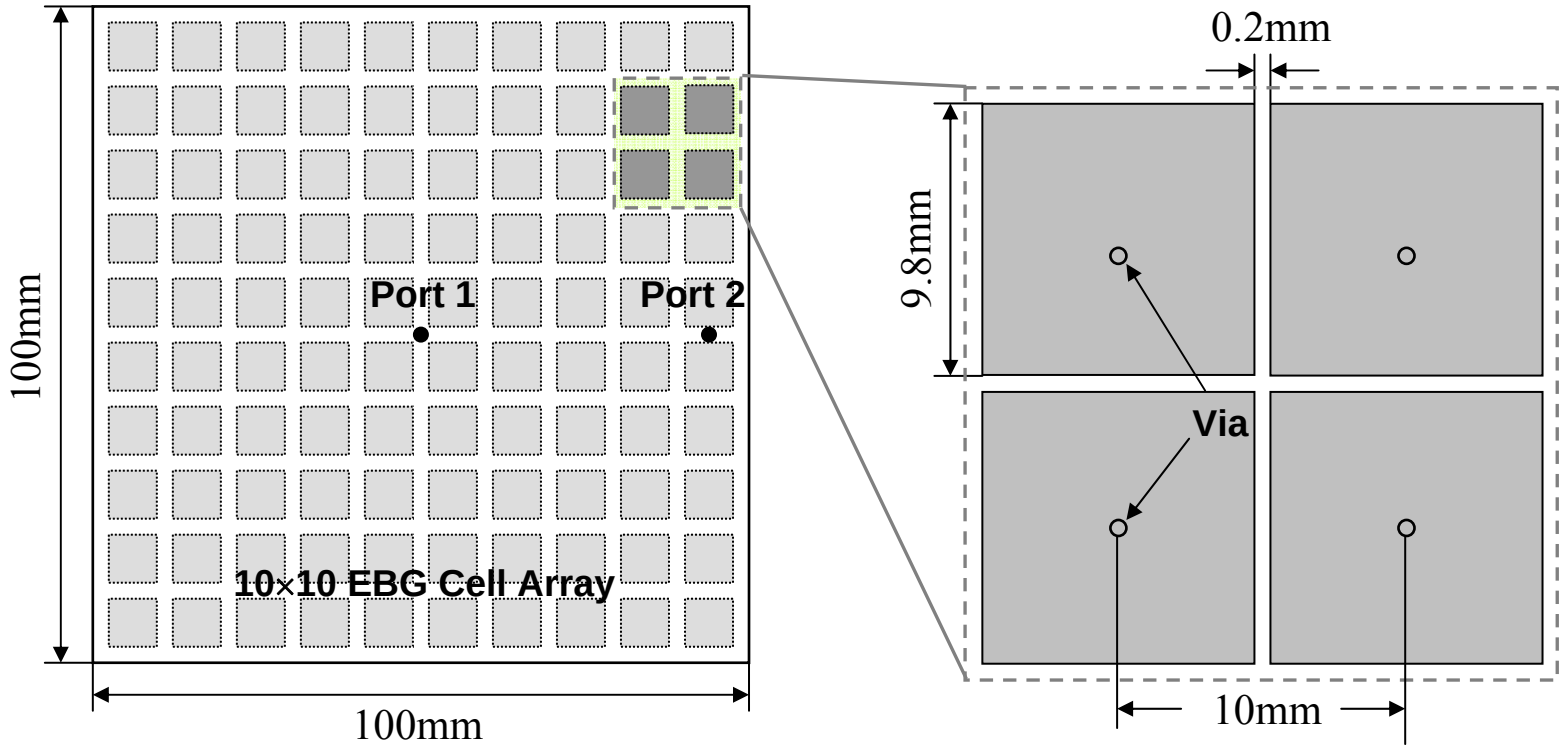


Fig.1. (a) The top view of the test vehicle with EBG structure. 10×10 EBG cells are arrayed in 100mm×100mm board. The measurement port 1and 2 locate at the center and the edge of the board, respectively.

Measured Z21, Transfer Impedance of PDN

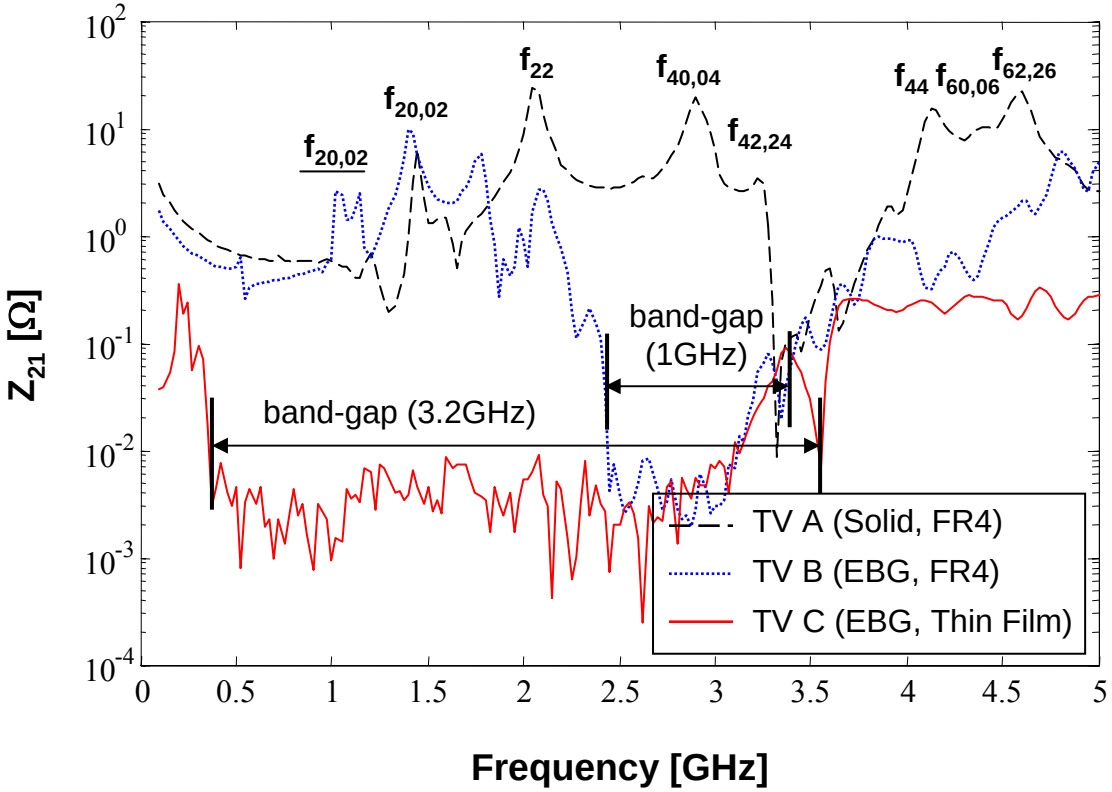
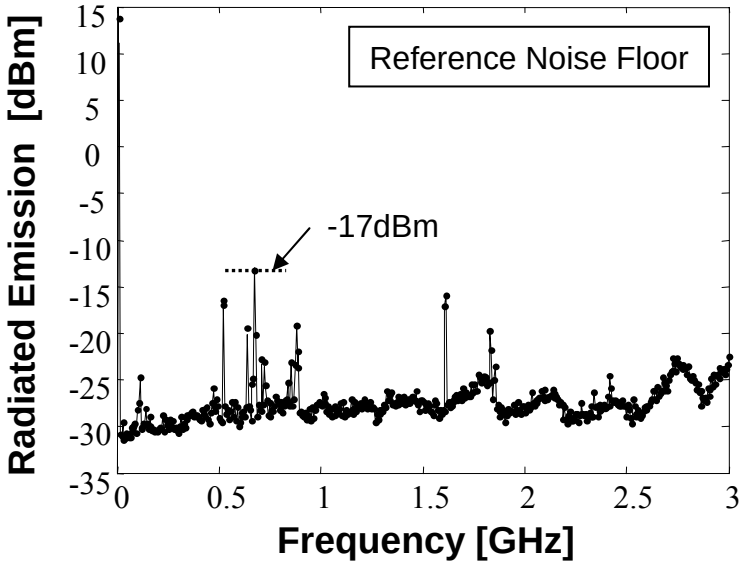
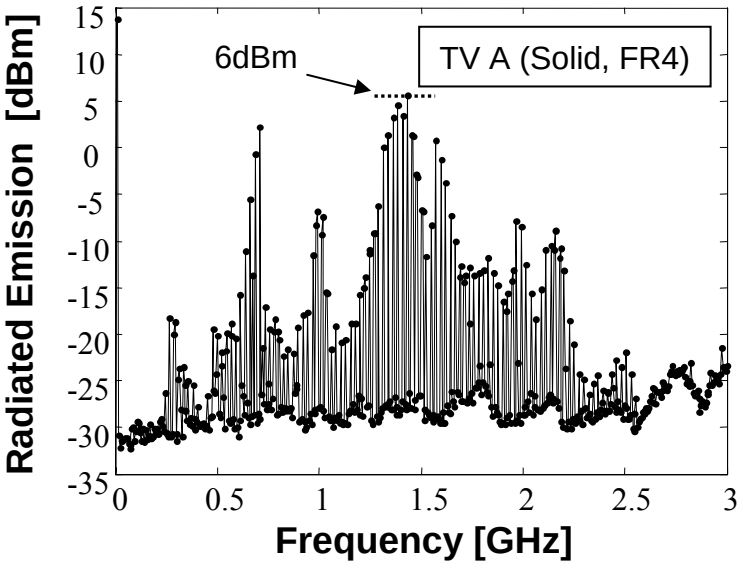
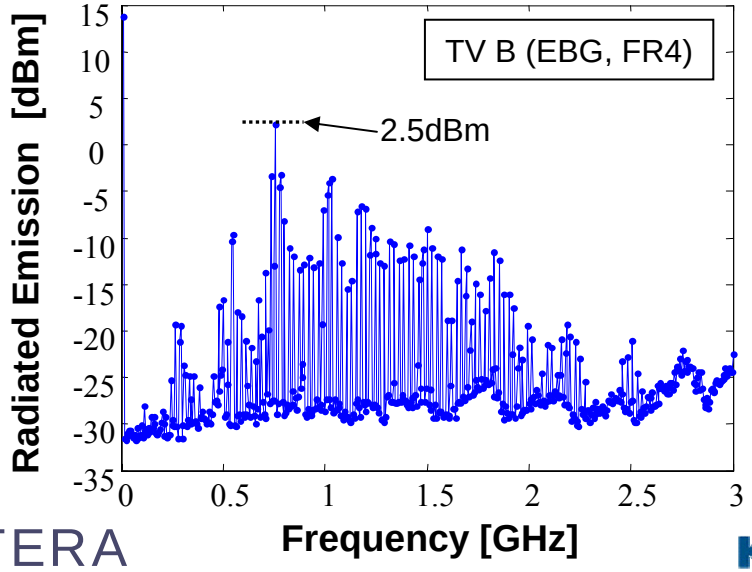


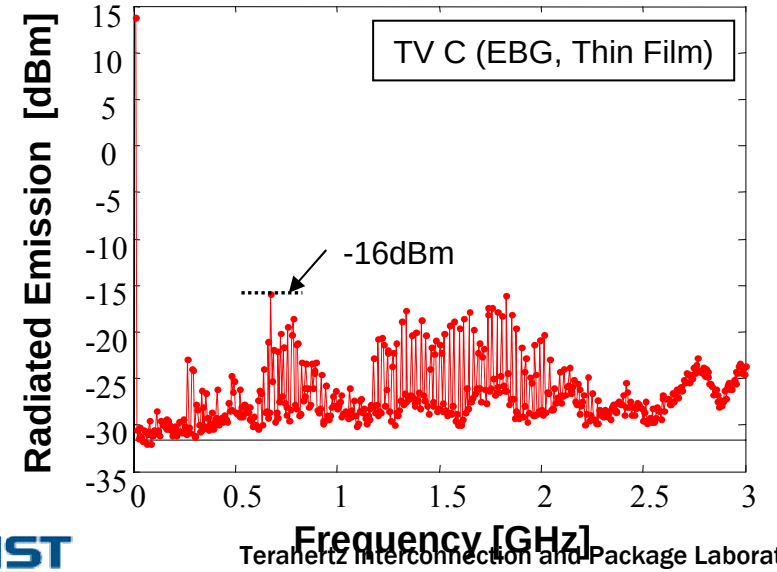
Fig. 3. (b) The measured transfer impedance curves between port 1 and 2: TV A (dashed line); TV B (dotted line); and TV C (solid line). TV C (thin film EBG) has band-gap from 300MHz to 3.5GHz and TV B (typical EBG) has band-gap from 2.3GHz to 3.3GHz.

Measured Radiated Emission Spectrum









Summary

- Significant noise coupling occurs from digital PDN to noise sensitive RF and analog circuits on a same SiP.
- The clock frequencies and harmonic frequencies should be placed away from the RF carrier frequencies.
- Low PDN impedance should be maintained.
- PDN resonance frequencies should be placed away not only from the clock frequencies, and their harmonic frequencies, but also from RF carrier frequencies.
- Via and wire are a major noise coupling path from digital PDN to noise sensitive circuits.
- Noise coupling reduction methods including using PDN design, frequency control, filtering, separation/isolation, decoupling, shielding, and grounding techniques.
- Chip-package co-design can provide optimal and cost-effective solutions.