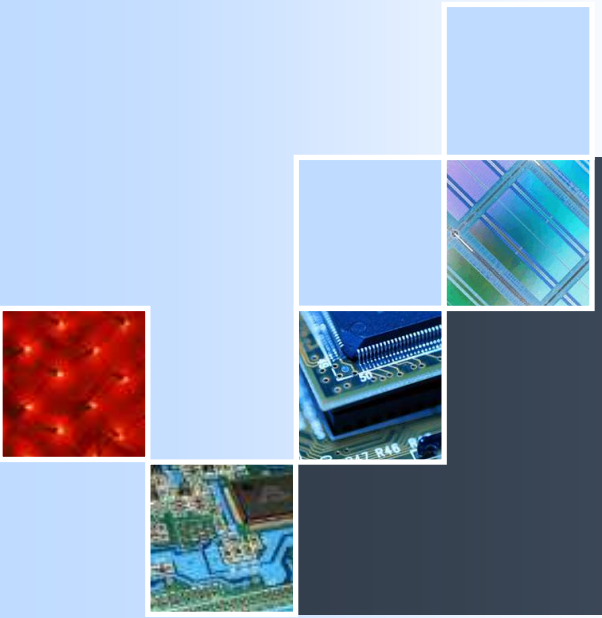

Trends and Requirements for System-Level Design of Signal and Power Delivery

EPEPS 2009

Future Directions in IC and Package Design Workshop

October18, 2009

Portland, OR

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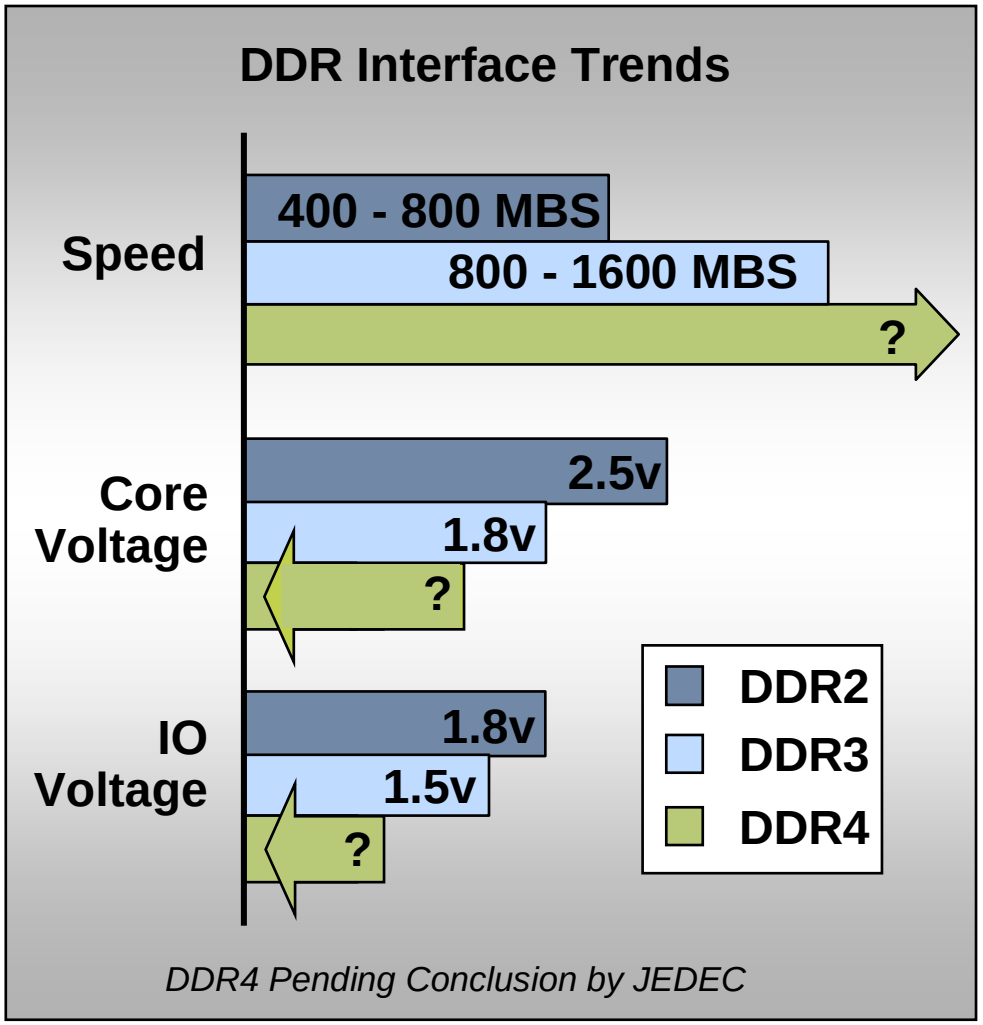
Agenda

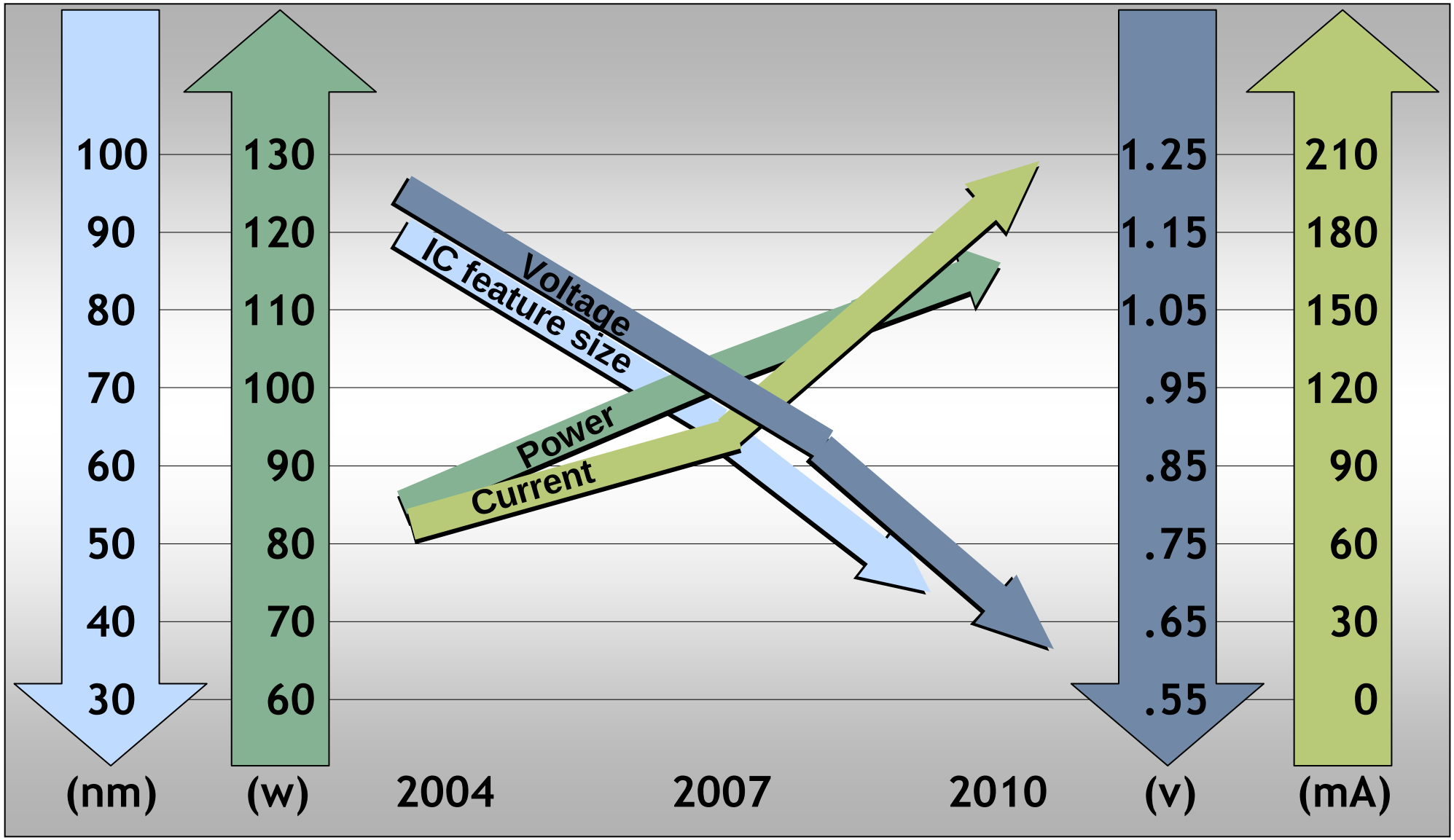
1. Whole-package/board SI and PI
2. System-level analysis for SI and PI
3. High-speed serial channel design

High speed interfaces exacerbate design challenges



- Increasing need for chip-package-board system analysis
- Similar challenges for SSO / SSN issues for even mainstream designs
- Power and ground behavior is paramount
- Similar challenges for SerDes, PCI-X, …

PDS trends affecting modern designs



1 - Whole-package/board SI and PI

Whole package/board analysis

- **To support system-level design the entire package/board must be characterized**
  - or at least a large enough portion of it to include all relevant SI and PI effects

- Circuit Simulation
  - SPICE has long been the standard
    - RF expatriates more familiar with frequency domain
    - frequency domain more amenable to model generation
  - very fast but accuracy bounded analysis
    - ideal PDN implicitly assumed, global node 0
    - designer must manually include couplings, some tools parse layout to automate

- EM Simulation
  - many techniques
    - integral/differential equations, time/frequency domain, planar/3D
  - high accuracy but capacity bounded analysis
    - too much computer time and memory
    - can simulate portions of real boards or small/isolated channels

Analysis technologies
application ranges

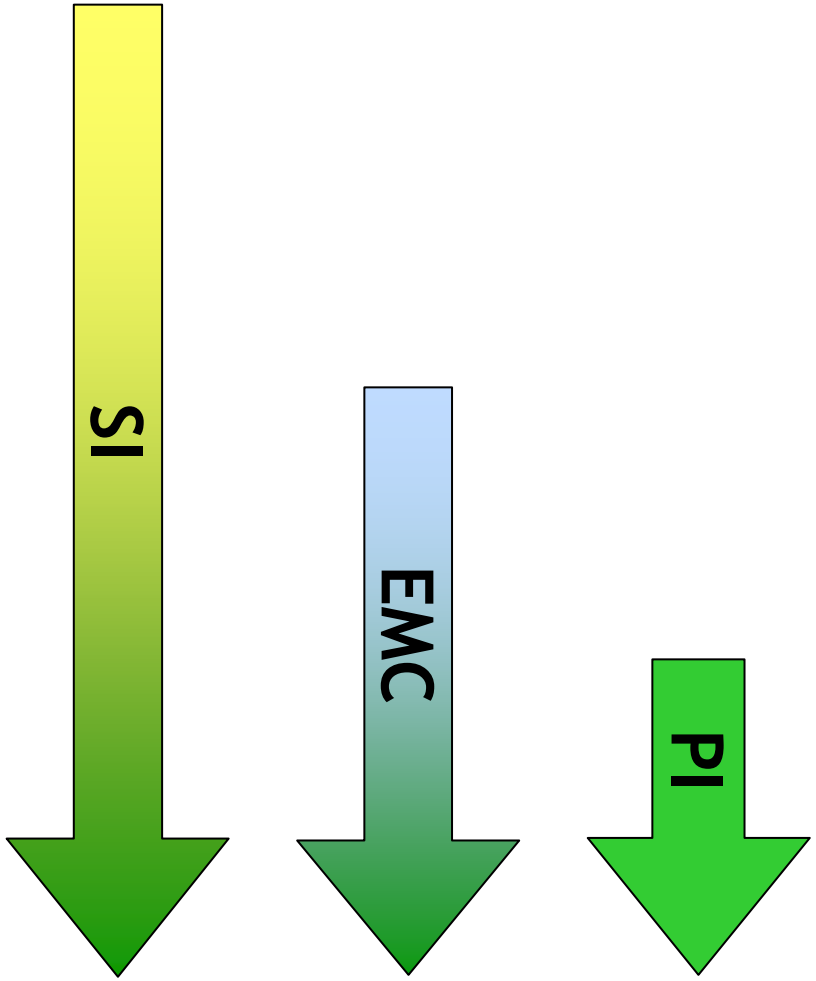
Technology

Circuit Simulation
circuits, systems

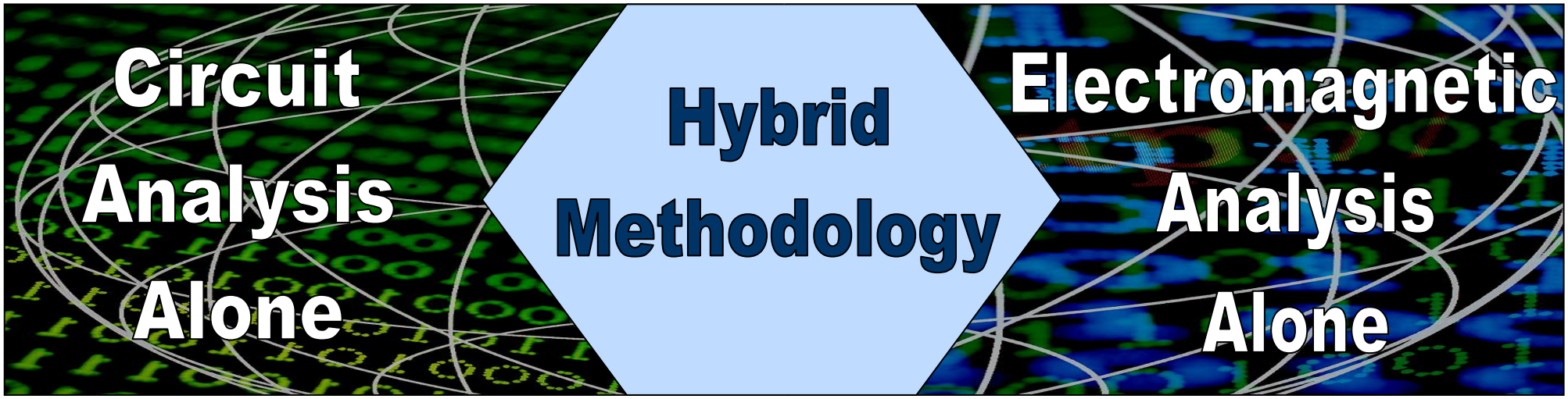
3D EM Simulation
components, small circuits

Hybrid EM-Circuit Solvers
boards, packages, systems

Application

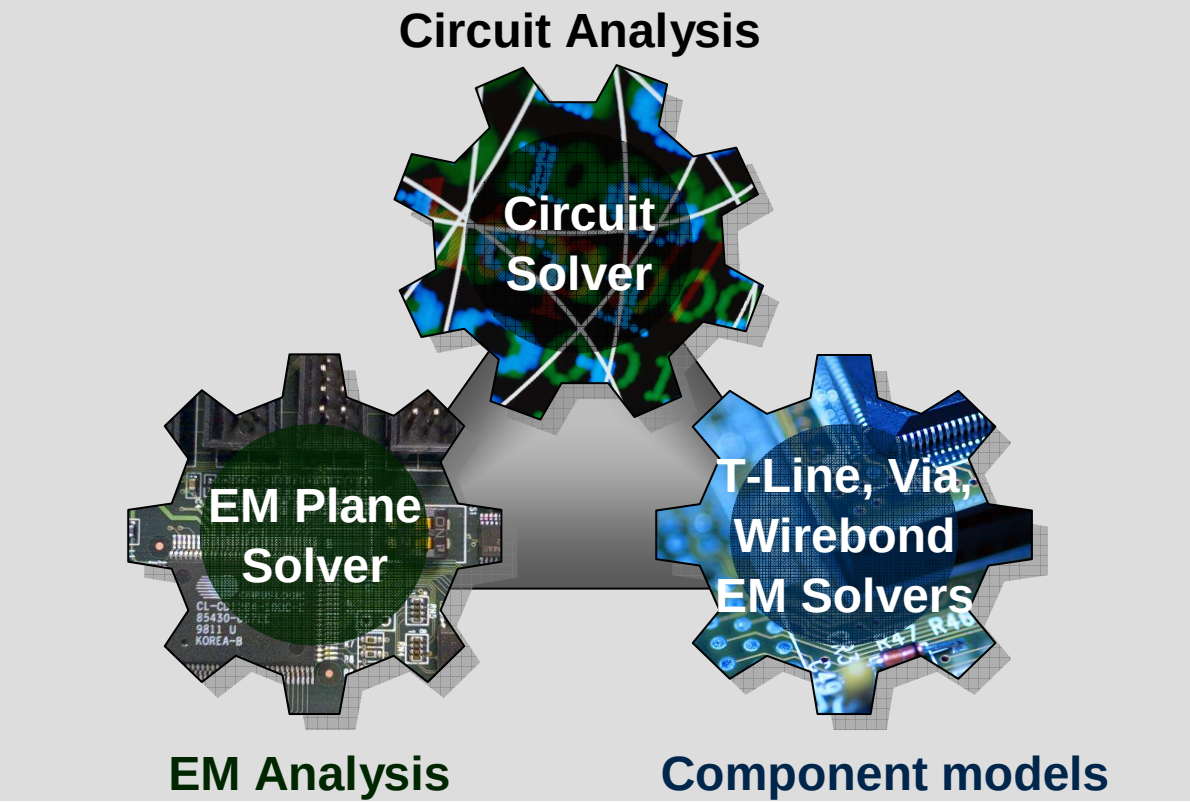


Hybrid solver technology challenges



- Maintain enough speed to enable whole-package/board analysis for modern designs (maximum *hours*, not *days*)
  - packages of 10(+) layers, 5000 or more pins
  - board with 20(+) layers, 10(+) ASICs/FPGAs
- Support enough "full-wave behavior" to enable accurate analysis
  - coupling and referencing within the design
  - loading exterior to the design
- Provide both frequency and time domain analysis capability
  - frequency domain provides models for subsequent system analysis
  - time domain allows IBIS drivers and arbitrary signaling conditions
- Interact effectively with circuit-only and EM-only analyses

Three classes of solvers working together



SPICE

Modified Nodal Analysis

$$\begin{pmatrix} Y & C \\ C^T & Z \end{pmatrix} \begin{pmatrix} v \\ i \end{pmatrix} = \begin{pmatrix} i_s \\ v_s \end{pmatrix}$$

Hybrid Solver Technology

Combined Ckt/EM Nodal Analysis

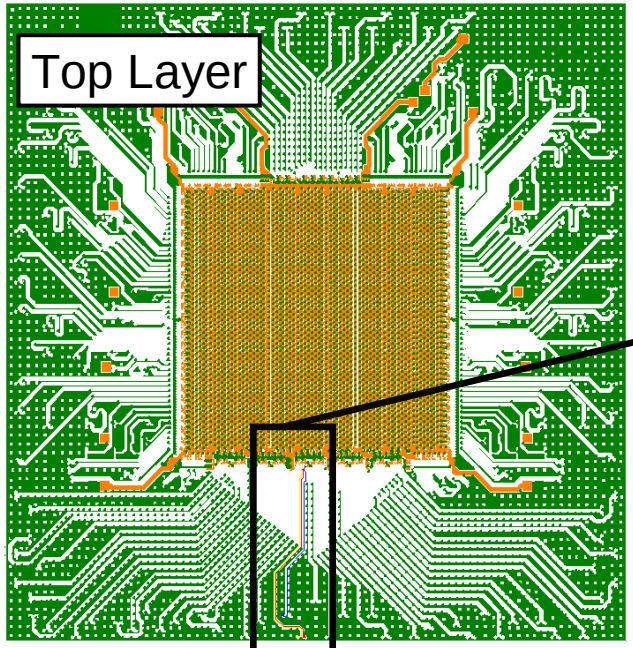
$$\begin{pmatrix} Y_{ckt} & Y_{ckt\text{-}EM} \\ Y_{EM\text{-}ckt} & Y_{EM} \end{pmatrix} \begin{pmatrix} v_{ckt} \\ v_{EM} \end{pmatrix} = \begin{pmatrix} i_{ckt} \\ i_{EM} \end{pmatrix}$$

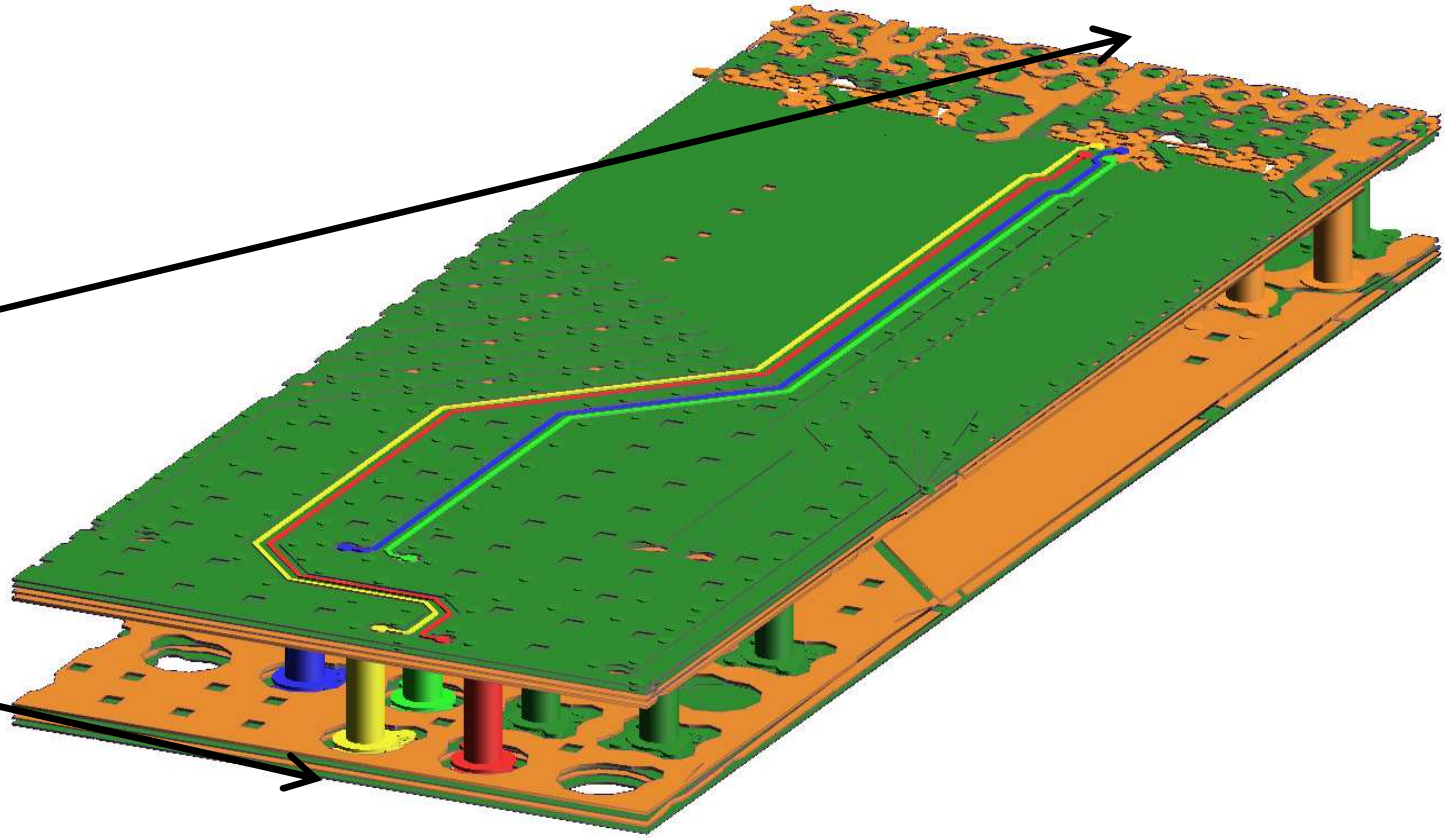
Hybrid solver algorithms

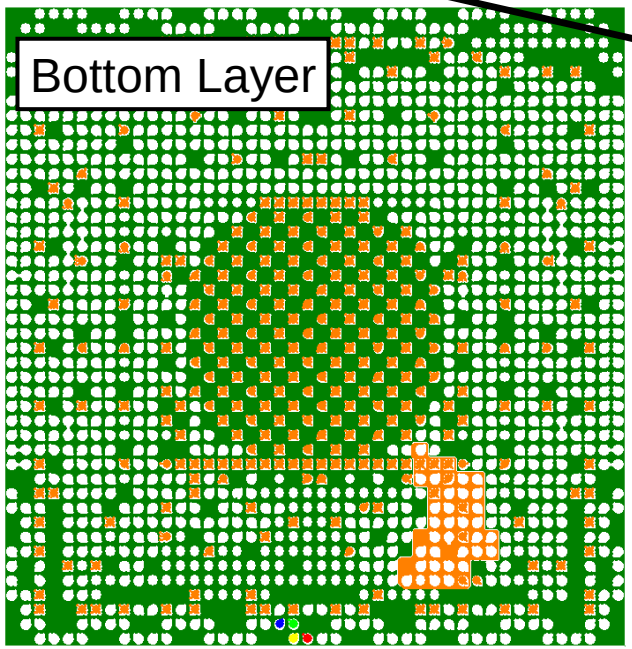
1. Parse layout
   - components: nets, pads, vias, wirebonds, etc
   - planes
   - interactions of components and planes
     - vias through multiple planes, nets crossing voids/splits, via-to-via coupling
2. Setup circuit portion
   - create a virtual netlist
   - determine couplings, loadings, etc
   - create required component models
3. Setup EM portion
   - determine multi-layer topologies
   - discretize (mesh)
4. Setup circuit-EM interactions
   - implement connectivity
   - analytical and numerical interactions
5. Simulation
   - time or frequency domain composite analysis
6. Save, postprocess and display results
   - terminal characteristics (S/Y/Z-parameters)
   - node and plane voltages, branch currents
   - compute emissions (*from branch currents and plane-edge voltages*)

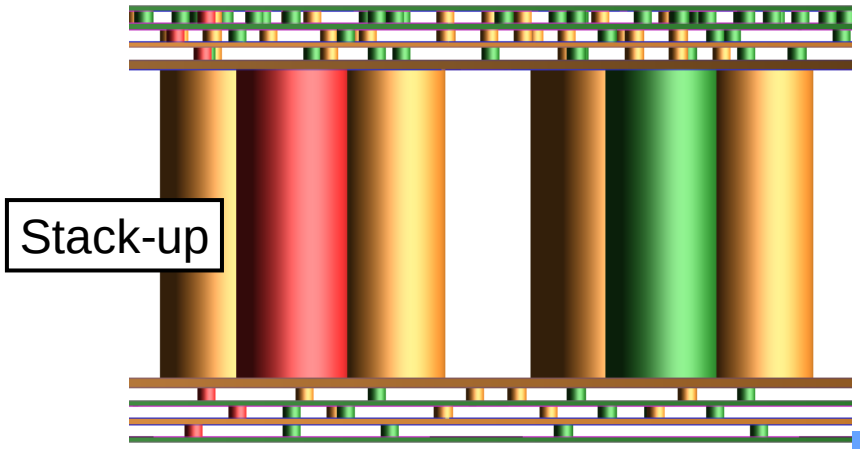
$$\begin{pmatrix} Y_{ckt} & Y_{ckt\text{-}EM} \\ Y_{EM\text{-}ckt} & Y_{EM} \end{pmatrix} \begin{pmatrix} v_{ckt} \\ v_{EM} \end{pmatrix} = \begin{pmatrix} i_{ckt} \\ i_{EM} \end{pmatrix}$$

Two high speed diff pairs in a package







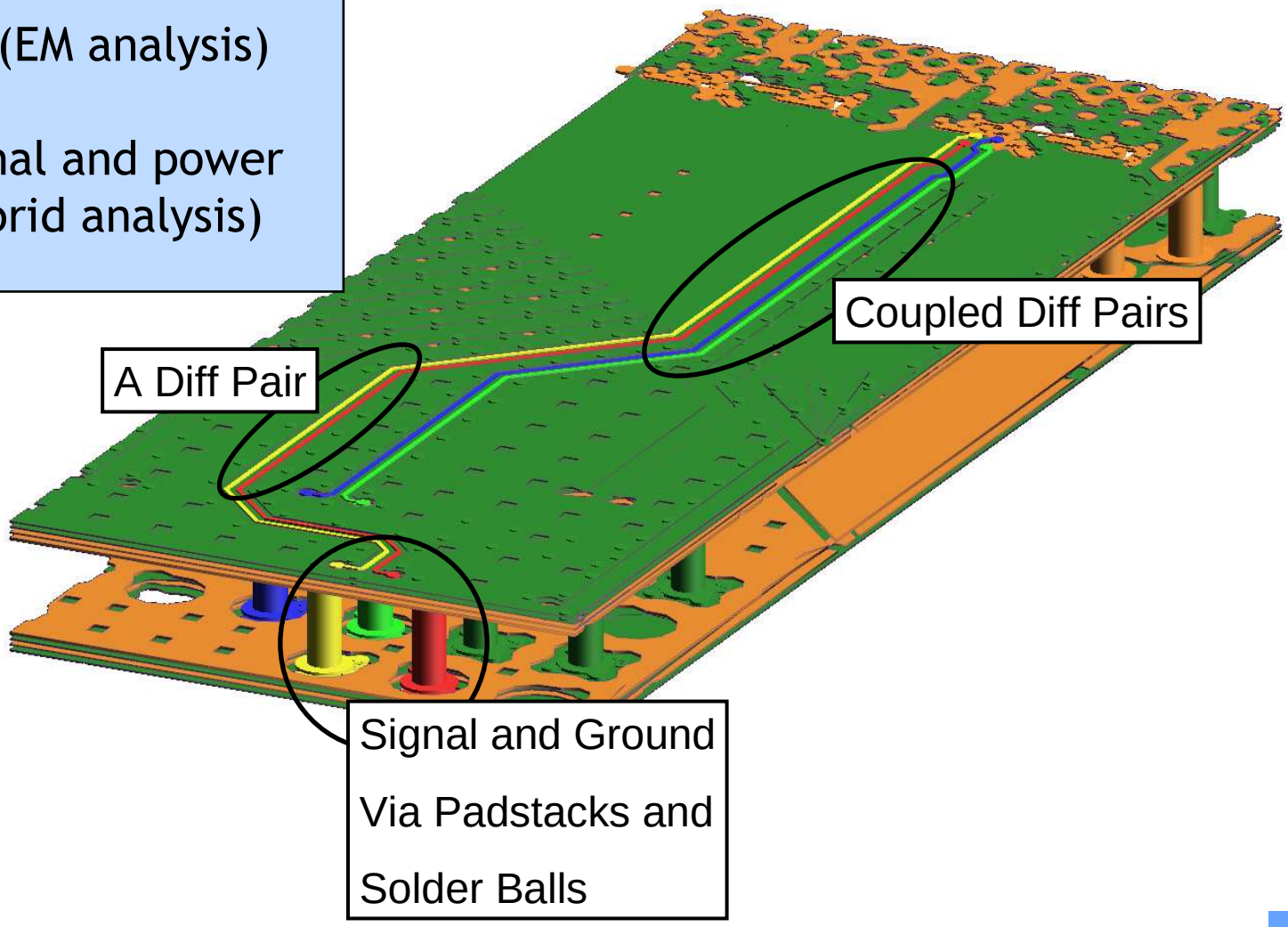


Schematic-level Circuit Modeling with Component Models

A concatenation of individual components? (circuit analysis)

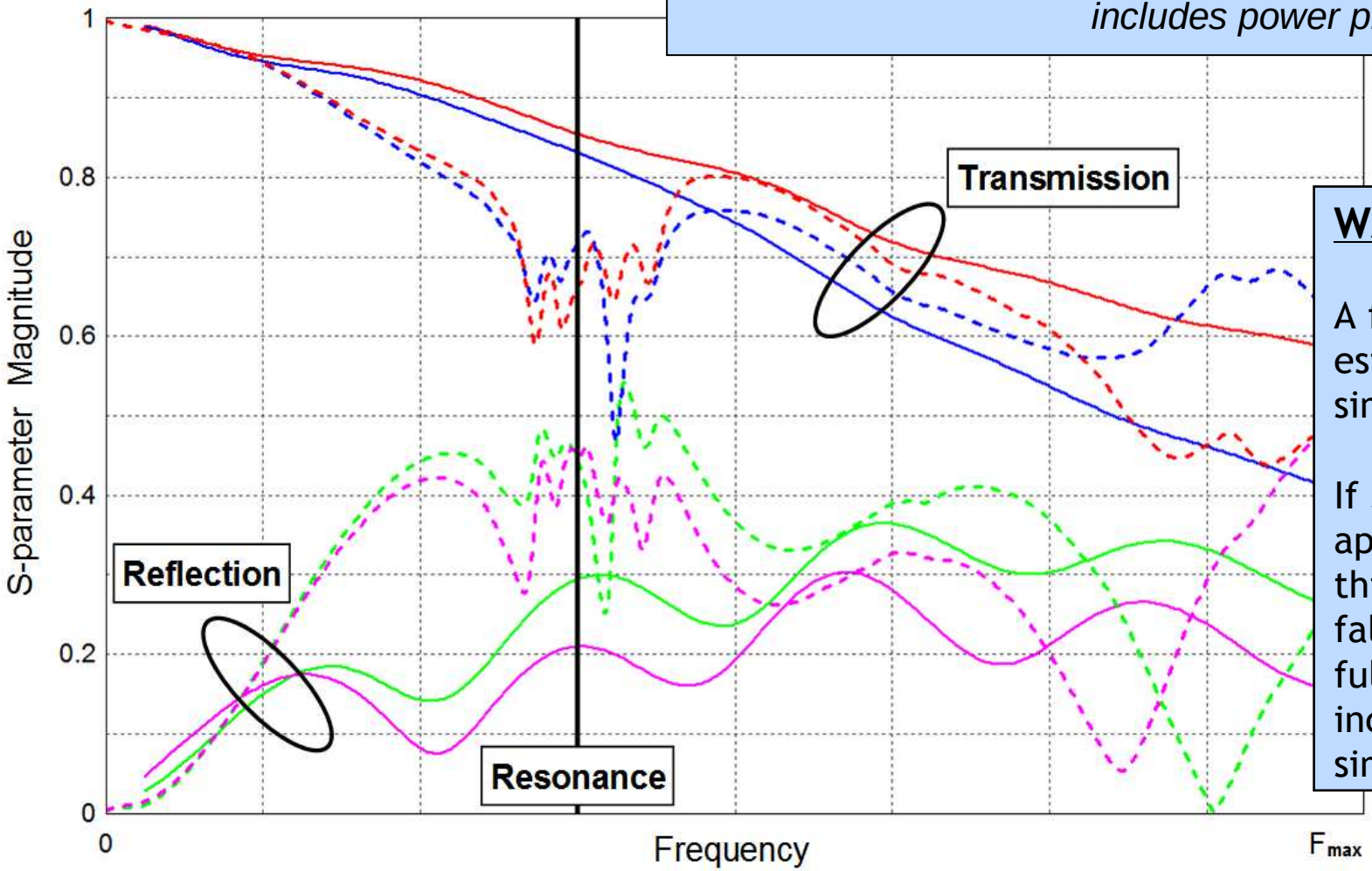
One big component? (EM analysis)

A part of a bigger signal and power delivery system? (hybrid analysis)



Power integrity *and* signal integrity !

solid lines	Circuit Analysis *and* 3D EM Analysis *(channels and locally-shorted planes, loss, slight impedance mismatch)*
dashed lines	SI/PI Full-package Analysis (*channel and full planes, includes power plane resonances)*

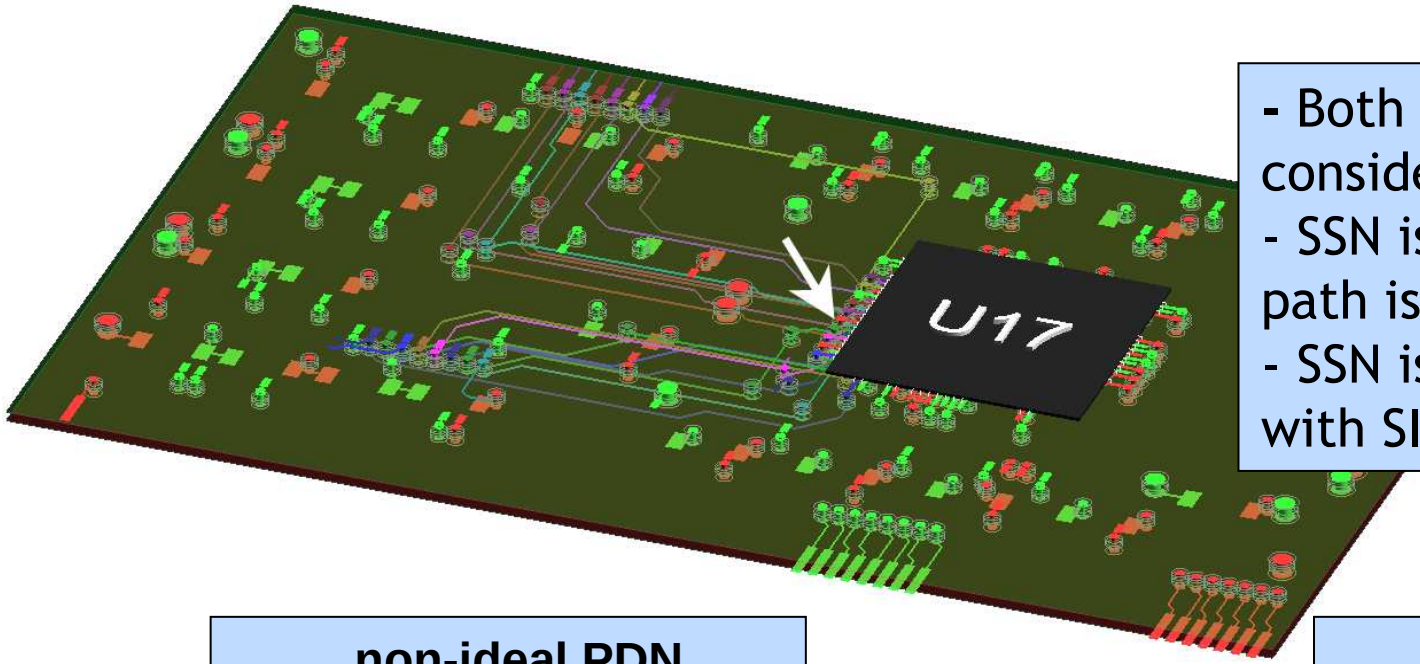


WARNING:

A false sense of security is established if only circuit simulation is applied.

If 3D EM simulation is later applied as a "verification", this sense of security can falsely be reinforced if the full power planes are not included properly in the simulation.

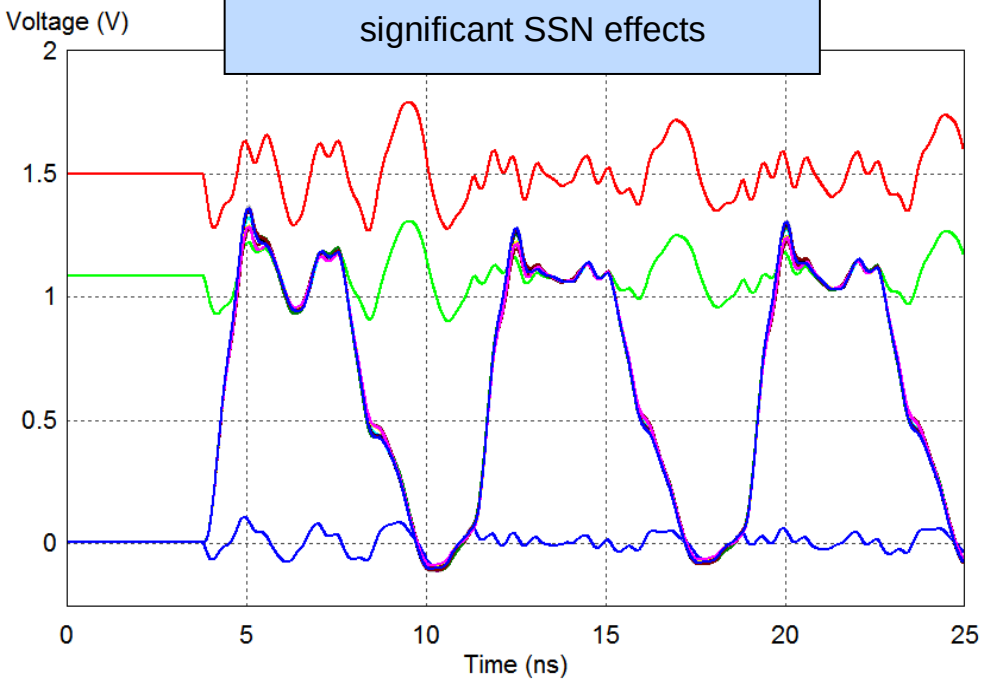
Simultaneous switching noise (SSN)



- Both SI and PI must be considered … simultaneously.
- SSN is dominated by return path issues.
- SSN is grossly underestimated with SI-only analysis tools.

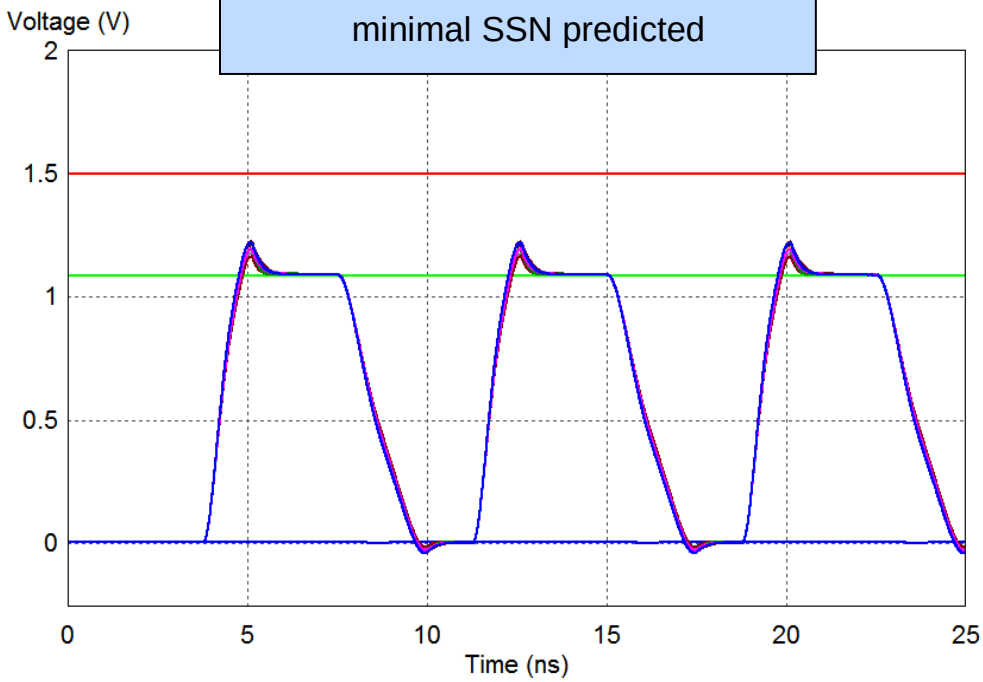
non-ideal PDN

significant SSN effects

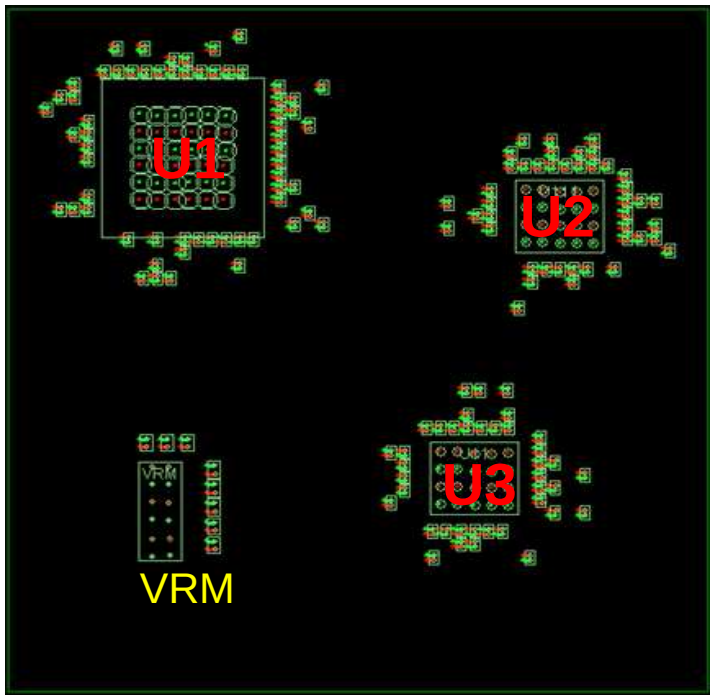


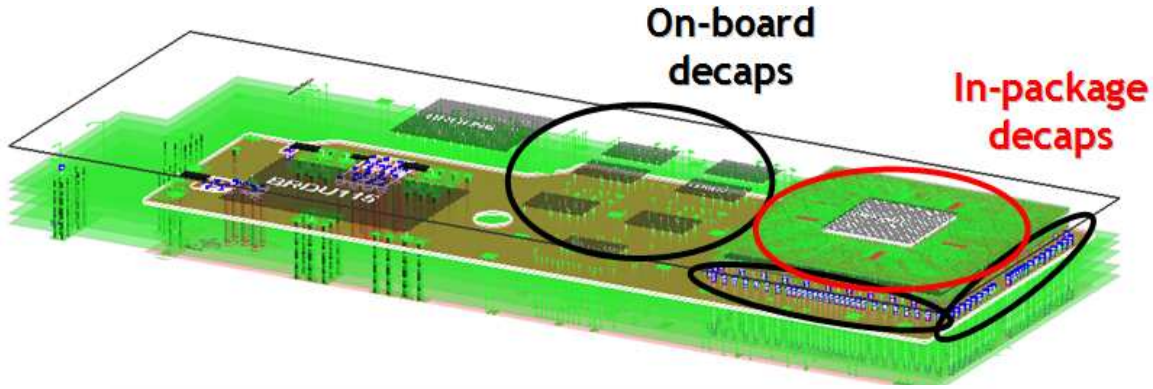
ideal PDN

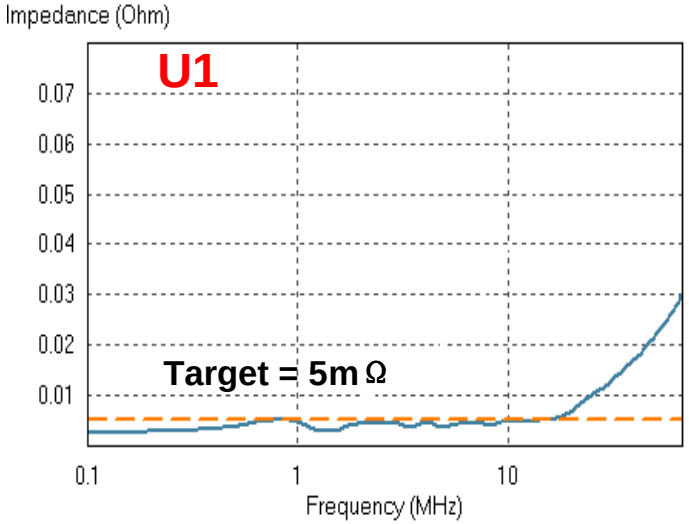
minimal SSN predicted

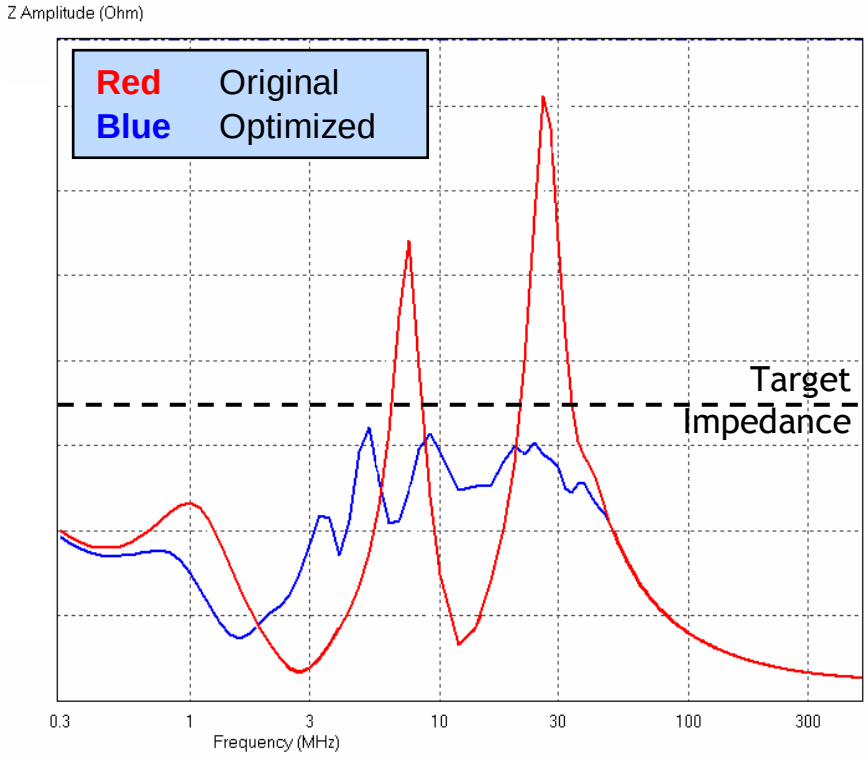


Perform PDS pre-route and post-layout design tradeoffs amongst: *performance-cost-area*

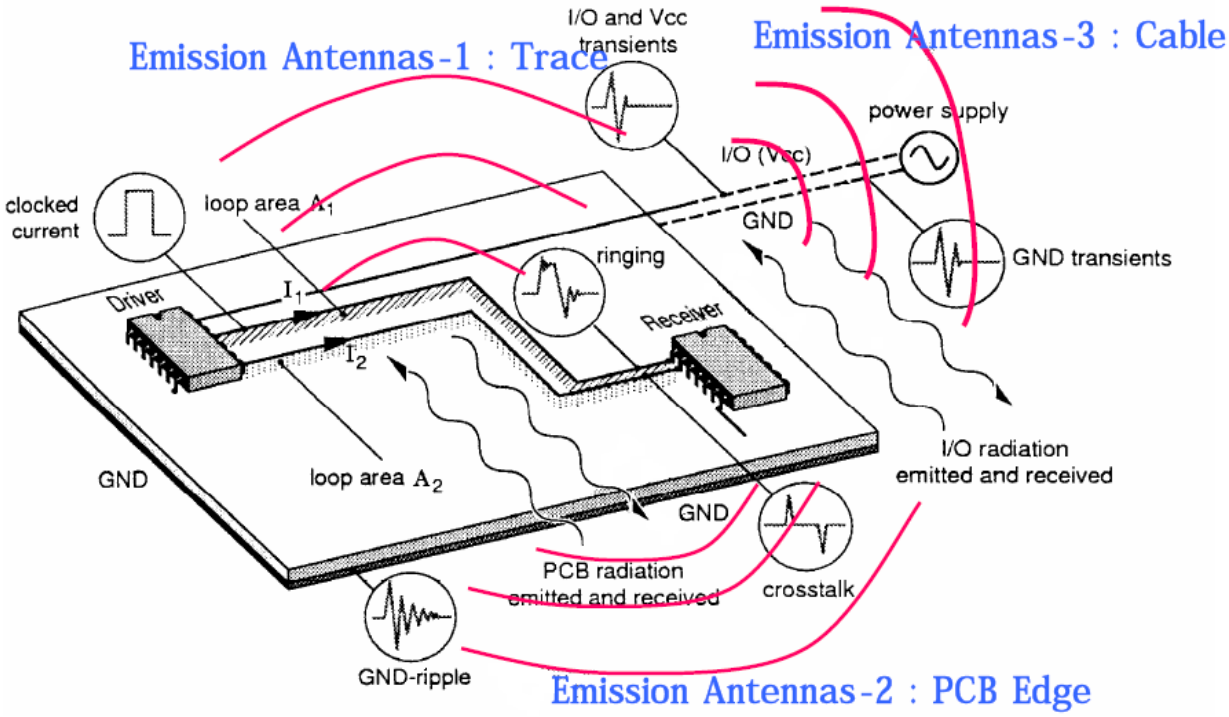


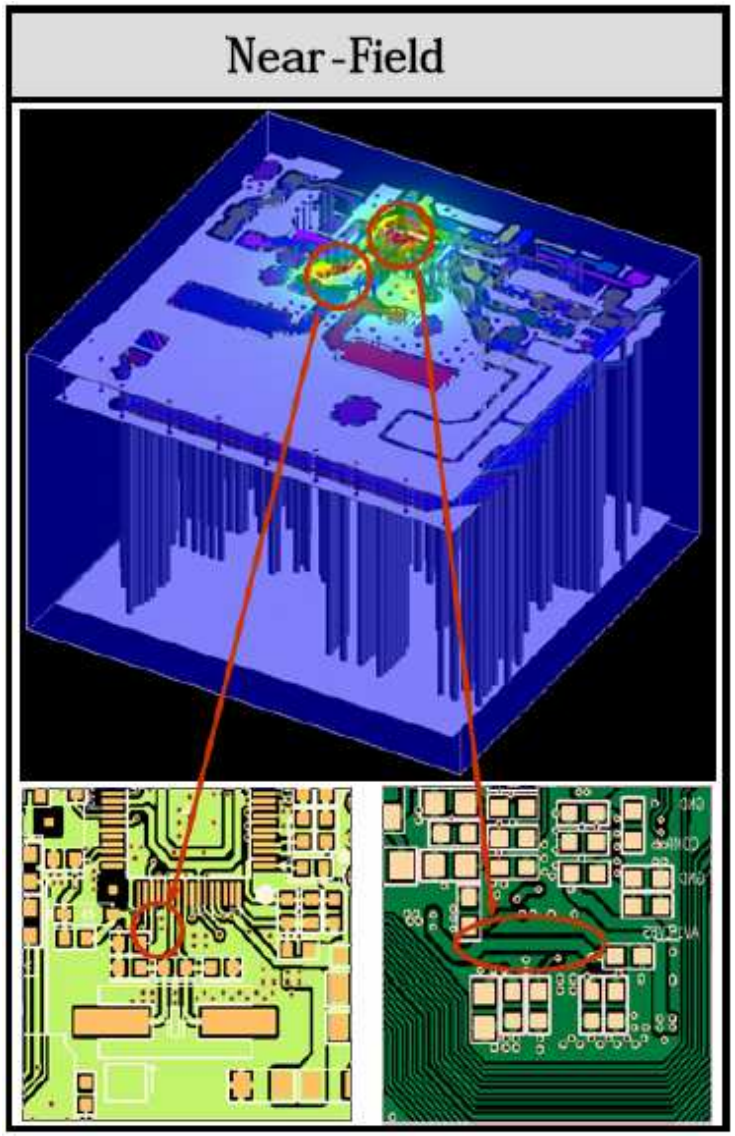






Predict and address EMC issues early in the product development cycle





Package performance *assessment* vs. *extraction*

- Performance assessment
  - dictionary definition of “assessment”
    - a judgment about something based on an understanding of the situation
  - the objective
    - an indication of quality or viability of the package design
  - numerical value and qualitative judgment are equally important’
    - higher level information to support decisions, shared with non- experts
  - usually performed earlier in the package design flow
    - a more iterative process

- Model extraction
  - dictionary definition of “extraction”
    - to obtain something from a source, usually by separating it out from other material
  - the objective
    - an electrical model to support subsequent analysis
  - numerical value and accuracy are important
    - lower level detail, shared with simulation experts
  - usually performed later in the package design flow
    - a non-iterative step, often a verification type step

Support of IC designers

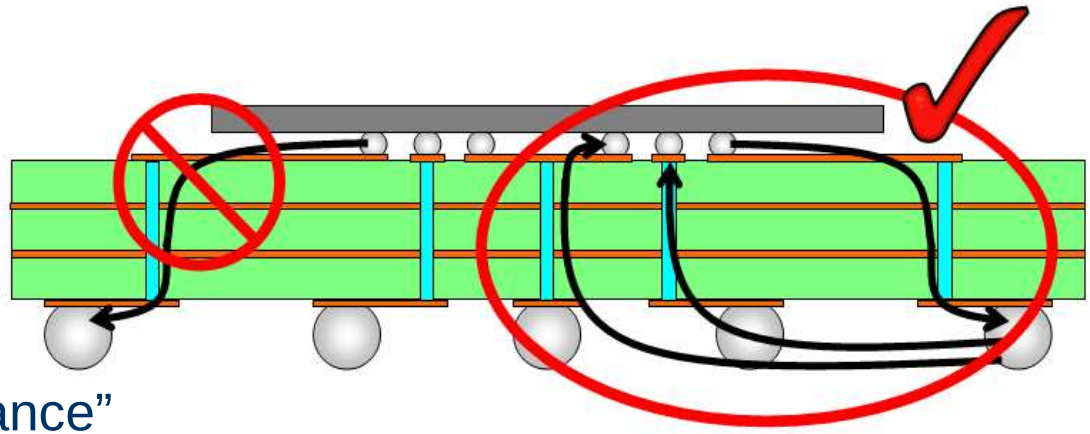
Net	Pin NodeName	R(mOhm)	L(nH)
VCC	Node4004!!P13::VCC	26.4678	1.06165
VSS	Node2391!!E60::VCC	24.833	1.04538
	Node4151!!G26::VCC	25.166	1.01003
	Node3809!!C73::VCC	67.4929	1.00087
	Node2604!!H22::VCC	27.8522	0.986105
	Node3867!!P26::VCC	21.9125	0.962073
	Node3366!!I28::VCC	23.7276	0.954088
	Node4284!!G12::VCC	23.0987	0.950023
	Node3049!!R13::VCC	26.5991	0.948813
	Node3172!!V4::VCC	21.7532	0.943962
	Node2240!!H12::VCC	22.7824	0.881285
	Node3681!!S10::VCC	19.1507	0.867224
	Node3360!!T38::VCC	19.5124	0.865496
	Node3811!!A79::VCC	55.9068	0.855043
	Node4042!!P7::VCC	18.1702	0.845731
	Node3540!!S23::VCC	20.8255	0.839841
	Node3312!!T44::VCC	19.4156	0.824768
	Node2683!!H6::VCC	19.4809	0.82168

Ready Computing completed

To support IC power delivery network design

- IC design teams often ask for an inductance report or specify constraints for package inductance
  - inductance is for each die pin looking into the package
  - all power and ground pins are of concern
  - no return current path is specified

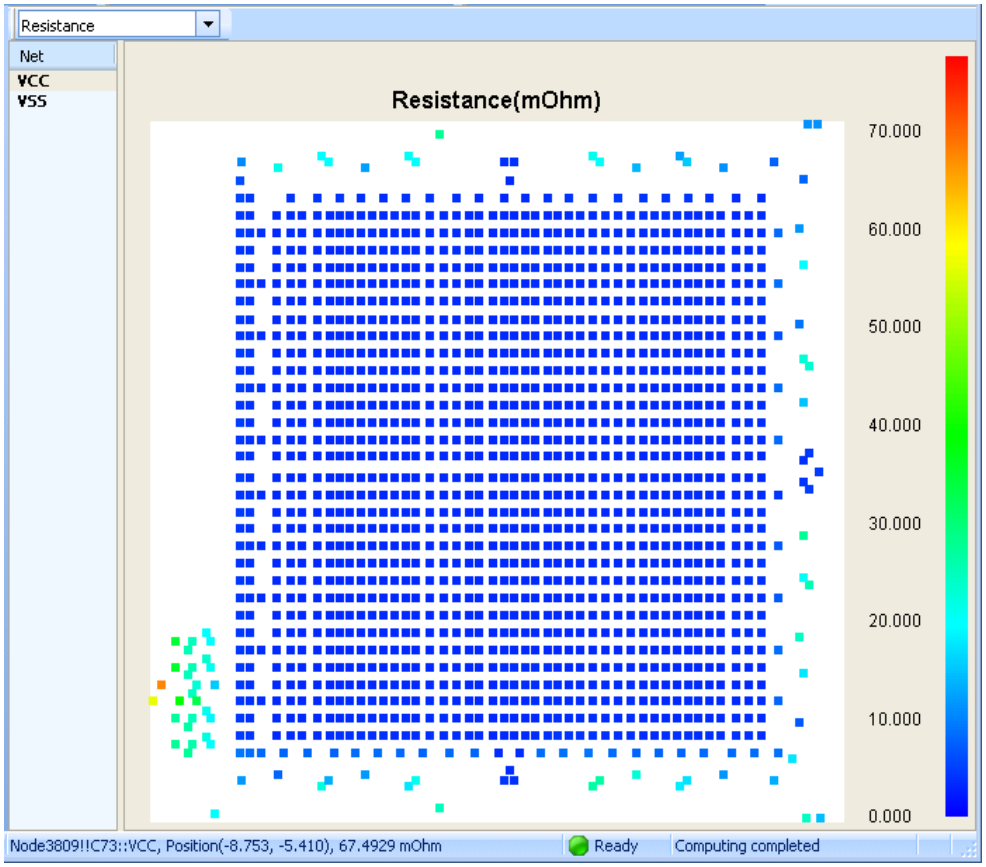
current must flow in loops
the inductance of an isolated current flowing from a die pin to the board is not meaningful and under-estimates real inductive parasitics

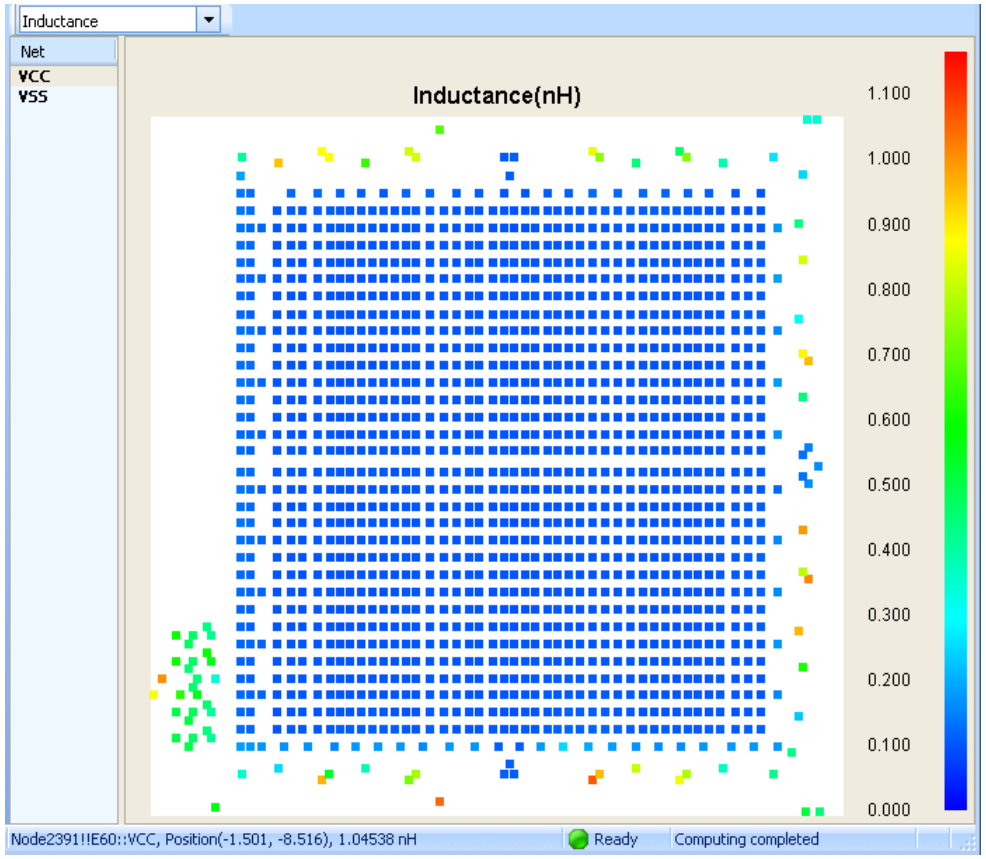


- This request is for “partial inductance”
  - cannot be measured for a package
  - DC EM analysis can compute
    - not defined for AC, full-wave EM analysis cannot compute
  - cannot be applied in isolation (*currents flows in loops – no “partial current*)

Per-pin pwr/gnd assessment

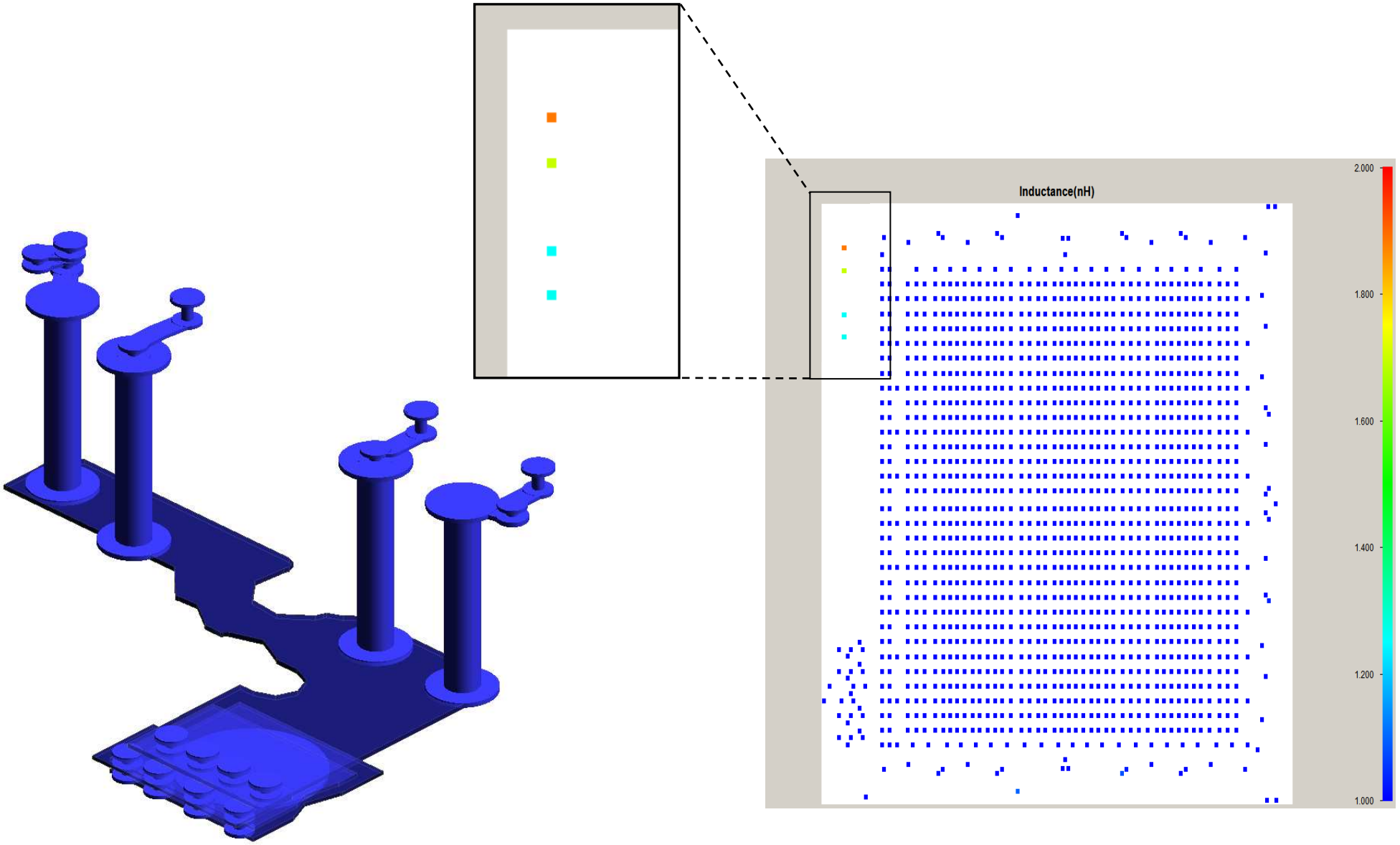
looking into package from die-side





- 2D plots of R and L help to quickly identify “weak” pins looking into the package
  - in this case, looking into the package from the die
- R and L distributions are similar but not identical

Per-pin pwr/gnd assessment

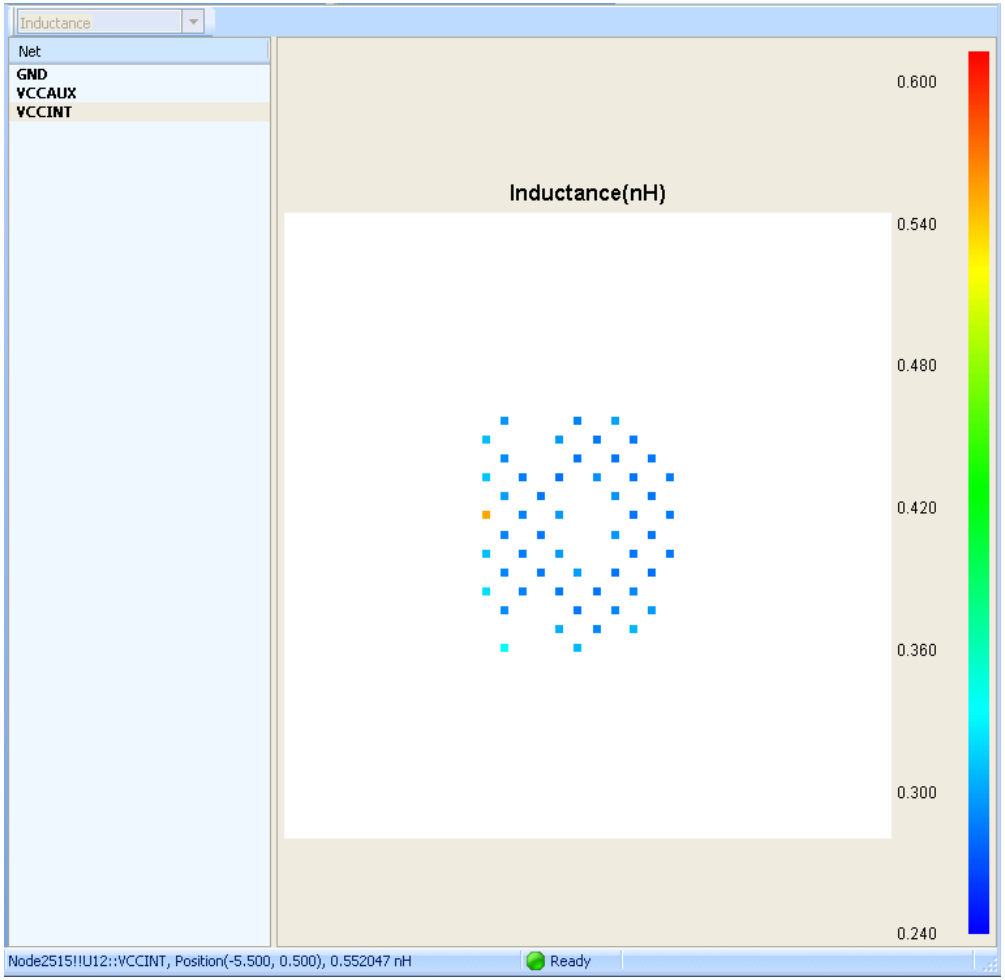


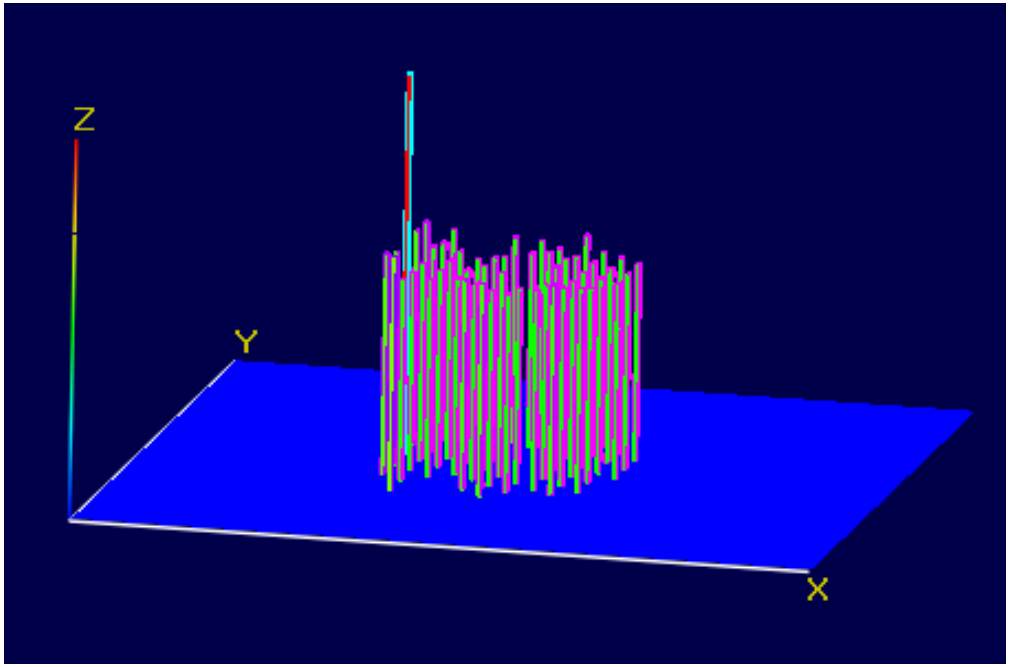
2-to-1 pin inductance variation identified in high speed I/O power net

Per-pin pwr/gnd assessment

another example, board-side core power

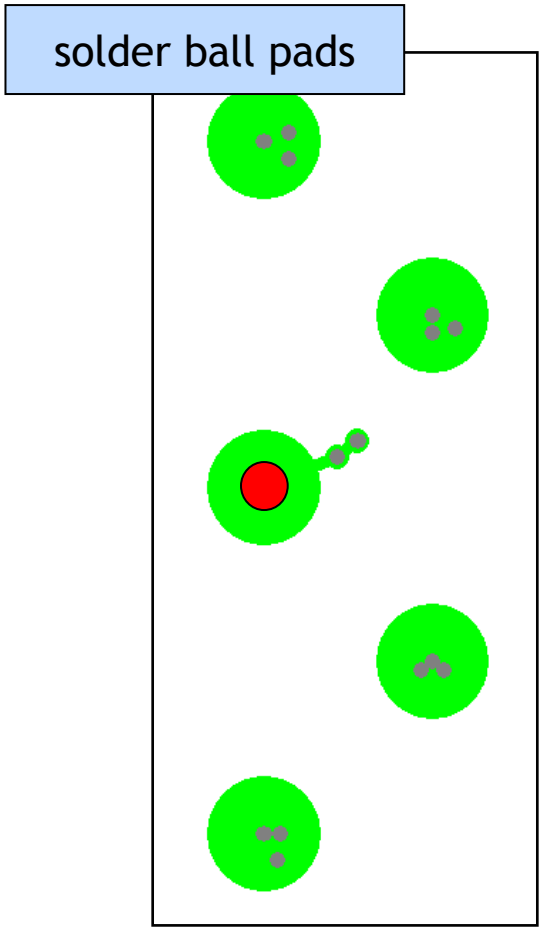
- Board-side loop inductances for core power delivery pins
  - one weak pin is immediately identified with nearly 2X the inductance of other pins

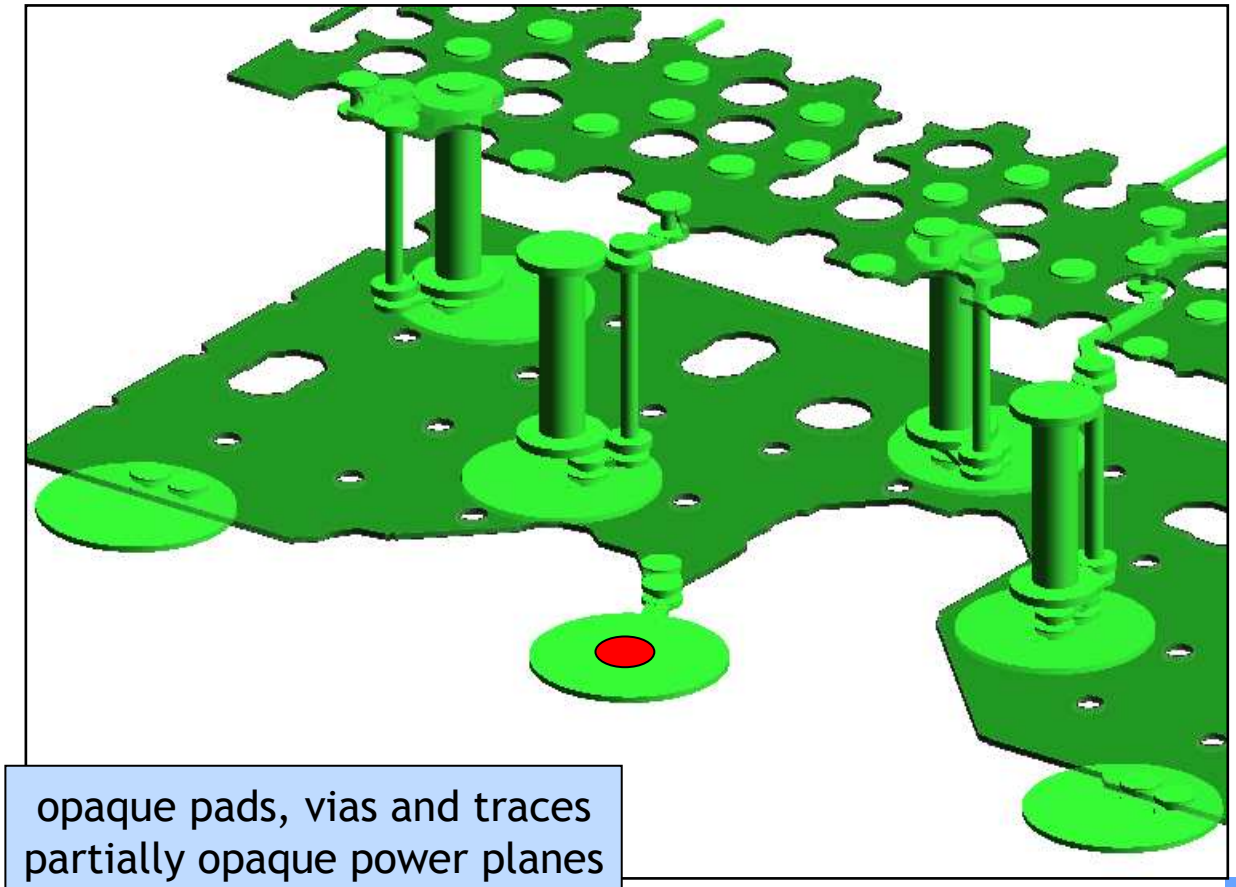




Per-Pin Resistance and Inductance Assessment

- 2D and 3D geometry views help to quickly identify design fixes
  - the ‘weak’ pin is on the plane edge and has a high impedance series interconnect
  - this power pin is more isolated from core vias than other power pins





Hybrid solver trends

- Faster and more memory efficient
  - multi-core and high performance computing support
  - algorithm improvements for both time and frequency domains
- Application to “pre-layout” analysis
  - don’t just tell me how my decap design works, tell me where to put the decaps
- Statistical behaviors
  - variations in manufacturing (spacing, width, thickness, etc)
  - component tolerances and multi-vendor sourcing
- Greater ability to handle local 3D geometries
  - more general built-in component solvers
  - coupling of plane solvers to built-in 3D solvers
  - will enhance high frequency accuracy of whole-package/board analysis
- Leadframe package design flow support and extraction
  - QFP, QFN, Amkor’s “Fusion Quad”
- Tighter integration with chip-level analysis tools
  - static and dynamic power noise and timing analyses
- Expanding support for package “design” tasks and decisions
  - assessment analyses and display
  - more compact yet complete models
- Greater incorporation of emissions on design-side simulation
  - tell me where I need decaps to reduce emissions

2 - System-level analysis for SI and PI

System-level analysis issues

- Model size
- Domain partitioning
- Model connectivity

Model Size

- Broadband, many-port Touchstone data files are large
  - can be several gigabytes for whole-package/board
- Sigrity could not wait for an industry standard to suppor system-level design
  - created a proprietary format “BNP” (broadband network parameters)
  - provide free viewer and API to read (e.g. in HSPICE)
  - incorporates
    - binary storage, reduced order model (e.g. pole/zero), symmetry, etc
- IBIS committee working on standards for similar capabilities
  - Touchstone 2.0 spec now available
  - near-term enhancements
    - sparsity, port naming
  - longer term enhancements
    - binary, pole/zero

Multi-domain analysis
(*package/board as an example*)

1. Characterize individually, combine with SPICE
   - circuit-level connectivity
     - please don't use language of "non-TEM" – it simply is not correct
   - includes "loading" but not "coupling"

2. Merge physical databases together
   - very large analysis, a high price to pay
   - composite stack-up
   - includes all possible coupling/loading effects

- When is a merged analysis required?
  - rarely
  - for potential "RF-type" couplings
  - for example: a high-gain power amplifier
    - -50dB to -60dB isolation required input-to-output
    - multi-layer proximity coupling may be important

The challenge with model connectivity

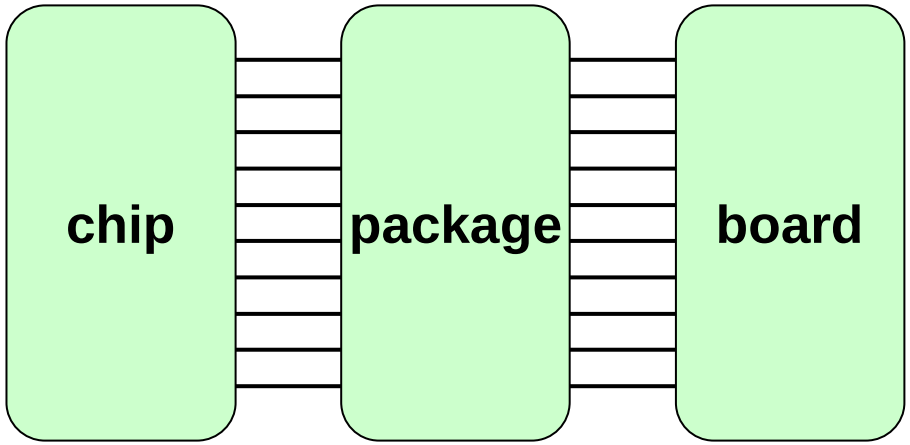
- Assume I have …
  - a chip/package/board system with hundreds or thousands of physical connections (pins)
  - individual electrical models for each chip, package and board
    - I did not generate each of these models myself, therefore I do not have full knowledge of the pin mapping information for each model.

- How do I …
  1. know which pins of one model to connect to the pins of another model?
  2. reliably and in reasonable time connect these models in a netlist or a schematic?

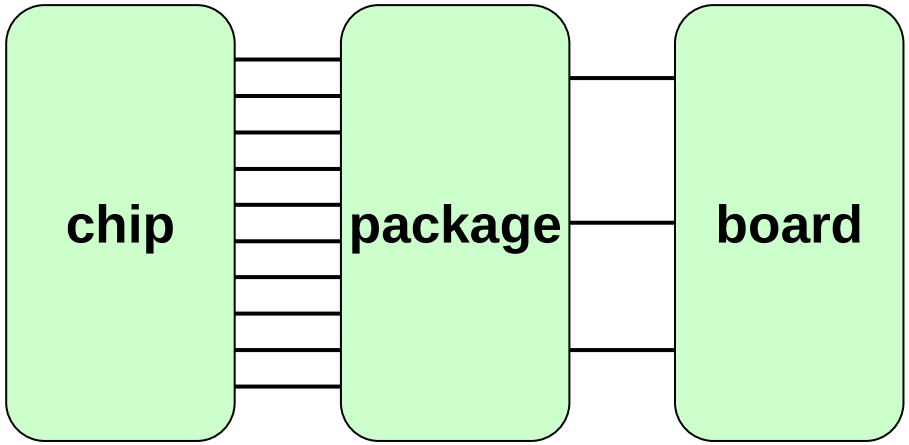
Requirements

- Chip/package/board systems have many physical connections (pins)
  - chip-package boundary ≈ 100 – 5000
  - package-board boundary ≈ 100 – 2000
- Not all electrical models can have pin-level resolution
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools
- Adequate modeling may not be possible with net-level resolution
  - especially, if this low resolution is applied throughout the entire system
  - NOTE: “net-level resolution” groups all pins for each net at a domain boundary
- Support is required for
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools

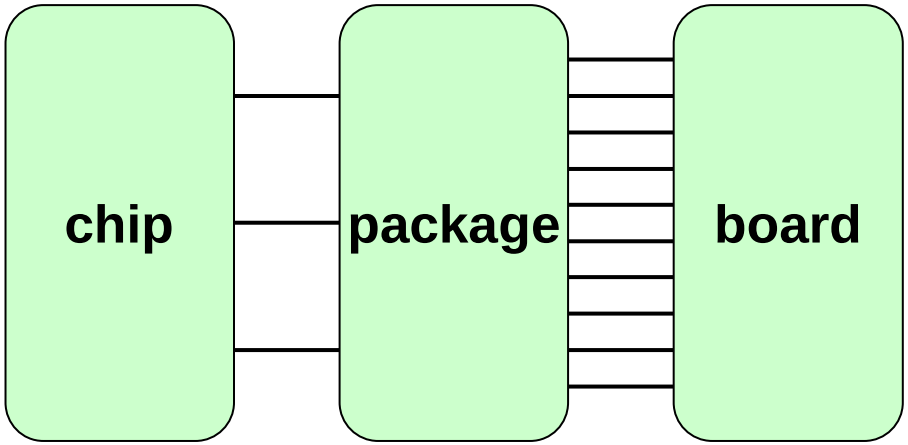
System Analysis



Physical connectivity



Chip-centric model abstraction



Board-centric model abstraction

Existing Model Connection Protocols for Chip/Package/Board Analysis

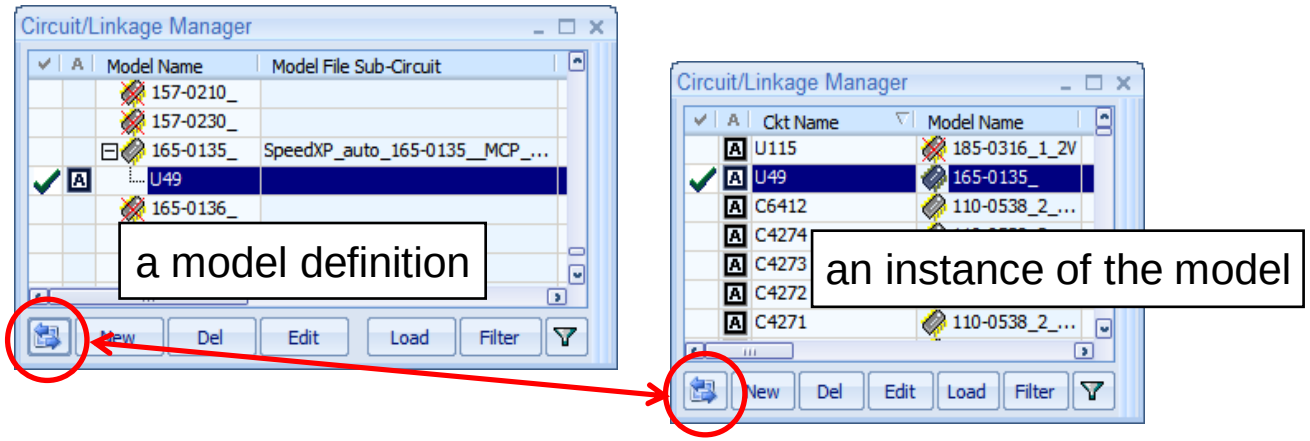
- Sigrity MCP (**M**odel **C**onnection **P**rotocol)
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board system analysis
  - presently Version 1.0
    - 1.1 available soon with user-requested pin locations
- Apache CPP
  - defined by Apache
    - definition covered under NDA

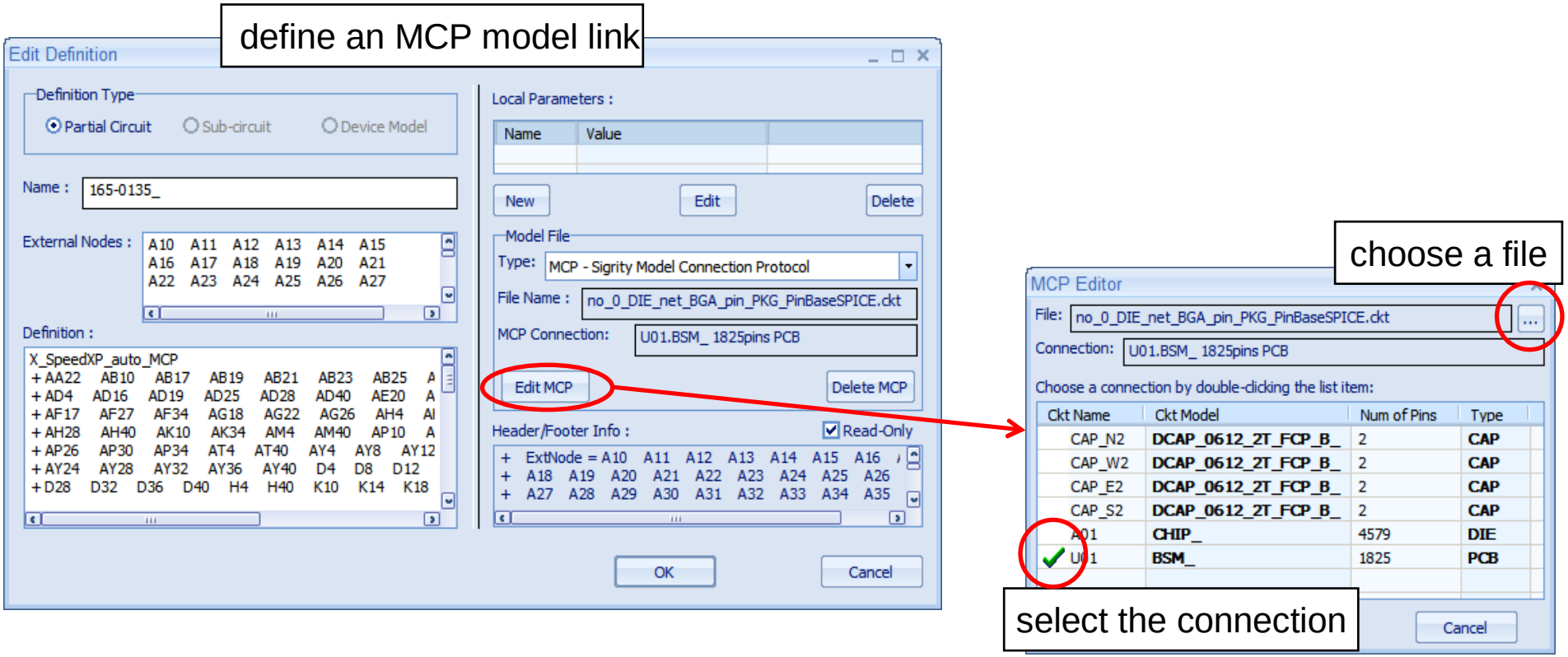
- Implemented as “headers”
- Contained within model-native comment lines
  - model could be either subcircuit or data file

A Typical Model Connection Protocol (Sigrity MCP)

```
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}
* [MCP Source] source text
* [Coordinate Unit] unit
* [Connection] connectionName  partName  numberPhysicalPins
*   [Connection Type] {DIE|PKG|PCB}
*     [Power Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*    [Ground Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*     [Signal Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
* [MCP End]
```

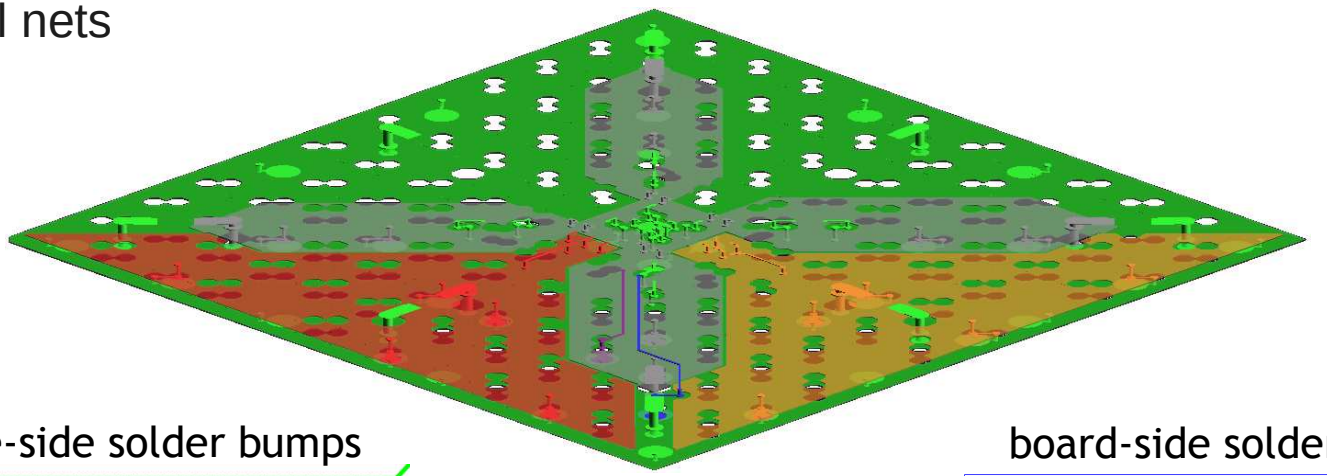
Application of an MCP model by an EDA tool



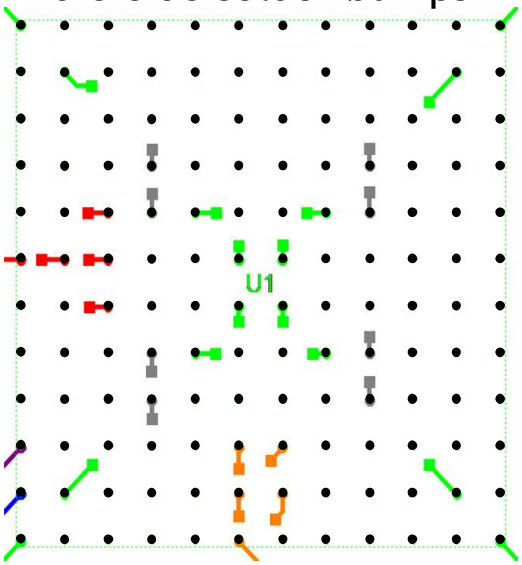


A Physical Example

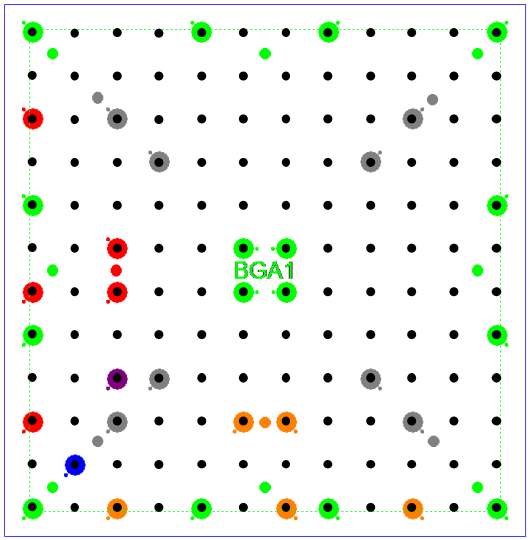
- a few nets in a small 4-layer flipchip BGA package
  (so the MCP sections fin on a single page)
  - 3 power nets
  - 1 ground net
  - 2 signal nets



die-side solder bumps

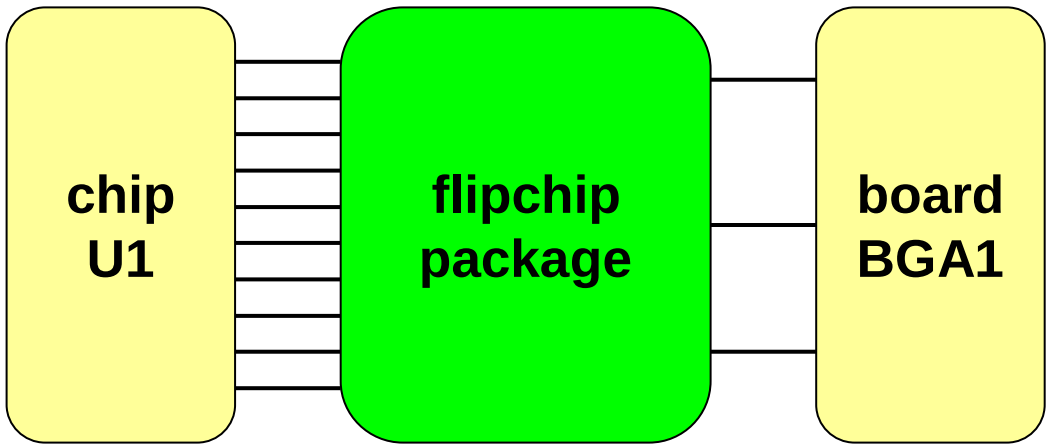


board-side solder balls



Model Resolution

- per-pin connectivity at the chip-package boundary
  - 36 physical pins - 36 electrical nodes
    - 18 power nodes - 5 VDD_1, 5 VDD_4, 8 VDDcore
    - 16 ground nodes - 16 VSS
    - 2 signal nodes - Net_1, Net_2
- per-net connectivity at the package-board boundary
  - 36 physical pins - 6 electrical nodes
    - 3 power nodes - 1 VDD_1, 1 VDD_4, 1 VDDcore
    - 1 ground nodes - 1 VSS
    - 2 signal nodes - Net_1, Net_2



A SPICE circuit with MCP header

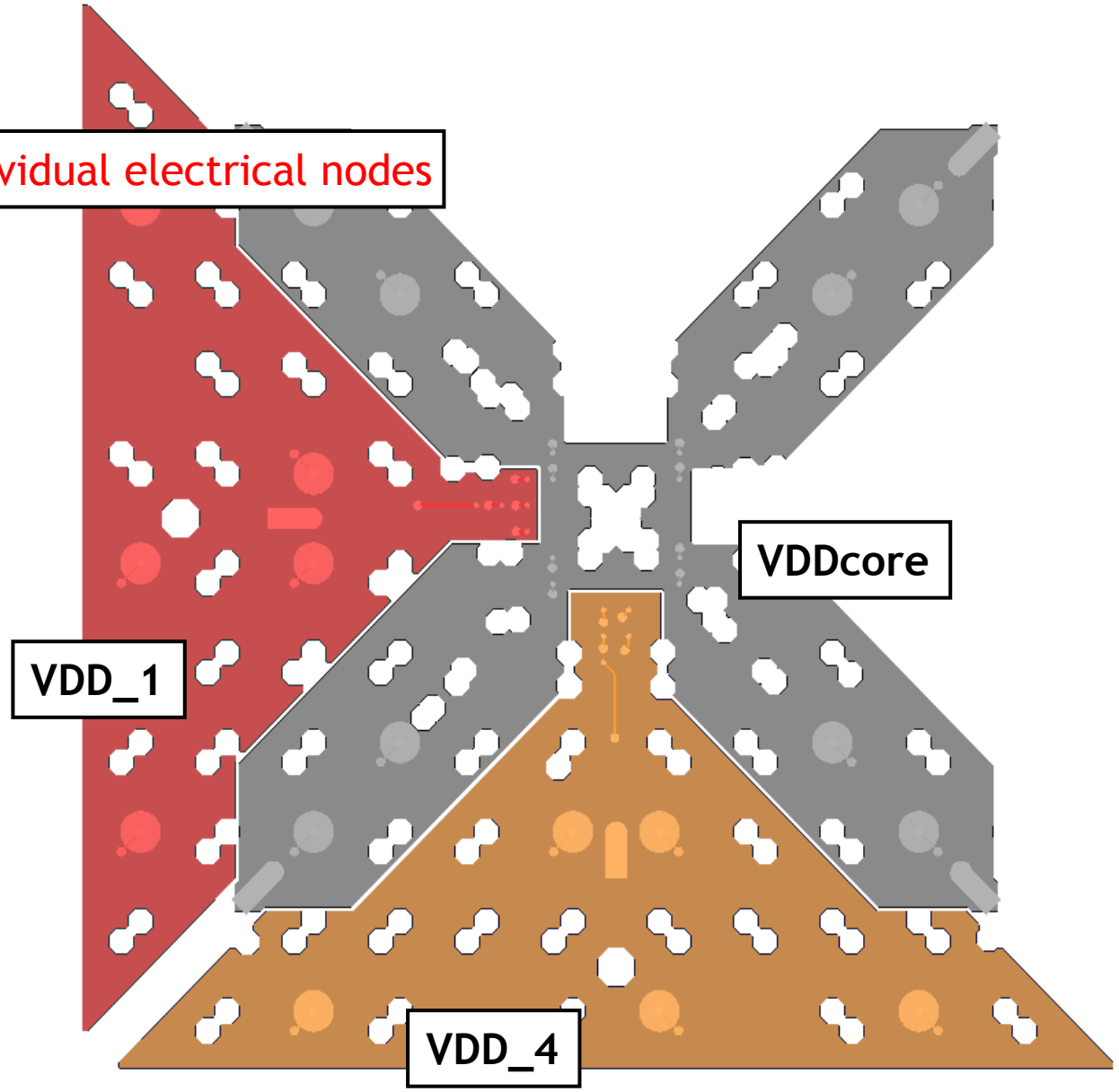
(*a mixed **pin**-level/**net**-level model*)

```
.SUBCKT FlipChip_pkg_SPICE
+  U1_E3  U1_F1   U1_F2   U1_F3   U1_G3
+  U1_K6  U1_K7   U1_L6   U1_L7   U1_M6
+  U1_D4  U1_D9   U1_E4   U1_E9   U1_H4  U1_H9  U1_J4   U1_J9
+  U1_A1  U1_A12  U1_B11  U1_B2   U1_E5  U1_E8  U1_F7   U1_G6
+  U1_G7  U1_H5   U1_H8   U1_L11  U1_L2  U1_M1  U1_M12  U1_F6
+  U1_L1  U1_K1
+  BGA1_C1  BGA1_K6  BGA1_C10  BGA1_A1  BGA1_L2  BGA1_J3
*
* The following is the Sigrity MCP Section
**************************************
*[MCP Begin]
*[MCP Ver] 1.0
*[Structure Type] PKG
*[MCP Source] Sigrity XtractIM 3.0.2.07061 7/18/2009
```

A SPICE circuit with MCP header

(*a pin-level die-side connection*)

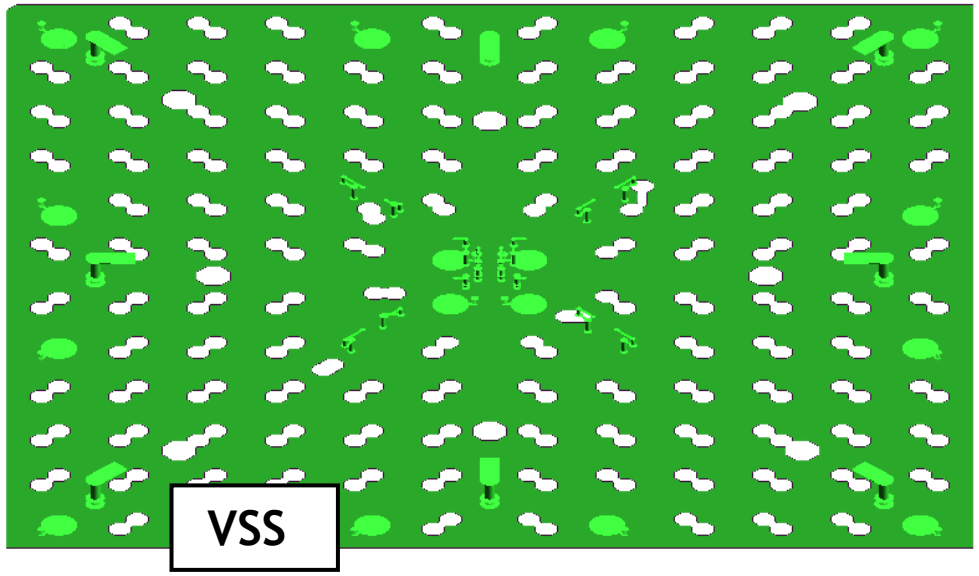
```
*[Connection] U1 die_12x12 144
*[Connection Type] DIE
*[Power Nets]
* E3    U1_E3    VDD_1
* F1    U1_F1    VDD_1
* F2    U1_F2    VDD_1
* F3    U1_F3    VDD_1
* G3    U1_G3    VDD_1
* K6    U1_K6    VDD_4
* K7    U1_K7    VDD_4
* L6    U1_L6    VDD_4
* L7    U1_L7    VDD_4
* M6    U1_M6    VDD_4
* D4    U1_D4    VDDcore
* D9    U1_D9    VDDcore
* E4    U1_E4    VDDcore
* E9    U1_E9    VDDcore
* H4    U1_H4    VDDcore
* H9    U1_H9    VDDcore
* J4    U1_J4    VDDcore
* J9    U1_J9    VDDcore
```

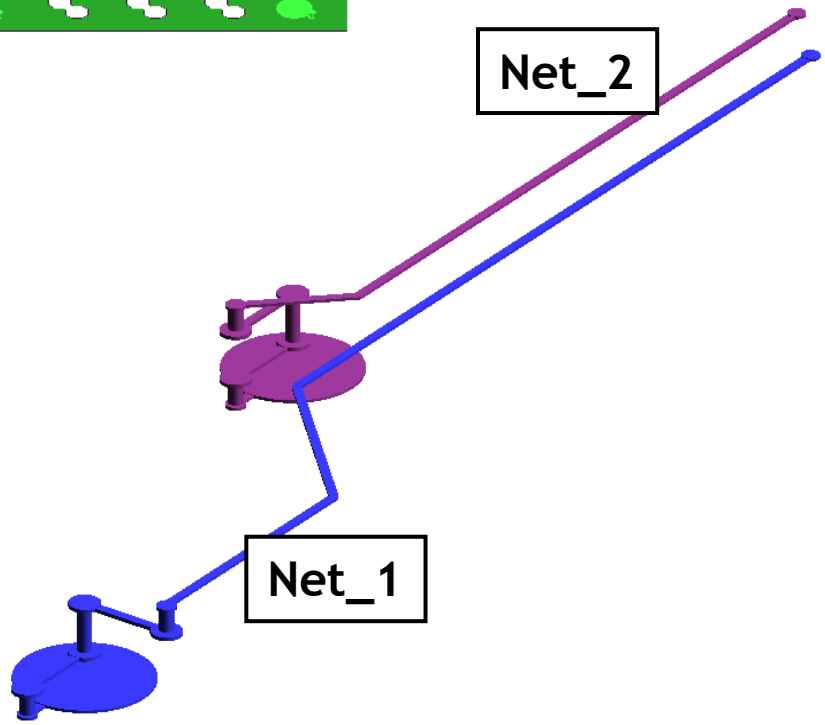


A SPICE circuit with MCP header

(*a pin-level die-side connection*)

```
*[Ground Nets]
* A1    U1_A1    VSS
* A12   U1_A12   VSS
* B11   U1_B11   VSS
* B2    U1_B2    VSS
* E5    U1_E5    VSS
* E8    U1_E8    VSS
* F7    U1_F7    VSS
* G6    U1_G6    VSS
* G7    U1_G7    VSS
* H5    U1_H5    VSS
* H8    U1_H8    VSS
* L11   U1_L11   VSS
* L2    U1_L2    VSS
* M1    U1_M1    VSS
* M12   U1_M12   VSS
* F6    U1_F6    VSS
*[Signal Nets]
* L1    U1_L1    Net_1
* K1    U1_K1    Net_2
```

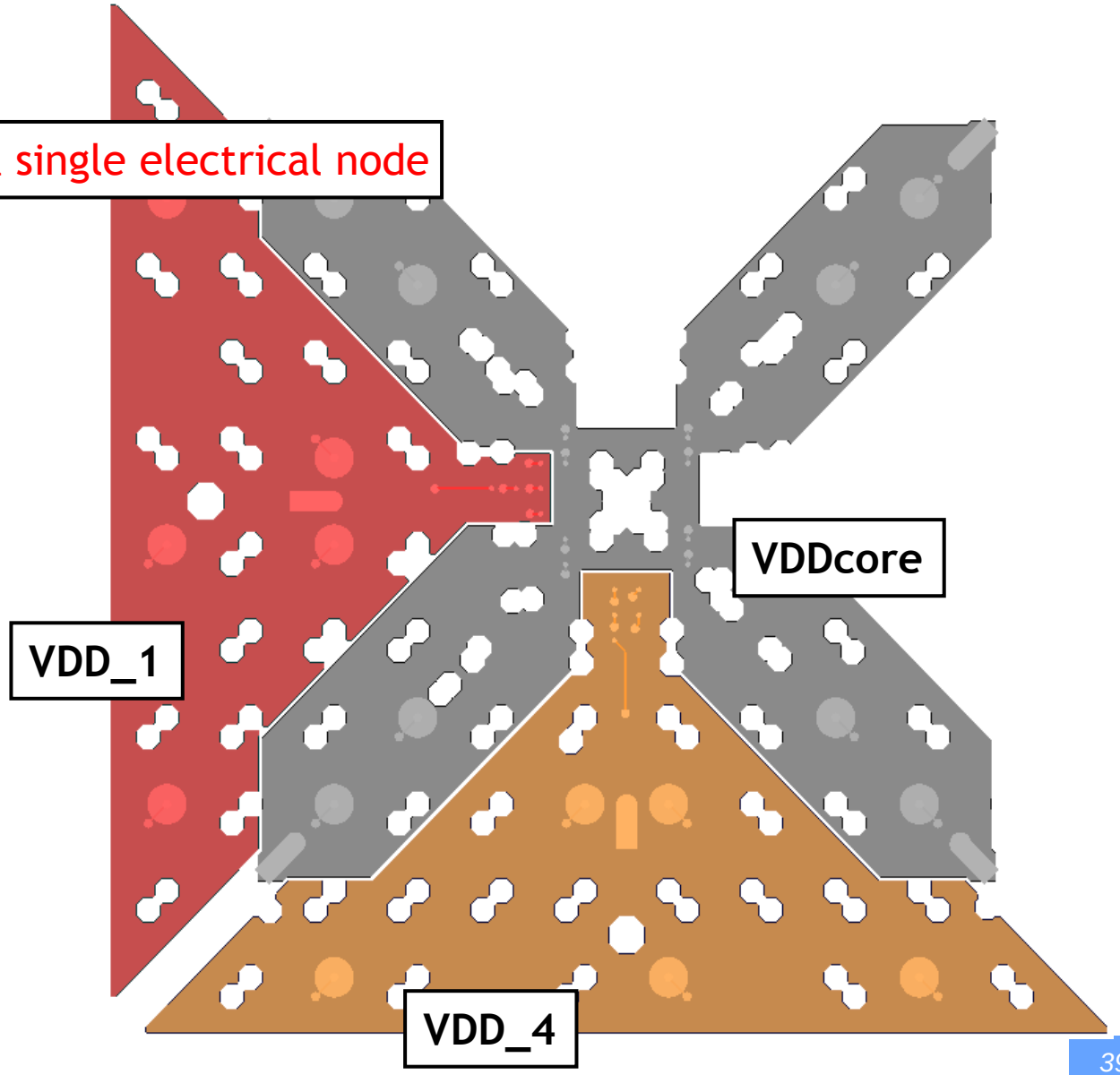




A SPICE circuit with MCP header

(*a net-base pcb-side connection*)

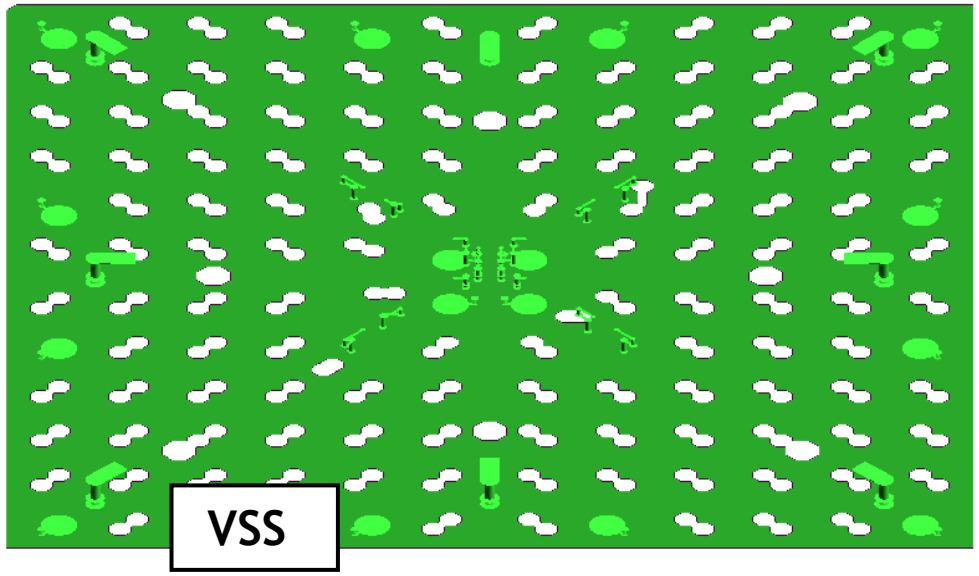
```
*[Connection] BGA1 board_12x12 144
*[Connection Type] PCB
*[Power Nets]
* C1   BGA1_C1    VDD_1
* F3   BGA1_C1    VDD_1
* G1   BGA1_C1    VDD_1
* G3   BGA1_C1    VDD_1
* K1   BGA1_C1    VDD_1
* K6   BGA1_K6    VDD_4
* K7   BGA1_K6    VDD_4
* M10  BGA1_K6    VDD_4
* M3   BGA1_K6    VDD_4
* M7   BGA1_K6    VDD_4
* C10  BGA1_C10   VDDcore
* C3   BGA1_C10   VDDcore
* D4   BGA1_C10   VDDcore
* D9   BGA1_C10   VDDcore
* J4   BGA1_C10   VDDcore
* J9   BGA1_C10   VDDcore
* K10  BGA1_C10   VDDcore
* K3   BGA1_C10   VDDcore
```

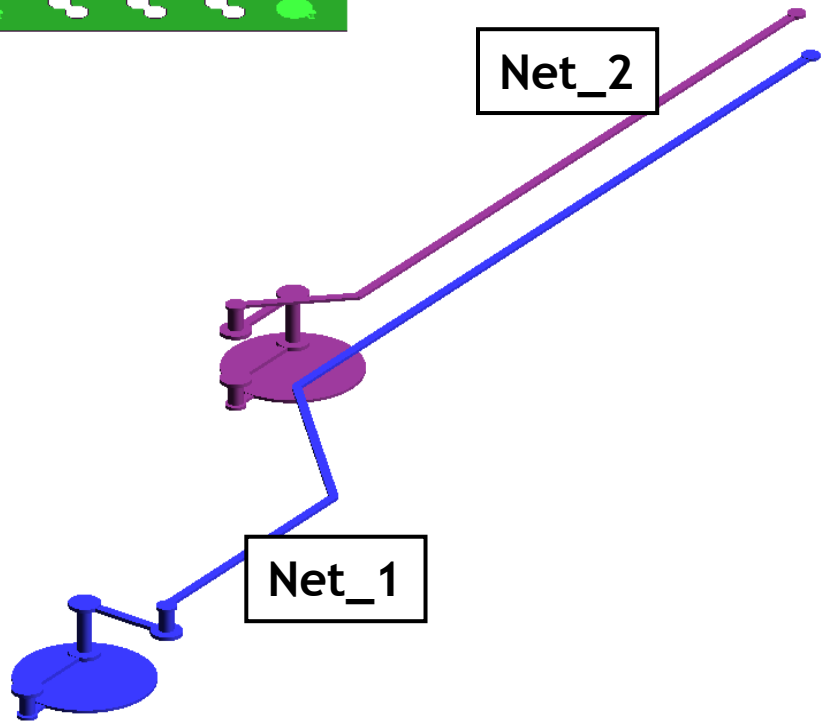


A SPICE circuit with MCP header

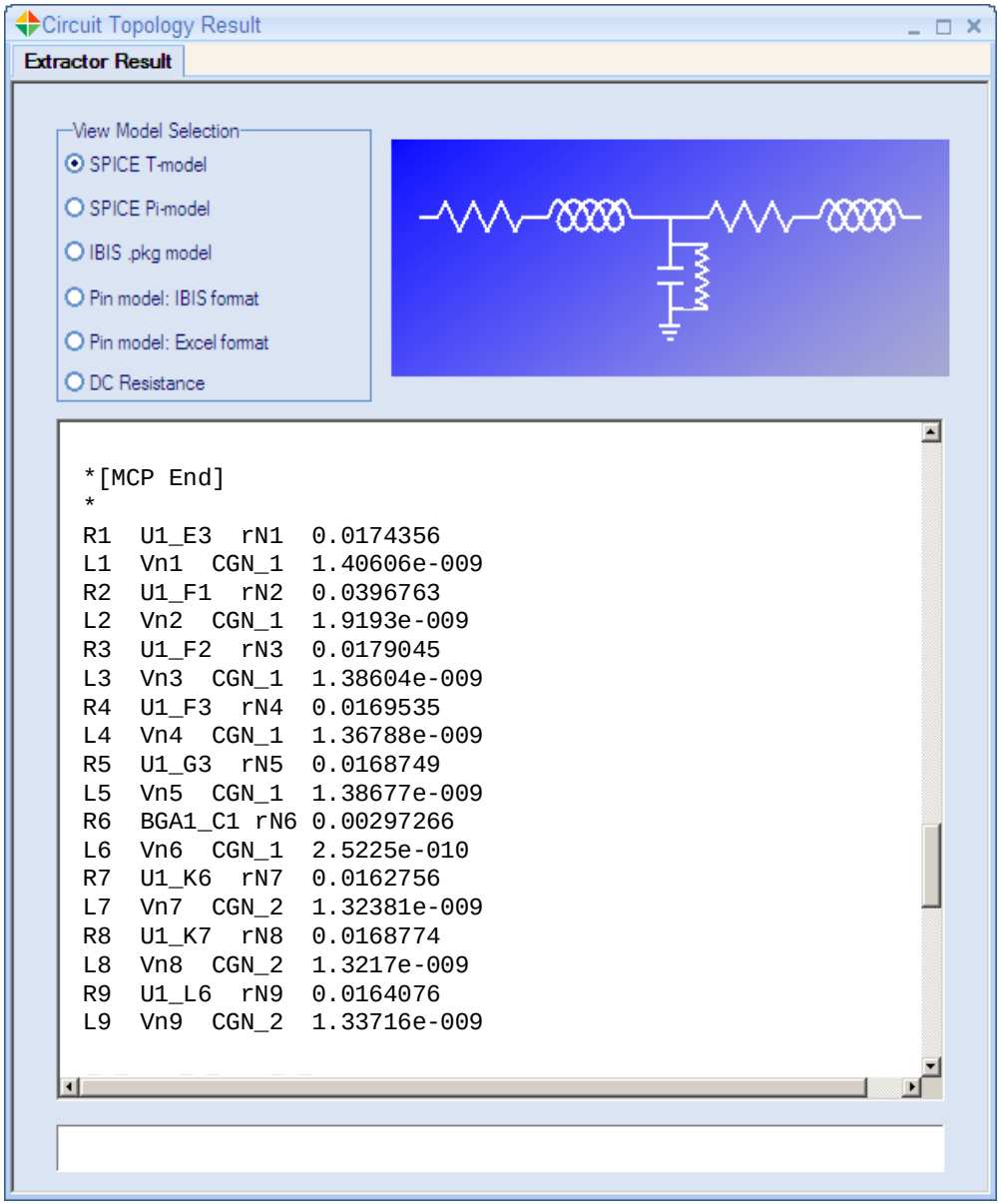
(a net-level pcb-side connection)

```
*[Ground Nets]
* A1    BGA1_A1    VSS
* A12   BGA1_A1    VSS
* A5    BGA1_A1    VSS
* A8    BGA1_A1    VSS
* E1    BGA1_A1    VSS
* E12   BGA1_A1    VSS
* F6    BGA1_A1    VSS
* F7    BGA1_A1    VSS
* G6    BGA1_A1    VSS
* G7    BGA1_A1    VSS
* H1    BGA1_A1    VSS
* H12   BGA1_A1    VSS
* M1    BGA1_A1    VSS
* M12   BGA1_A1    VSS
* M5    BGA1_A1    VSS
* M8    BGA1_A1    VSS
*[Signal Nets]
* L2    BGA1_L2    Net_1
* J3    BGA1_J3    Net_2
*
*[MCP End]
```





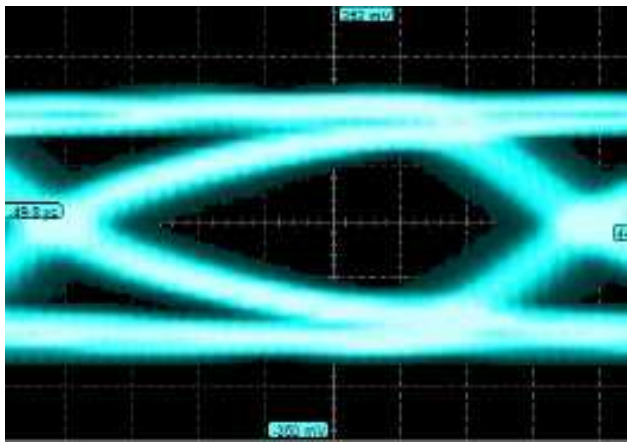
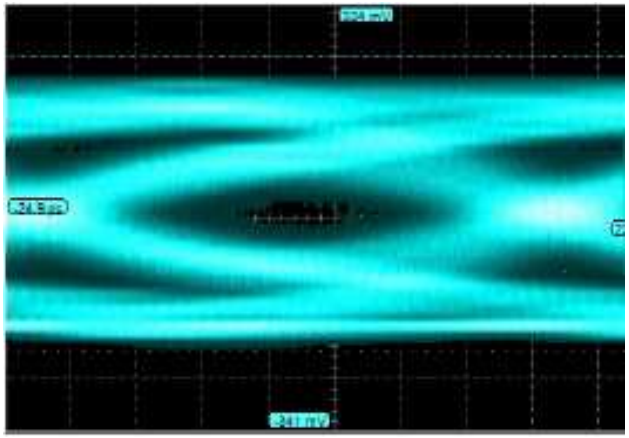
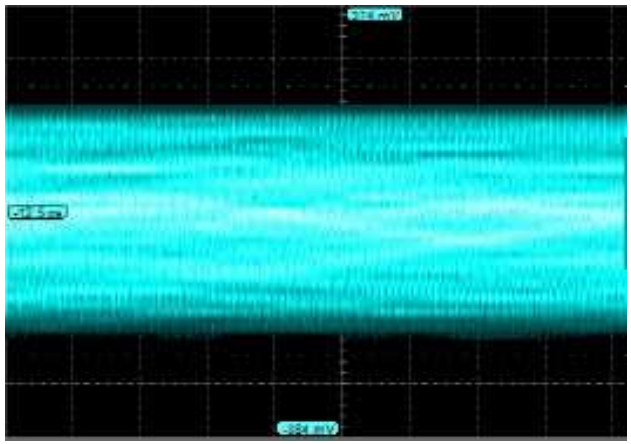
A SPICE circuit with MCP header



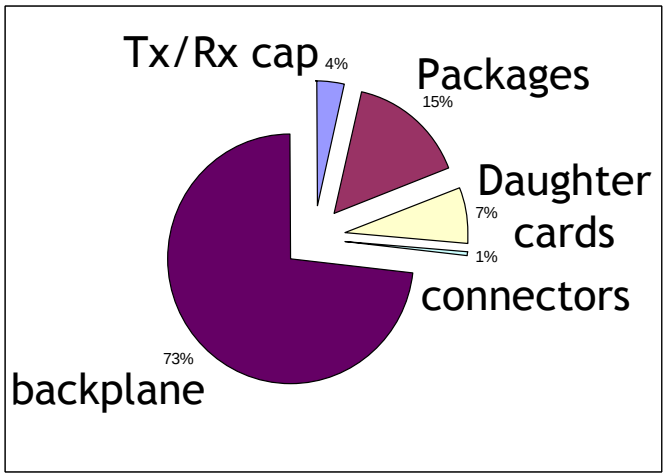
3 - High-speed serial channel design

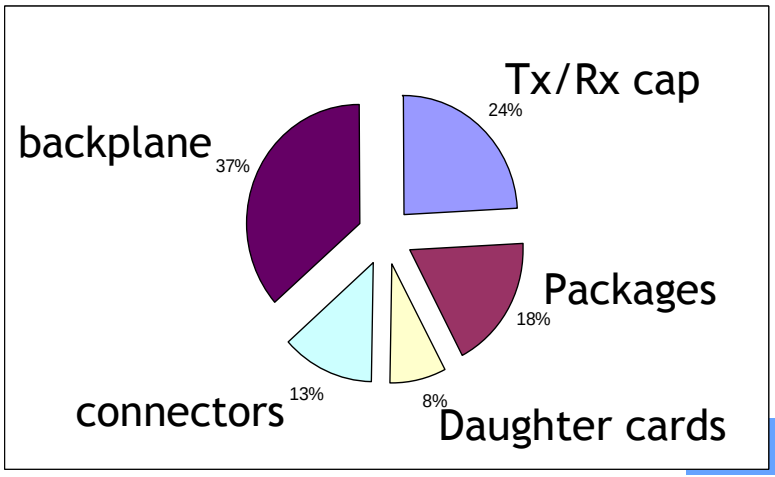
Challenges for Serial Link Design

- Bit Error Rate (BER), Inter-symbol Interference (ISI), Jitter
- Crosstalk, Reflections, Loss, Dispersion

Increasing bit rate

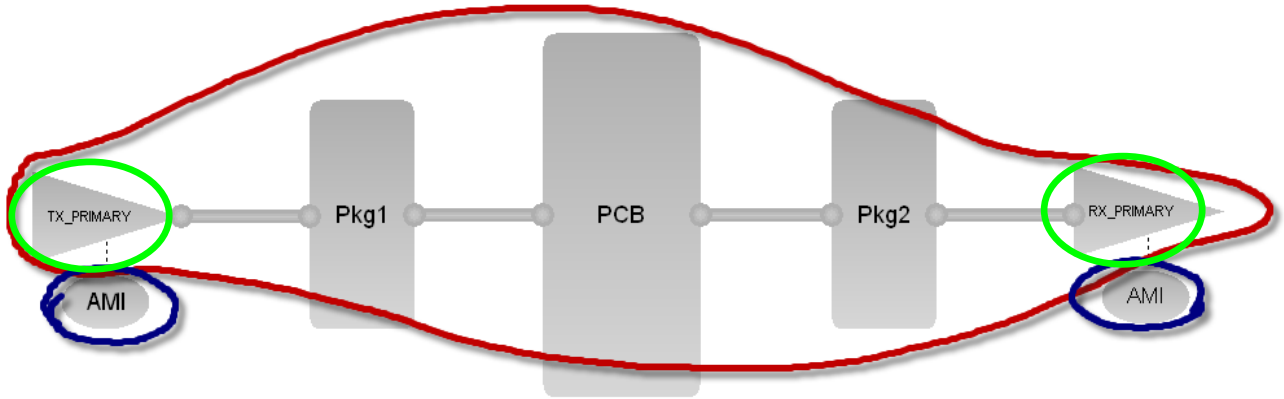




IBIS AMI concept
(Algorithmic Modeling Interface)

- The Tx –to– Rx pathway is composed of 3 separate entities
  - Tx algorithmic part
  - Analog channel
  - Rx algorithmic part

Three "decoupled" parts can be *independently* solved in time domain



- Executable model delivered as a dynamically linked library (DLL)
  - Data flow between these three parts is addressed by a standardized API
  - Robust and flexible parameter passing to Tx & Rx

IBIS AMI
What it *does* and *does not* do

- Does
  - How and what data is interchanged between EDA tool and IC AMI model
  - Pass the user settable parameters to the AMI model

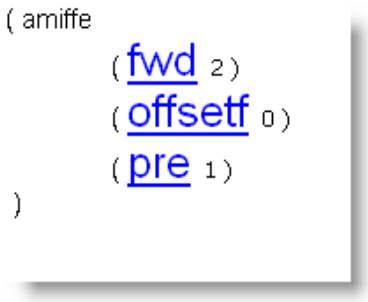
- Does not
  - Prescribe how the device must be modeled
  - State and limit the parameters which can be passed
  - Specify how the EDA tool should perform the simulation
    - simulator agnostic
  - Stipulate how eye diagram, Bit Error Rates must be computed

Channel design requirements

- Analysis Capability
  - Flexible design space exploration:
    - AMI models, Jitter/Noise parameters, System components
  - Techniques for crosstalk and jitter modeling
  - Transient simulation of S-parameters for channel characterization
  - User definable data coding
  - Account for real power supply effects
- Workflow
  - Block wise schematic editor
    - automated model connectivity
  - Access, extraction and viewing of single-ended and mixed-mode S-parameters for the whole channel or any part of it
    - layout-based package and board models
  - AMI and design templates

Investigate design alternatives

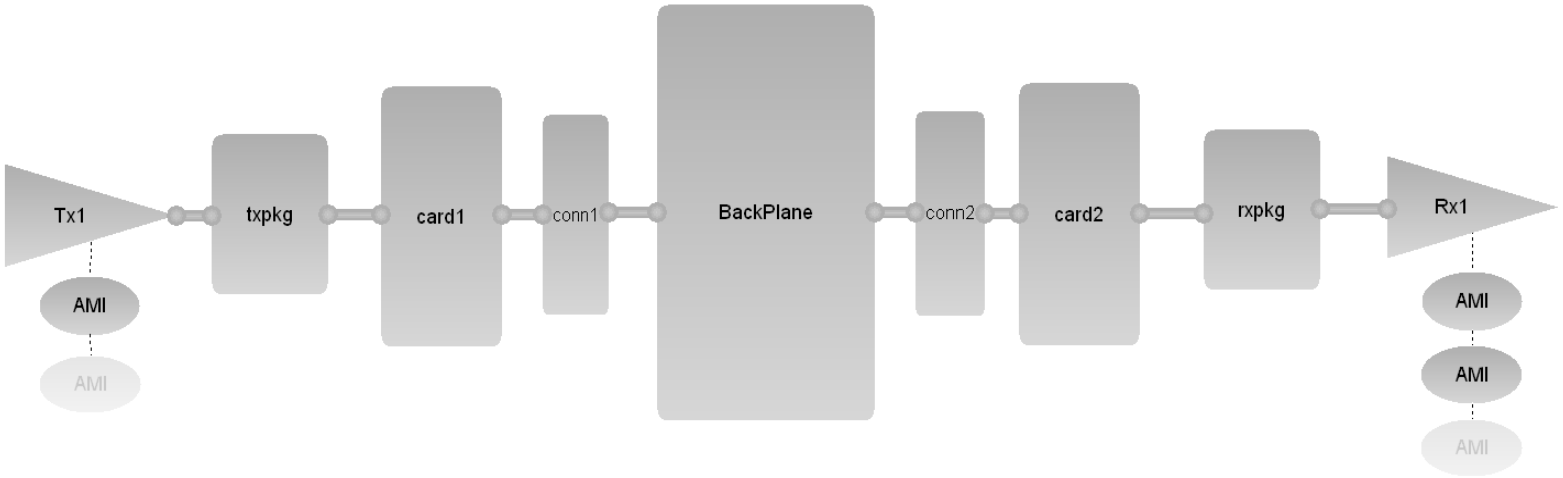
- Quick what-if type analysis by changing
  - Jitter/Noise settings
  - Equalization parameters
  - Various channel component models: connectors, cables, packages, boards, …etc
  - Subcircuit parameters such as die cap, R_{term}, and Tx drive level

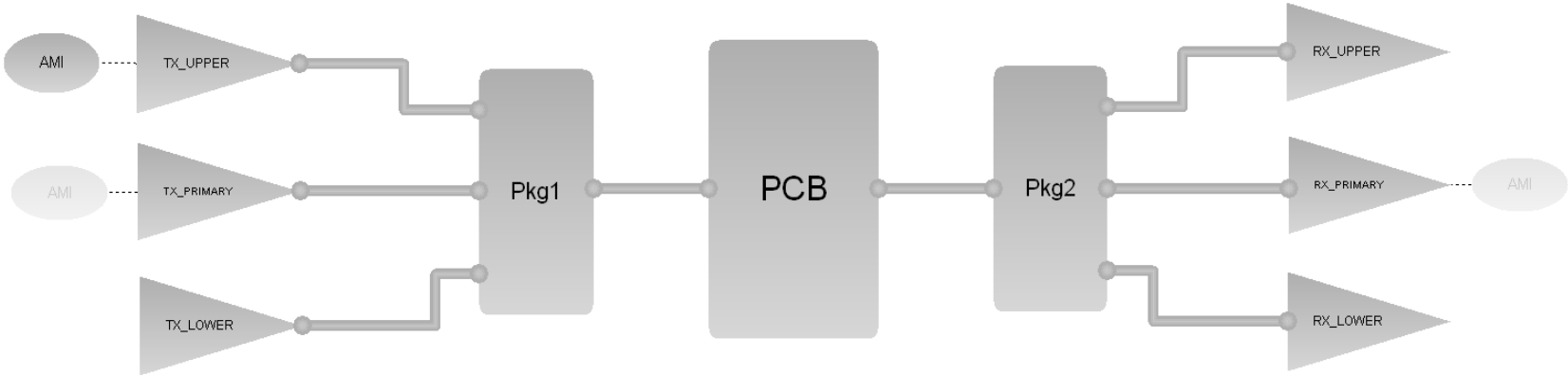


Parameter	Value	Circuit File	Line
nmos_imp	25	C:\Sigrity_Fil...	1
tx_rt	50	C:\Sigrity_Fil...	1
tx_c_comp	1p	C:\Sigrity_Fil...	1
tx_scale	1	C:\Sigrity_Fil...	1

Property	Value
Number of Bits	100000
Bit Sampling Rate	32
Random Jitter (Rj) (%)	0.88
Deterministic Jitter (Dj) (%)	0
Random Noise (Rn) (mV)	1
Deterministic Noise (Dn) (mV)	0
Data Rate (Gbps)	10
Delay (ns)	0
Periodic Jitter Frequency (Hz)	1.0238e+008
Periodic Jitter Amplitude (UI)	0.043
Periodic Noise Frequency (Hz)	60
Periodic Noise Amplitude (mV)	5
Transition Jitter (%)	0
Transition Noise (mV)	0.1
DCD (%)	0.67

Isolated or coupled channels

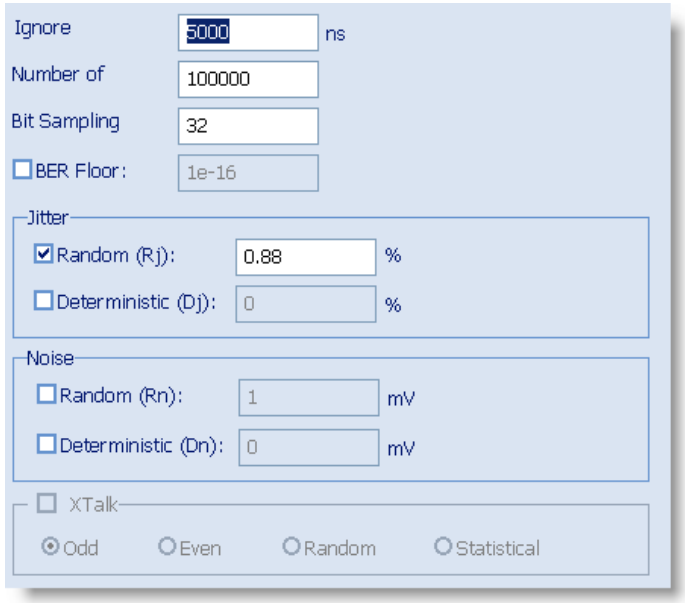


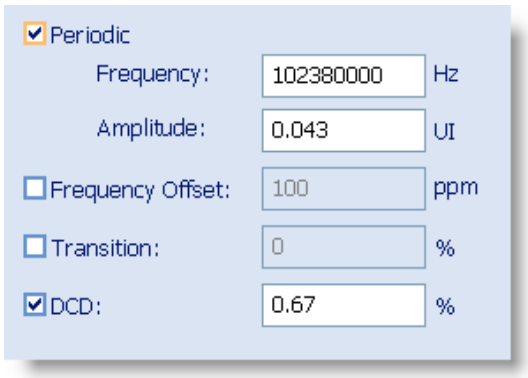


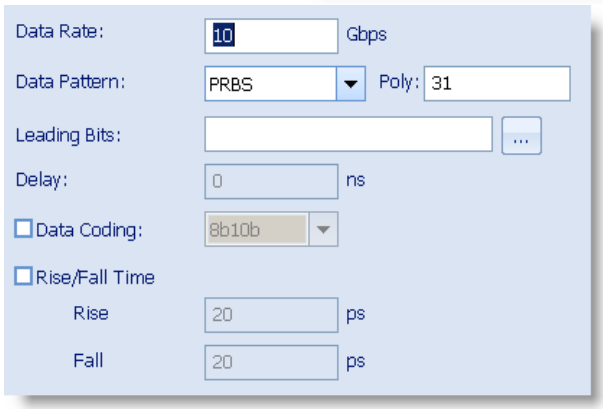
* Time Domain simulation of crosstalk
* Crosstalk Tx model can be different
* Crosstalk Tx can have different data rates and pattern
* Even, odd, random and statistical crosstalk modes

Comprehensive jitter/noise inputs

- Random jitter/noise
- Transition jitter/noise
- Periodic jitter/noise
- Frequency offset
- Duty Cycle Distortion (DCD)

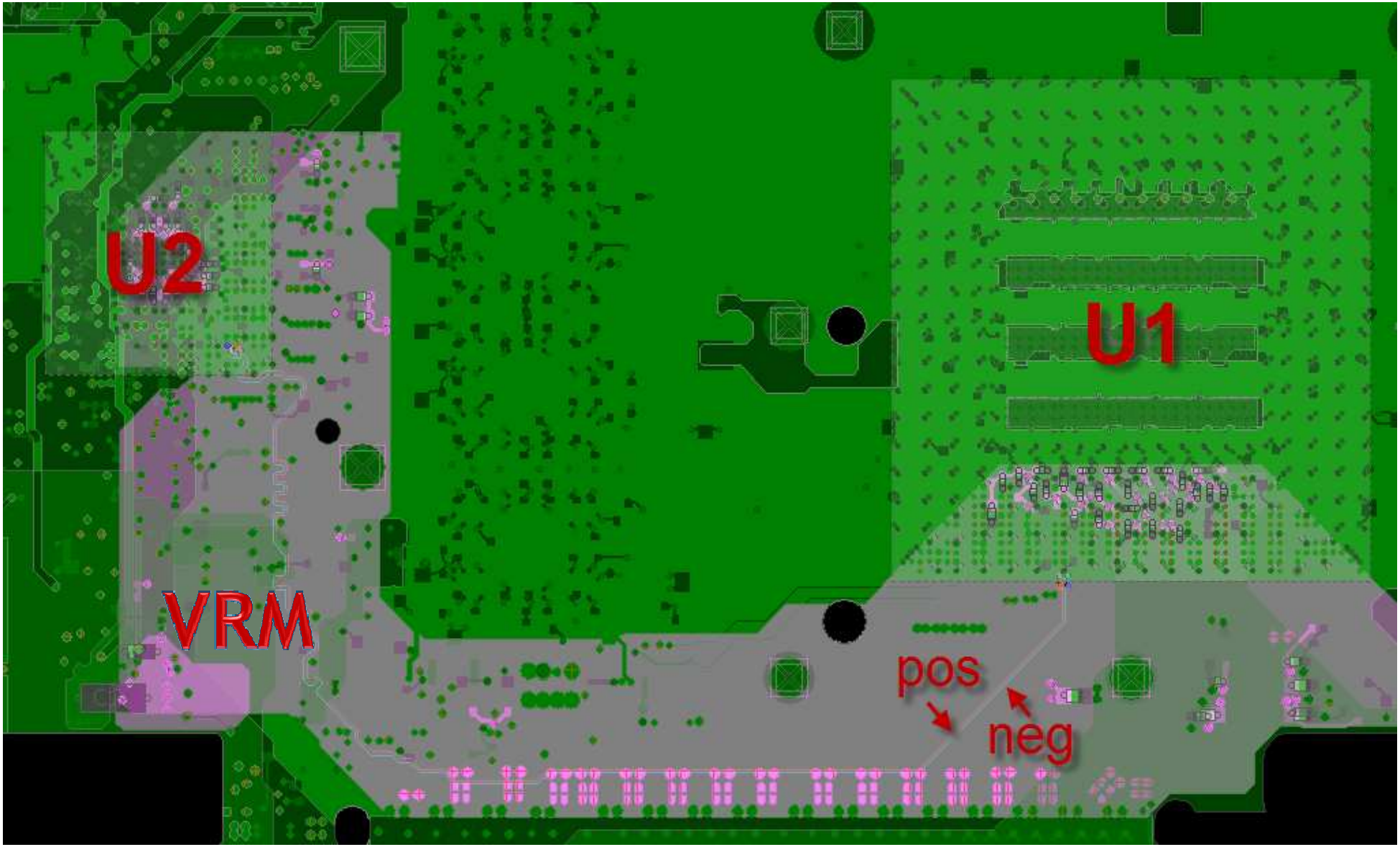






Jitter/Noise at Rx (post processing) and at Tx input (time domain simulation)

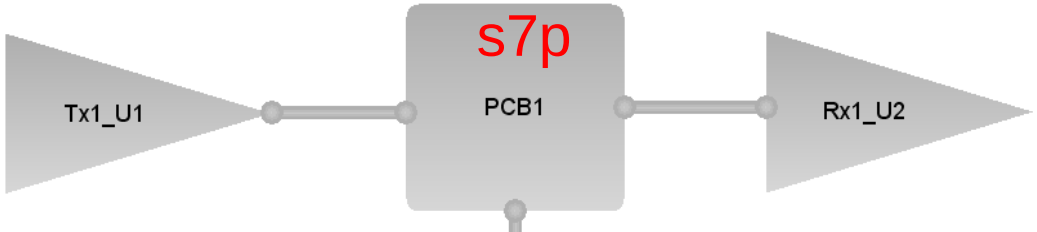
A serial link layout



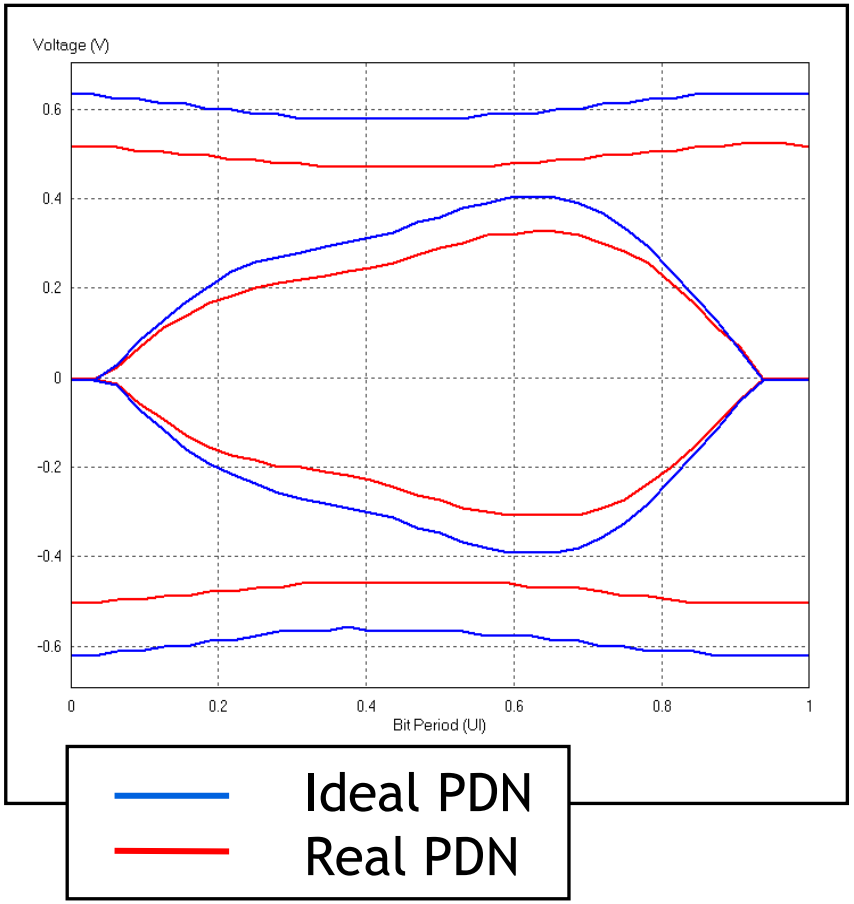
Setup of ideal/real PDN

Ideal PDN

5Gbps
100,000 bits
Random pattern

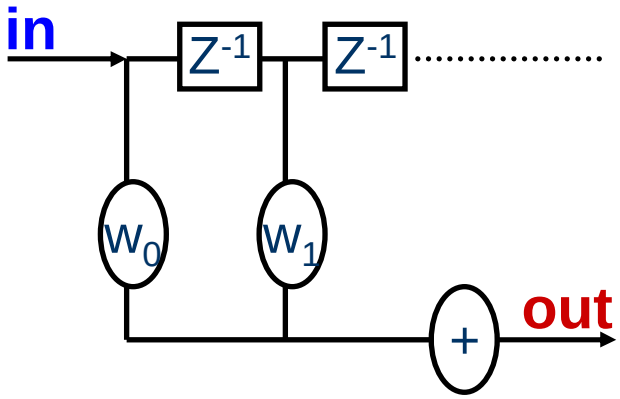


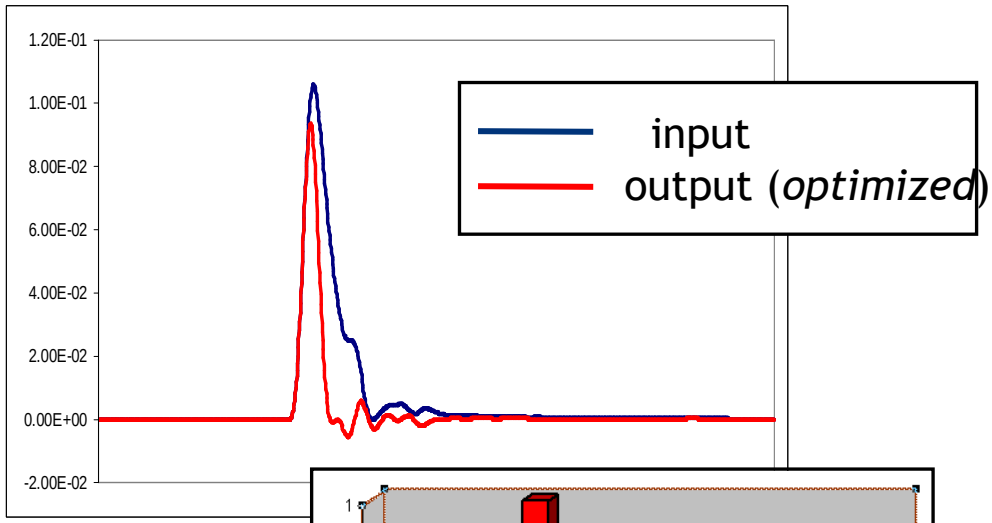
Real PDN

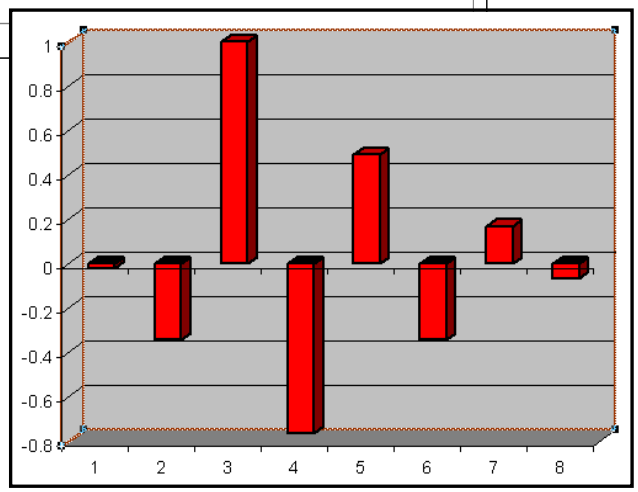


An FFE AMI template

- Feed Forward Filter can be deployed at Tx or Rx
- Can be cascaded with stand alone CDR
- Unlimited number of taps and pre taps
- The set of weighting factors w_i are called *tap coefficients*
- The tap coefficients are automatically optimized.
- The optimization maximizes signal to interference ratio (SIR)

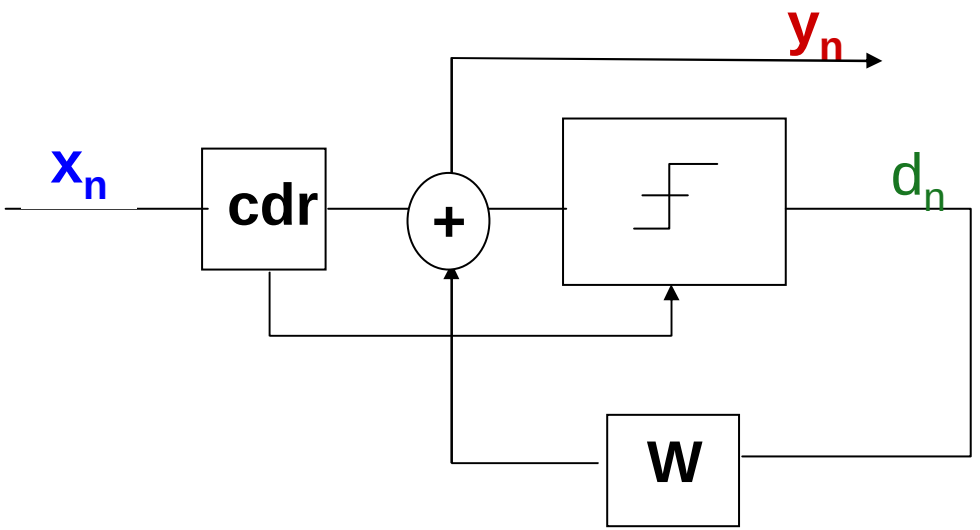






A DFE AMI template

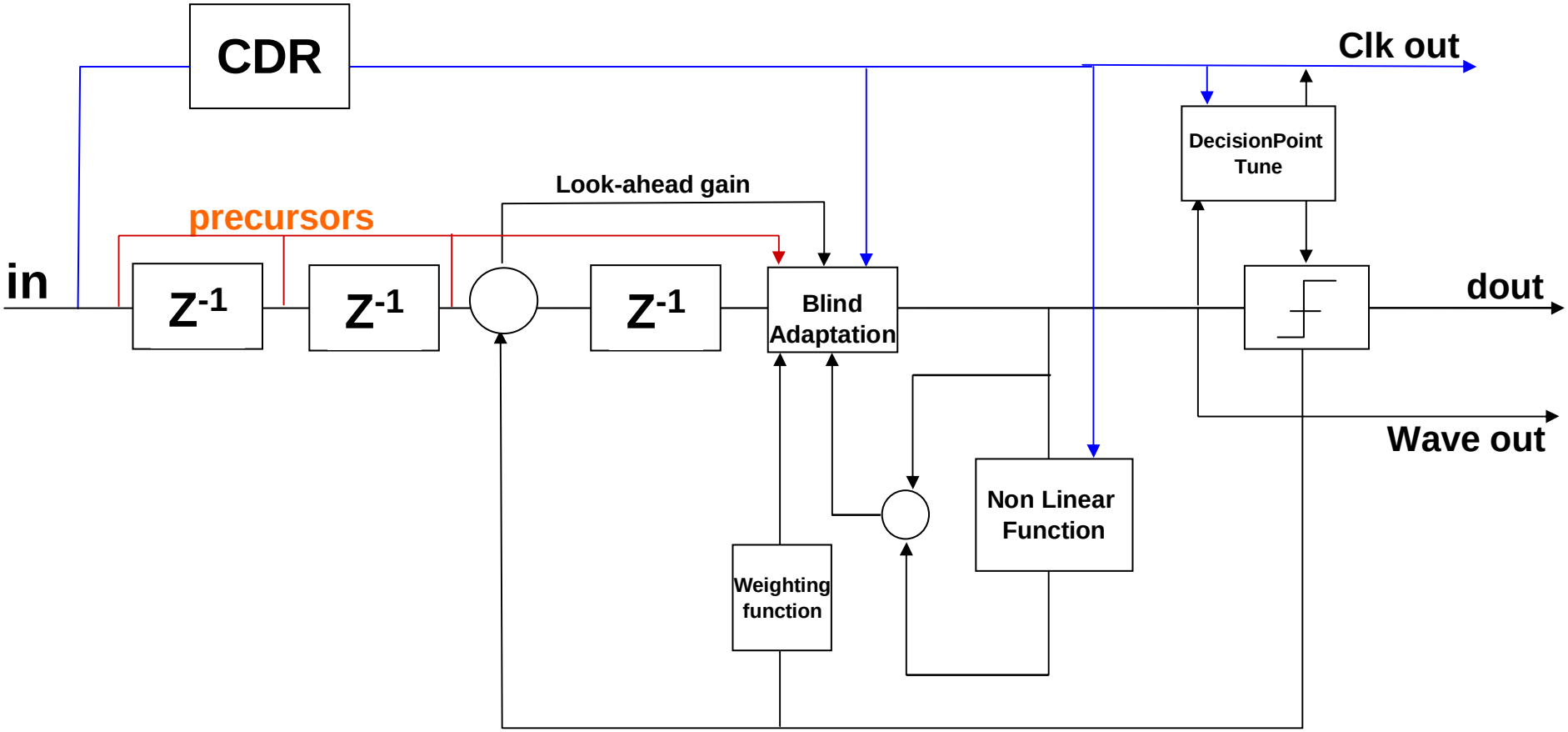
- DFE stands for Decision Feedback Equalizer
- Removes ISI by adding corrections to the input based on previous decisions
- Unlimited number of taps
- The tap coefficients are optimized dynamically (blind adaptation)
- DFE has an integrated CDR
- This DFE can be cascaded with FFE for precursor ISI cancellation



$y_n = x_n + \Sigma\, w_i * d_i$

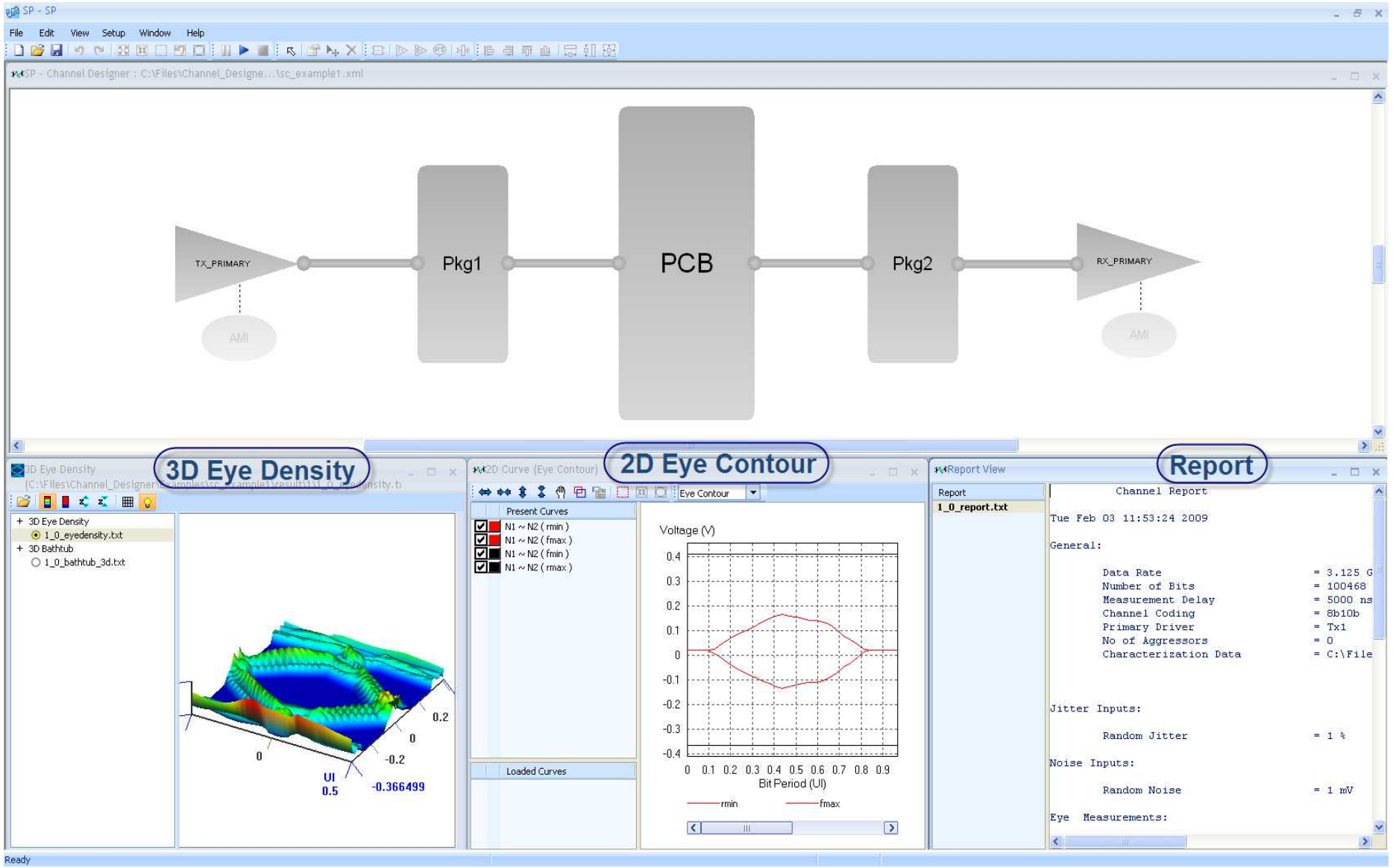
y_n - output
x_n - input
d_i - previous 'i_{th}' decision
w_i - i_{th} tap weight

A look-ahead equalizer AMI template



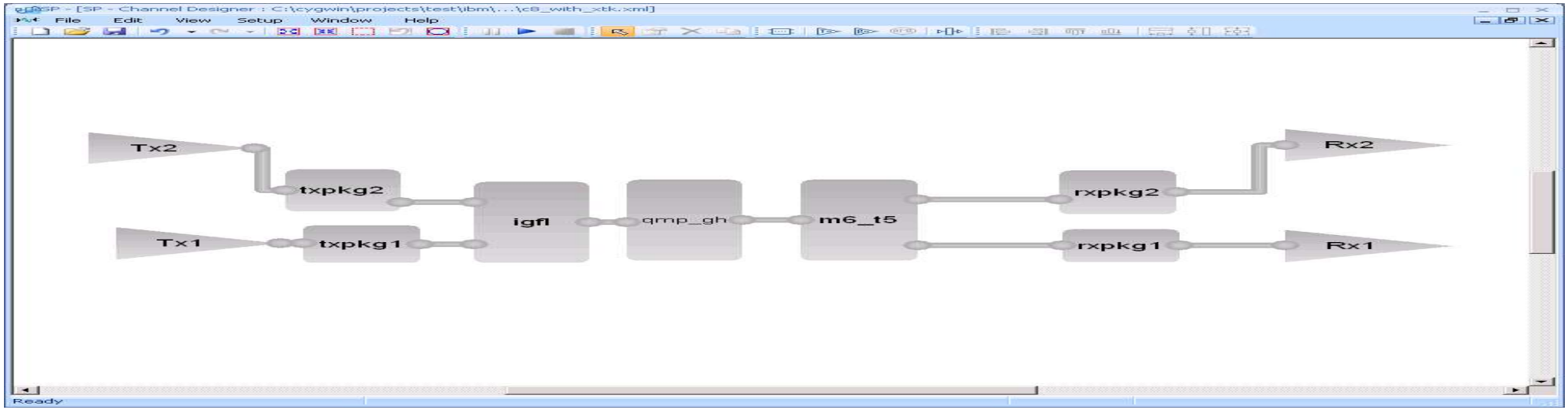
A typical environment for channel design

Sigrity Channel Designer – "SCD"



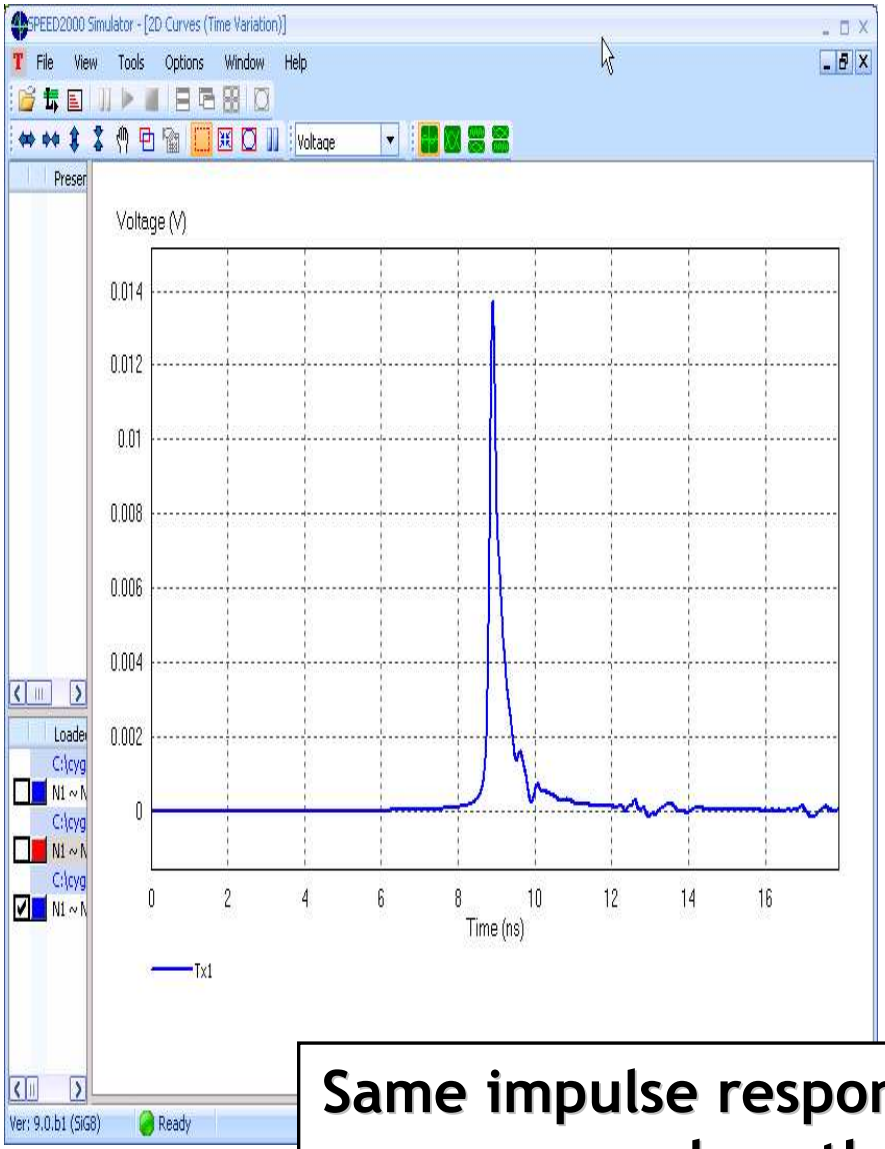
C8 with FFE AMI Model

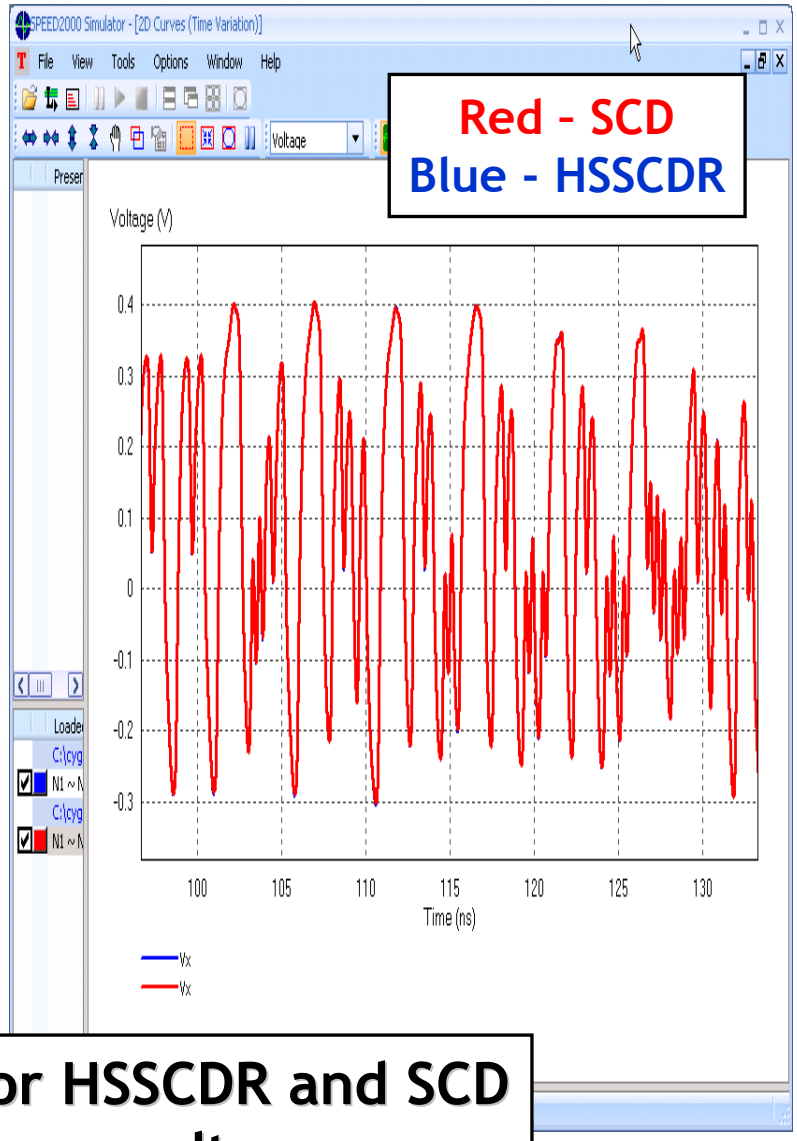
- ffe[c8.ffe]
  - C8.ffe list explicit 4 tap coefficients
- lffe[f4l_m.ffe]
  - F4l_m.ffe lists explicit limits for the 4 tap ffe
- HSSCDR was run with this setting
- SCD was run with IBM supplied Tx AMI model with ffe and lffe parameters



Multi-tool waveform comparison

(Using same impulse response for both tools)

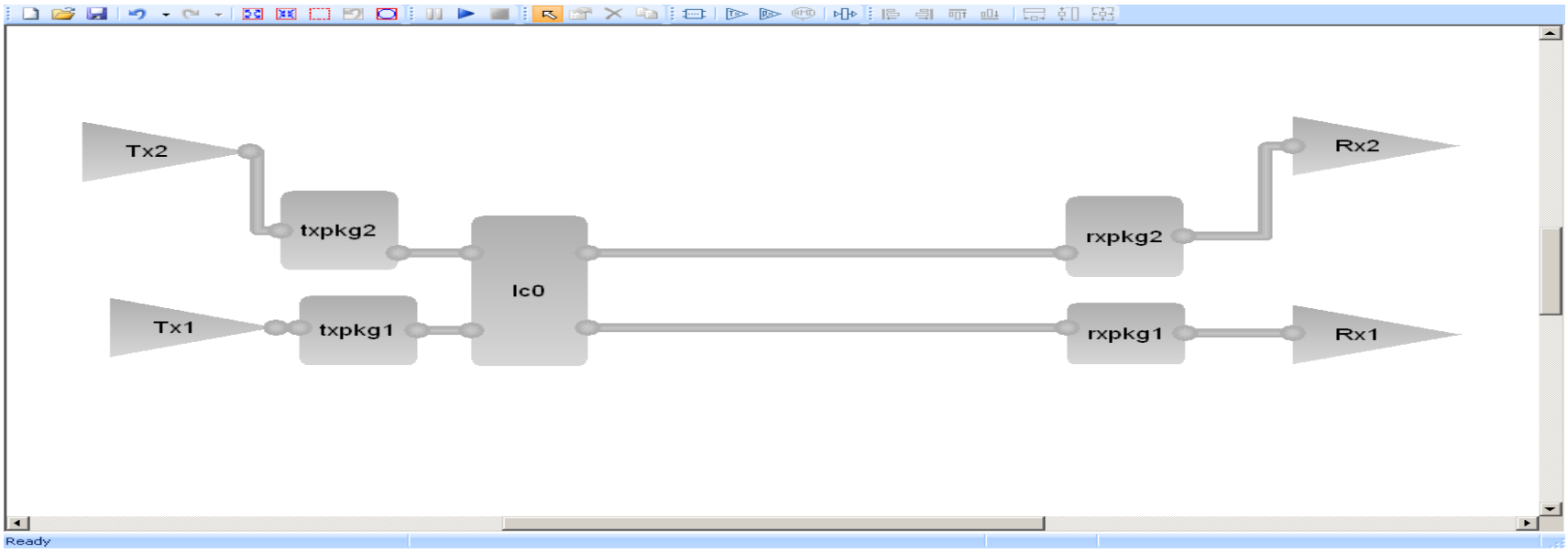




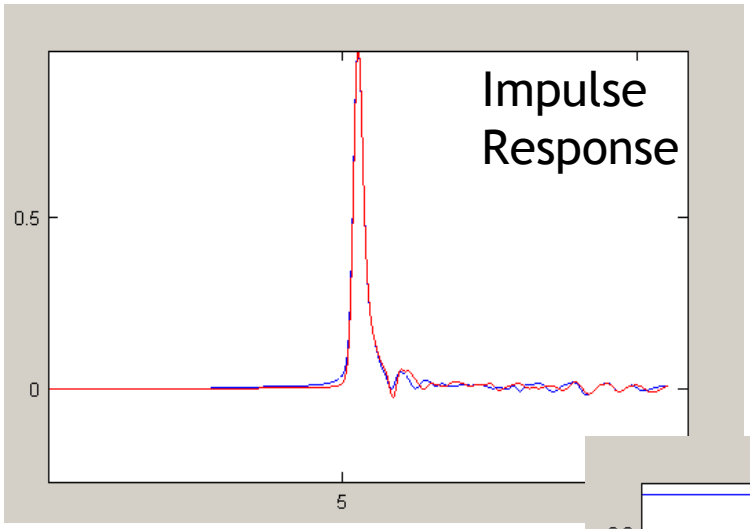
Same impulse response for HSSCDR and SCD produce the same results

C10 with FFE AMI Model

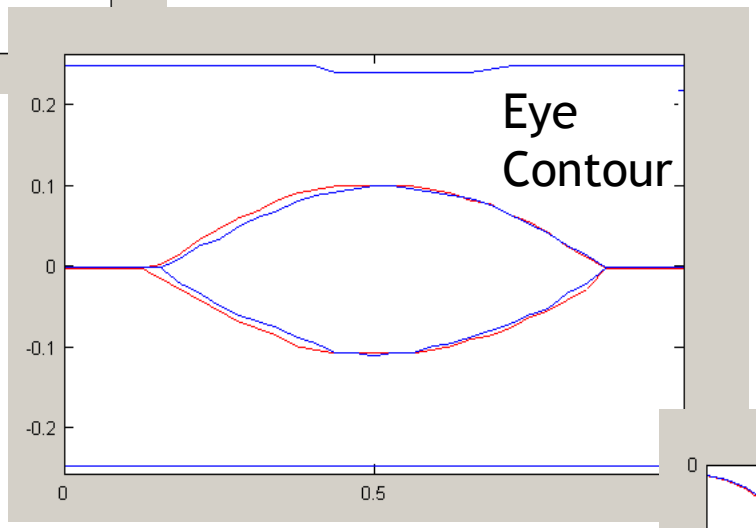
- Automatic 4 tap optimization
- lffe[f4l_m.ffe]
  - F4l_m.ffe lists explicit limits for the 4 tap ffe
- HSSCDR was run with this setting
- SCD was run with IBM supplied Tx AMI model with ffe and lffe parameters

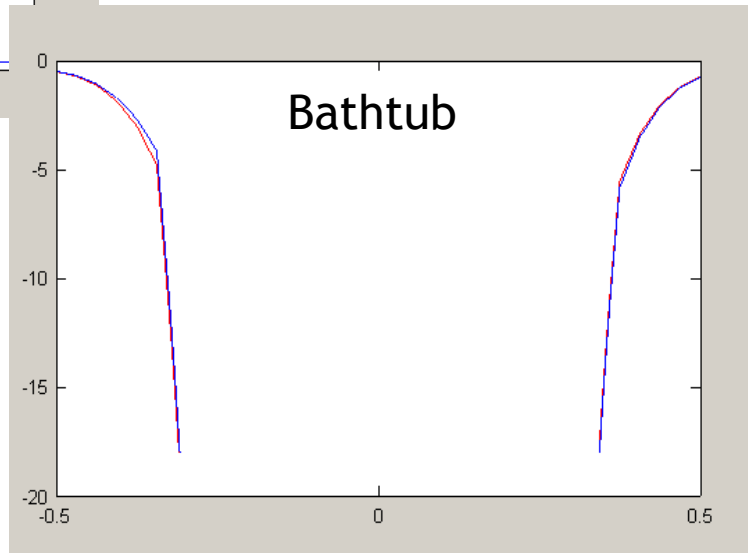


Extremely similar multi-tool simulation results



Red - SCD (w/ HSPICE)
Blue - HSSCDR





Yes “EDA tool agnostic” but …
Slight differences of circuit simulation for impulse response can result in slight differences for higher-level channel behavior.

Thank You!