

Preparing for Future System Design Challenges: Advanced Technologies and Integration

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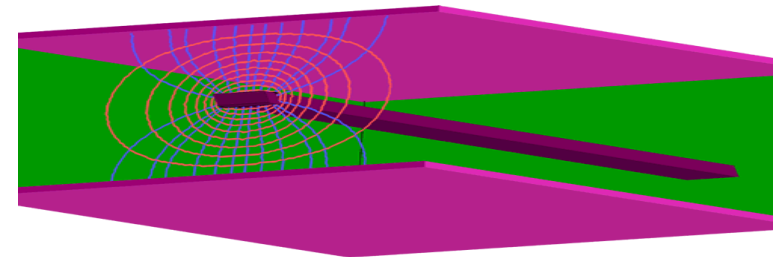
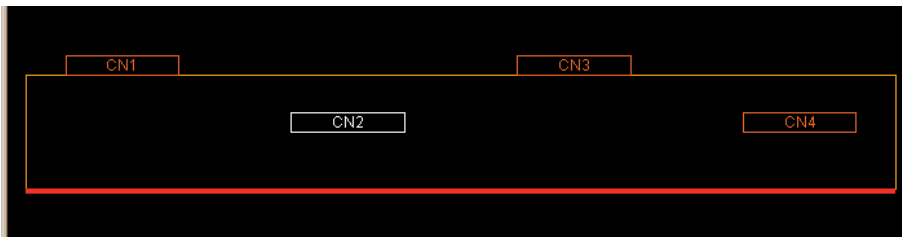
Zhen Mu Ph.D
Product Marketing Manager

Topics

- EM research and implementation in SI tools
- Industry trend in serial link designs
- EDA tools need to be enhanced in
 - supporting future design challenges
 - creating a user-friendly environment for majority SI engineers and designers in solving complex EM problems
 - making seamless integration across all design and simulation domains

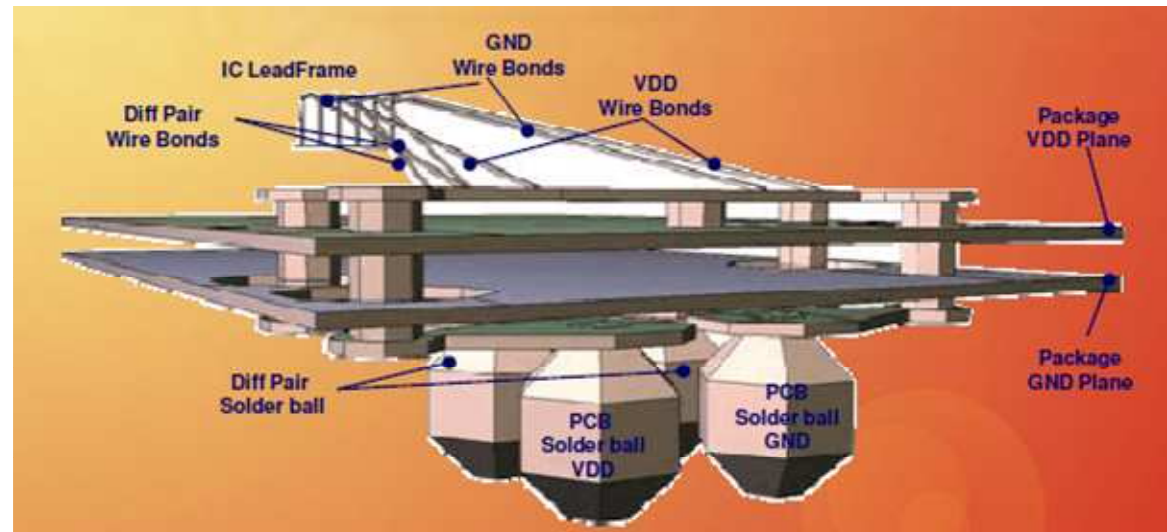
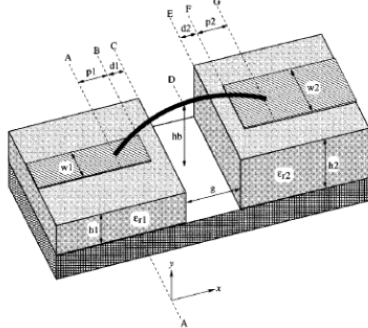
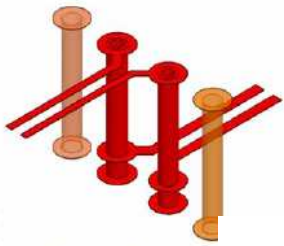
EM research and implementation in Signal Integrity tools

- Electromagnetic field theory and numerical method in PCB interconnect analysis
 - From the beginning of Signal Integrity tools
 - Example:
 - Greenfield 2D from Quantic in late 80s
 - Interconnect modeling tool for traces on board
 - All SI tools today include 2D field solvers for trace modeling
 - Improvements on field solvers almost in every release of all SI tools



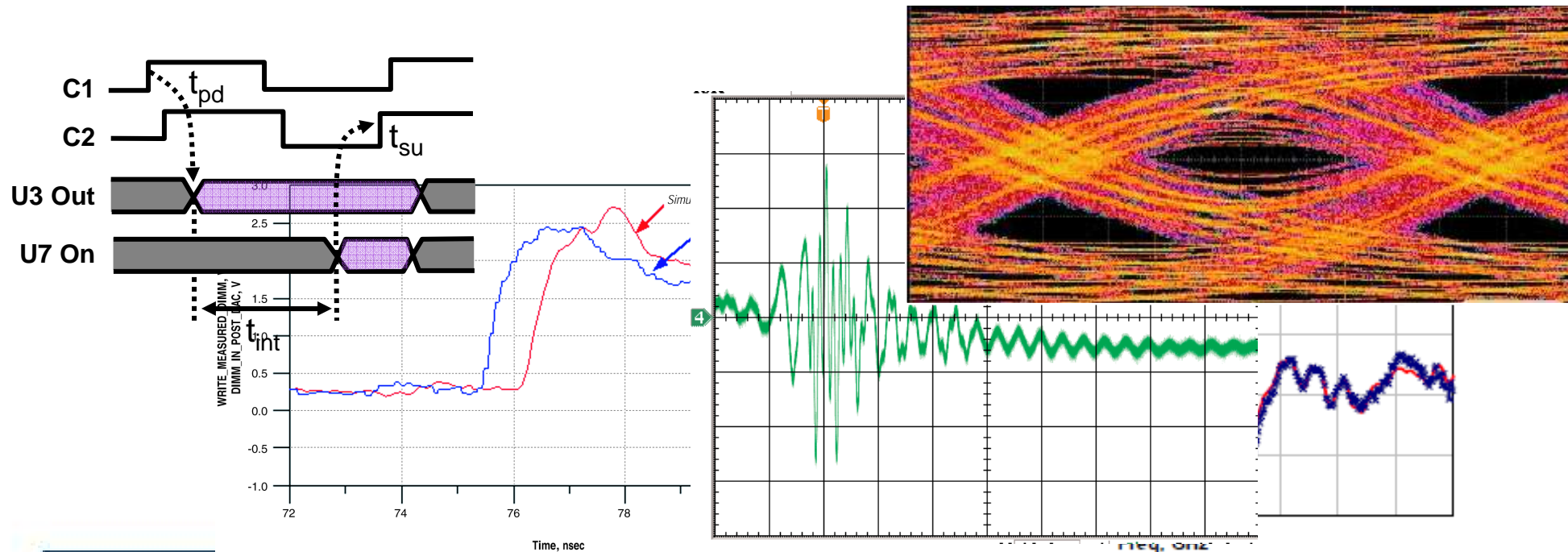
EM research and implementation in Signal Integrity tools

- Advanced modeling methods are introduced to SI tools as high speed simulation mythologies evolve
 - SI tools have introduced 2.5D or 3D field solvers to analyze
 - Complex structures on signal path and power delivery path
- Question: is this enough for high-speed designer?



EM work to serve hardware designers

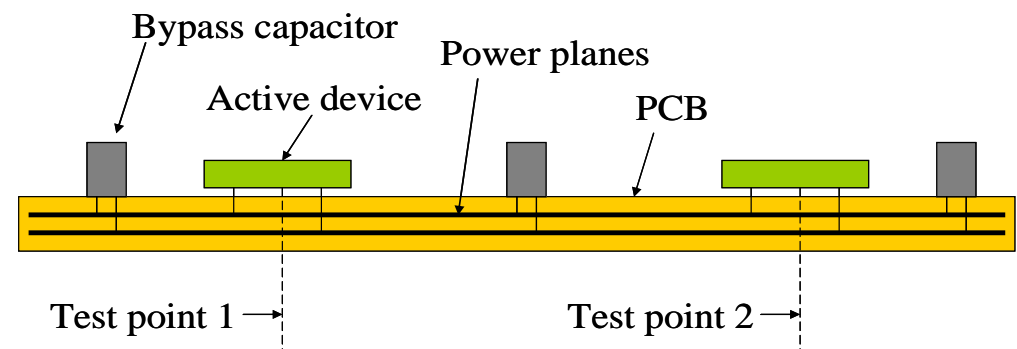
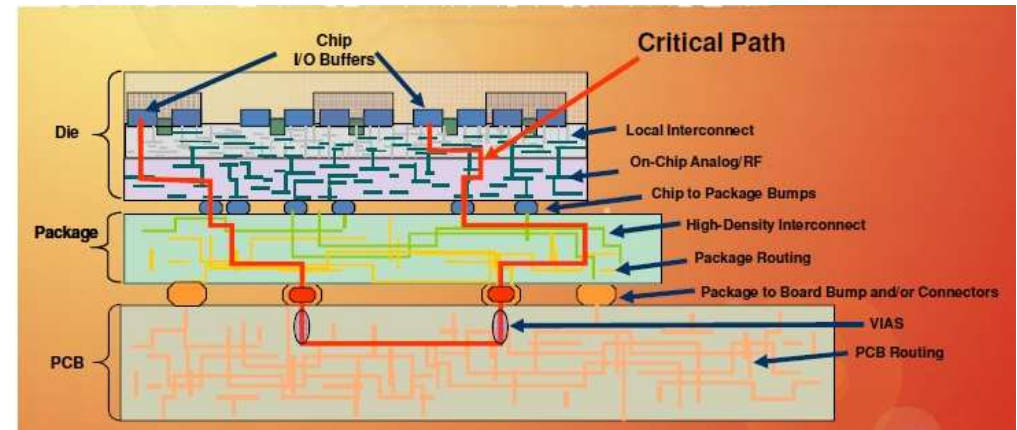
- Understanding the world of high-speed digital designs
 - Digital designers observe / describe signal or power behavior in time domain
 - Design goal is defined and measured in time domain
 - Signal quality, Power stability, and Timing budget



EM work to serve hardware designers

→ Understanding the world of high-speed digital designs (cont')

- Signals are studied from Die to Die
- Power delivery is designed from voltage source to IC components
- EM phenomenon is “buried” in signal waveforms and voltage ripples



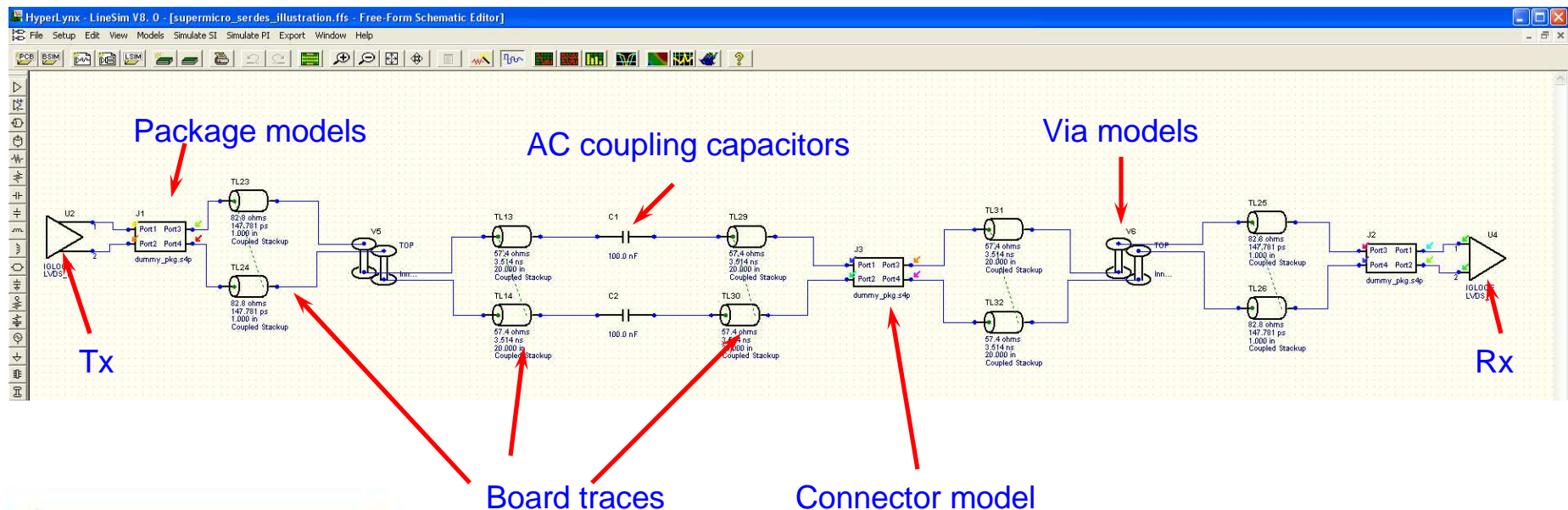
Courtesy image from IEEE EMC 2005 Symp. Panel



EM work to serve hardware designers

→ Simulation requirements for SI tools

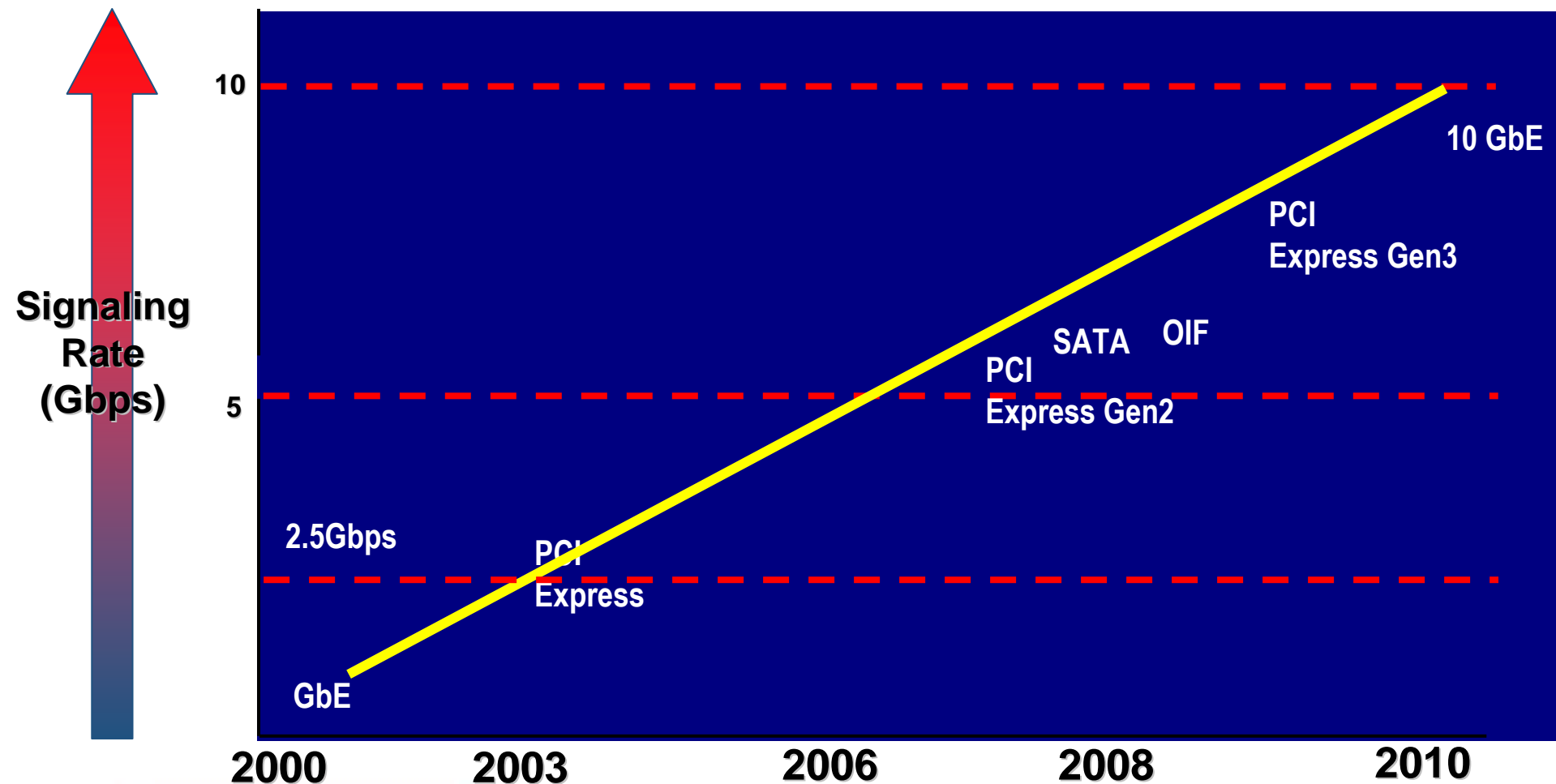
- Signal models + interconnect models
- Power source / sink models + delivery path models
- EM modeling is only part of the solution
- Advanced device models are critical to the success of entire signal path or power delivery path simulation



What is happening in high speed design world today?

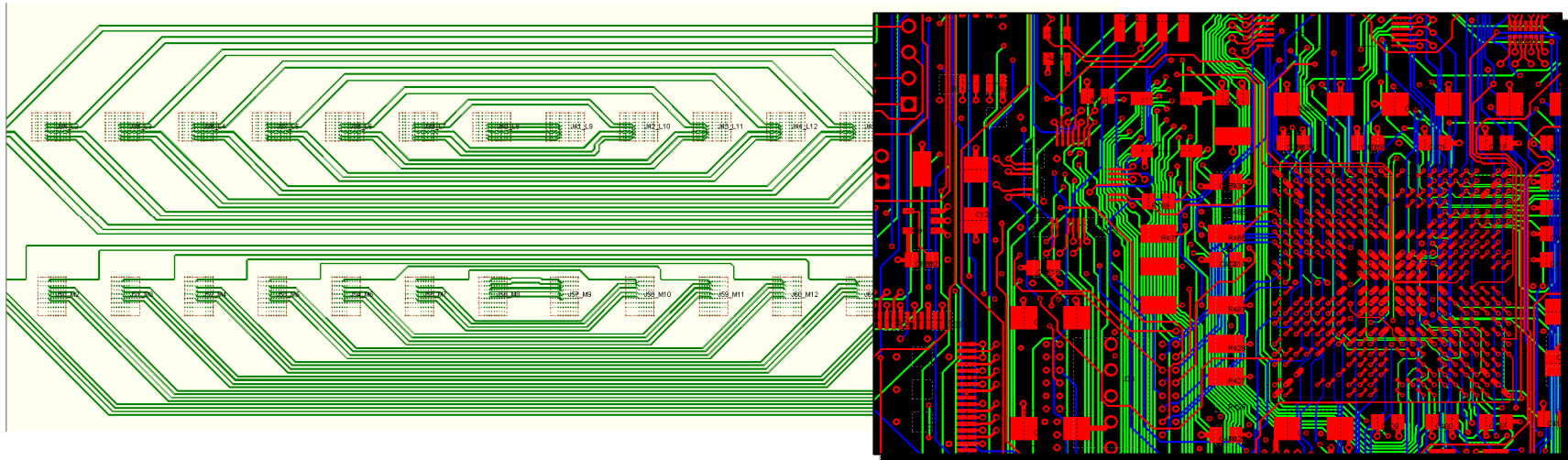
- In 2008, most of I/O interface works at the rates of 5 to 6Gbps
 - PCI Express Gen2 at 5Gbps for computer I/O buses
 - Optical Internetworking Forum (OIF) at 6Gbps for network communication
 - Serial Advanced Technology Attachment (SATA) III/SAS II at 6Gbps for storage area networks
- Next-generation standards will support data rates from 8 to 11Gbps
 - IEEE 10G Ethernet
 - PCIe Gen3 (8.0 Gbps) for computer I/O buses

What is happening in high speed design world today?



What is happening in high speed design world today?

- In general, 40% of the signal nets on board carry signals with data rates at multiple Gbps
 - 2.5 / 3.125Gbps signals have become part of the main stream designs
- This is where advanced analysis capability applies



Design flows of multi Gbps signals

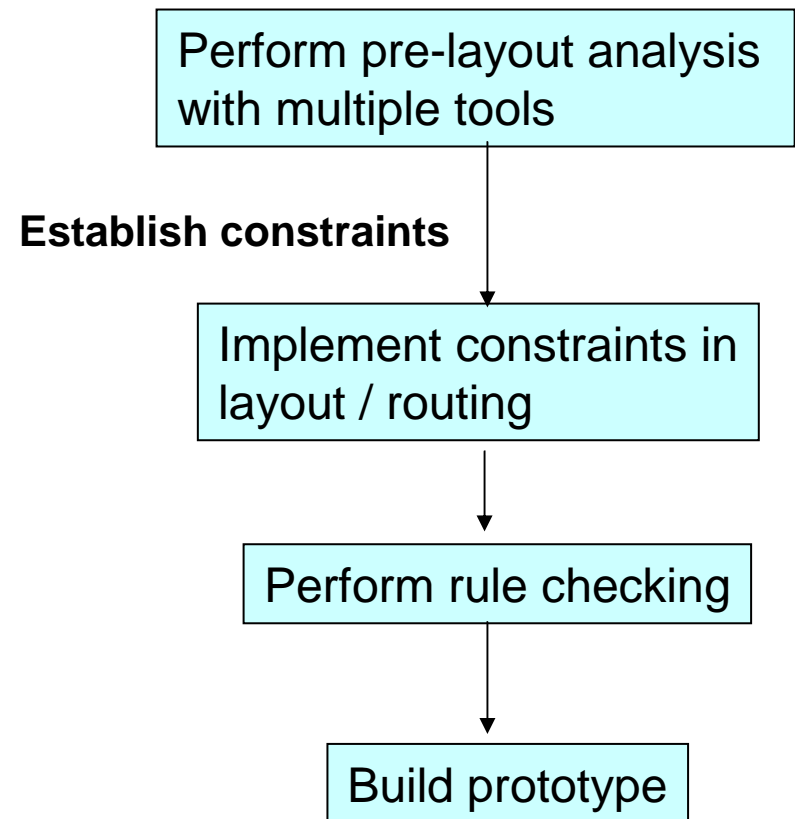
- Traditionally, for advanced designs
 - Multiple tools are used
 - results from these tools are pieced together
 - the behavior of individual structures on signal or power path are carefully studied
- What is missing today
 - The verification capability when large amount of SERDES signals present on board
 - The capability to apply EM solvers intelligently in post-route environment



Design flows of multi Gbps signals

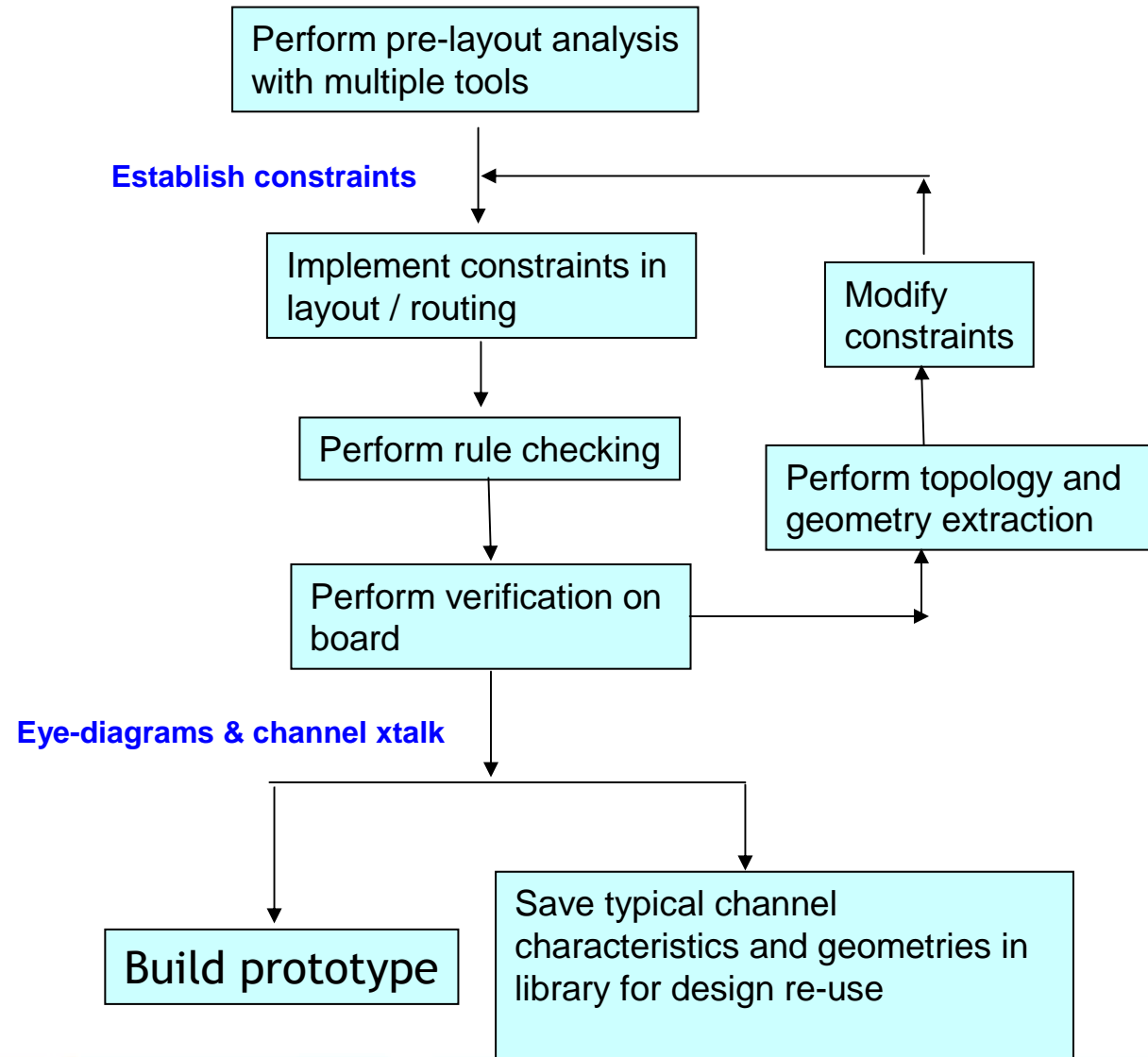
→ Existing multi-Gbps design flow

- Design depends on the usage of various tools and combining simulation results
- Design success heavily depends on pre-layout analysis
 - Very little is done in verification at board level
- Effective when
 - the number of SERDES signal nets is at minimum
 - new interface



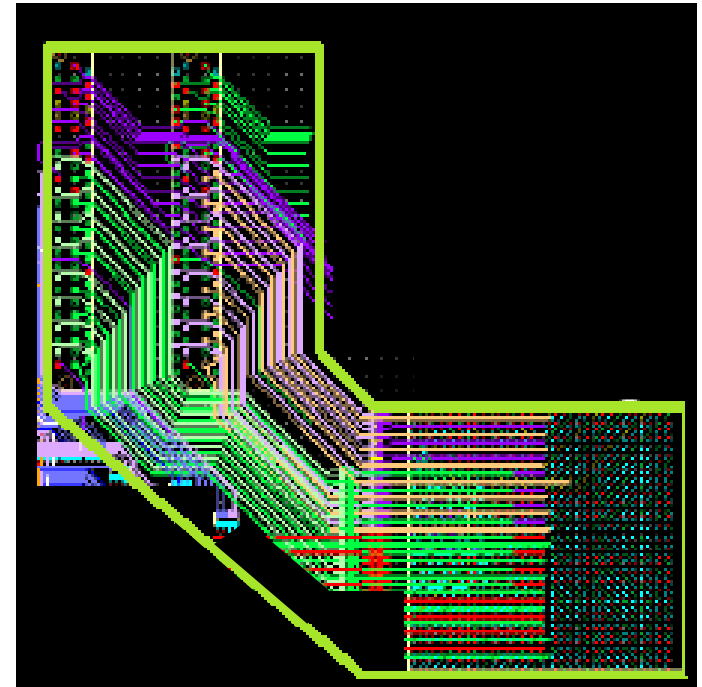
Design flows of multi Gbps signals

- Desired multi-Gbps design flow
 - Unified design and analysis environment
 - Efficient verification at the post-route stage



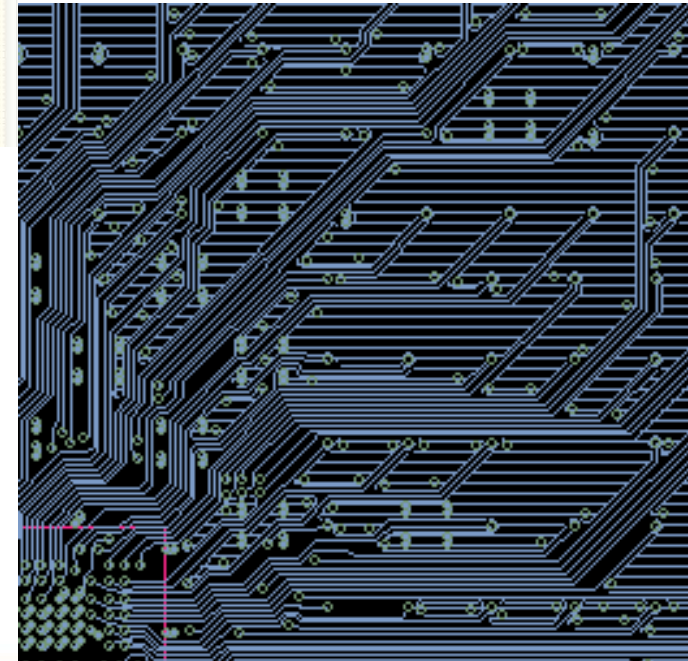
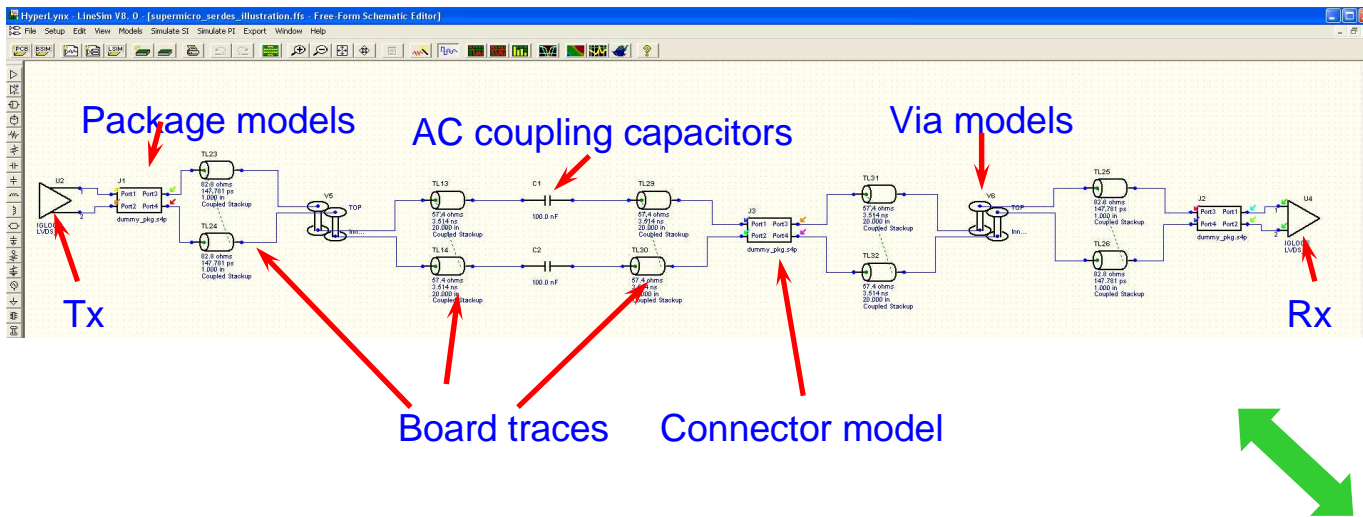
Challenges to SI tools

- With half of the nets on board carrying signals at the rates in Gbps range
 - SERDES channels lost “privilege”
- Requirements for SERDES analysis
 - Tightly integrated layout and analysis capabilities
 - Effective topology and geometry extraction
 - Robust and flexible simulation environment to simulate models from different sources
 - Efficient post-route batch mode channel analysis
 - Good model library management for design re-use



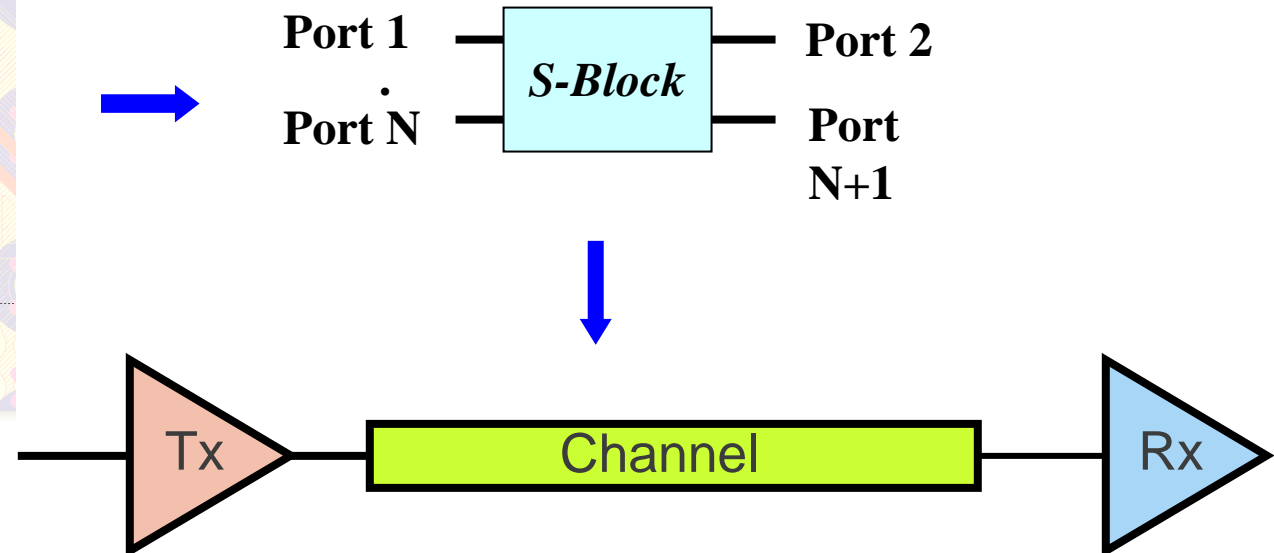
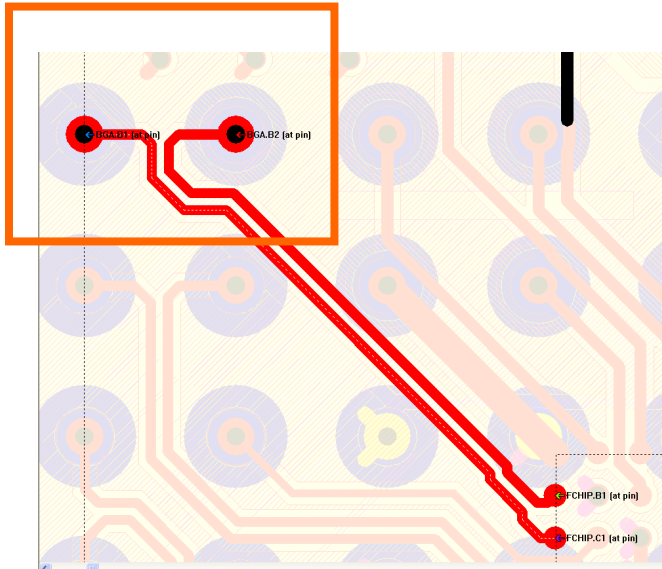
Challenges to SI tools

- Tightly integrated layout and analysis capabilities
 - Easy to implement and modify constraints



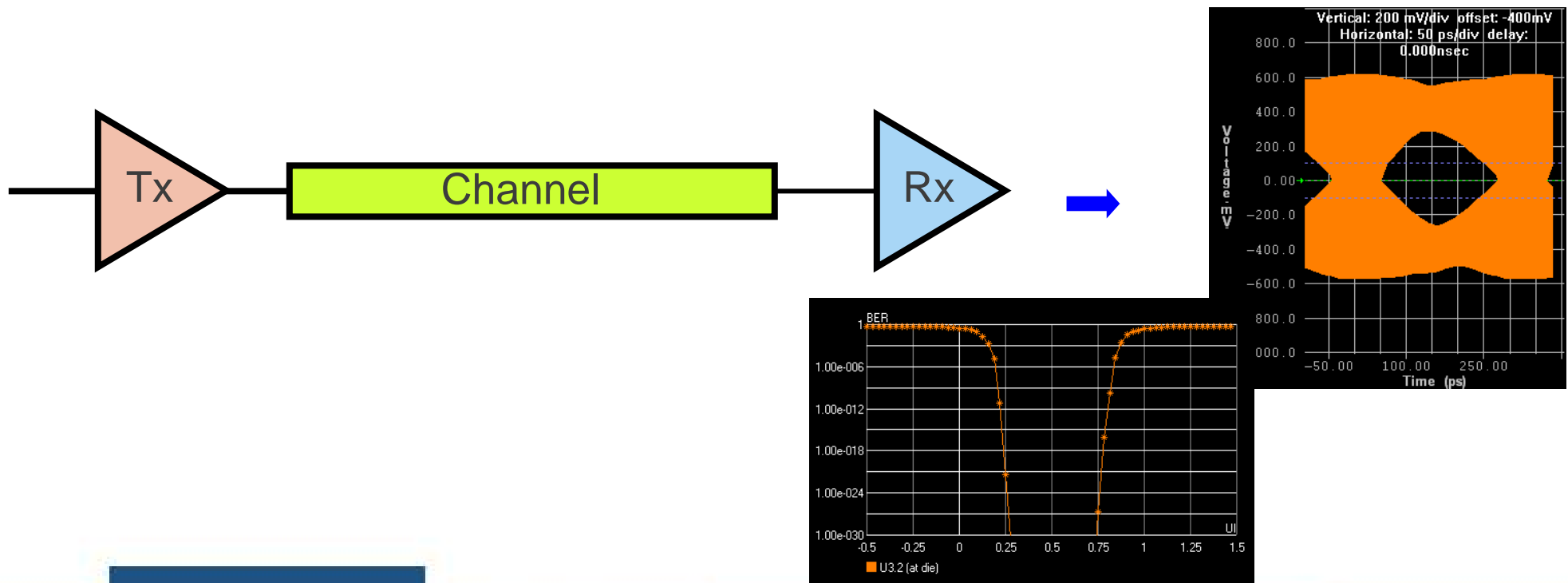
Challenges to SI tools

- Effective topology and geometry extraction
 - Easy to examine problematic channels
 - Easy to identify / select geometries to be modeled using advanced EM solutions



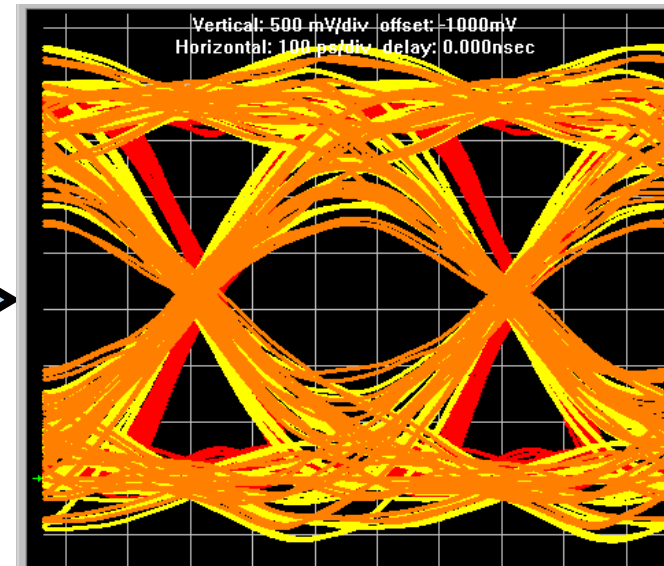
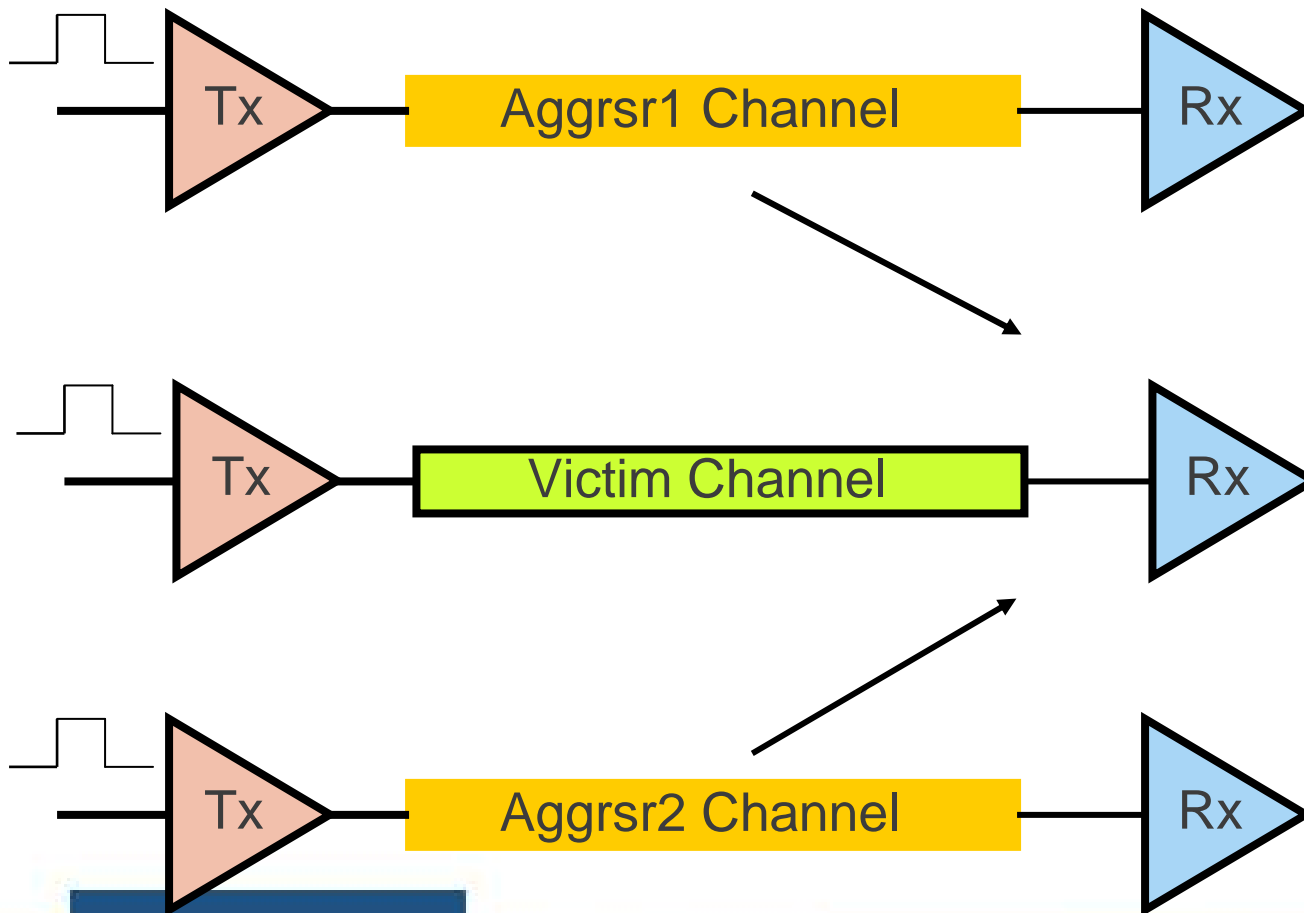
Challenges to SI tools

- Robust and flexible simulation environment to simulate models from different sources
 - Easy to simulate device models in different formats/standards (HSpice, classic IBIS, or IBIS-AMI)
 - Efficient and accurate S-parameter simulation in time domain



Challenges to SI tools

- Efficient post-route batch mode channel analysis
 - With channel coupling effects included



Challenges to SI tools

- How to make tool easy to learn and re-learn
 - Wizard driven simulation flow
- How to complex-algorithm/theory based function easy for designers who have little time to study a tool in detail

Preparing for the challenges

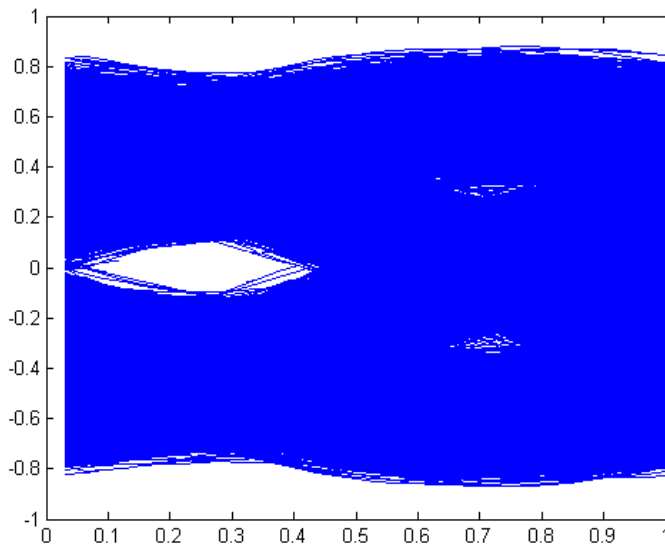
- History of SI tools development shows
 - Circuit simulator providers keep adding in field solutions
 - Field solver providers expand solution base to include advanced device modeling
 - Reason is obvious: EM modeling and circuit device simulation are not separable
- Detailed discussions (what we have done)
 - Worst bit sequence pattern prediction
 - Robust and efficient S-parameter simulation
 - Power and signal co-simulation

Worst bit sequence pattern prediction

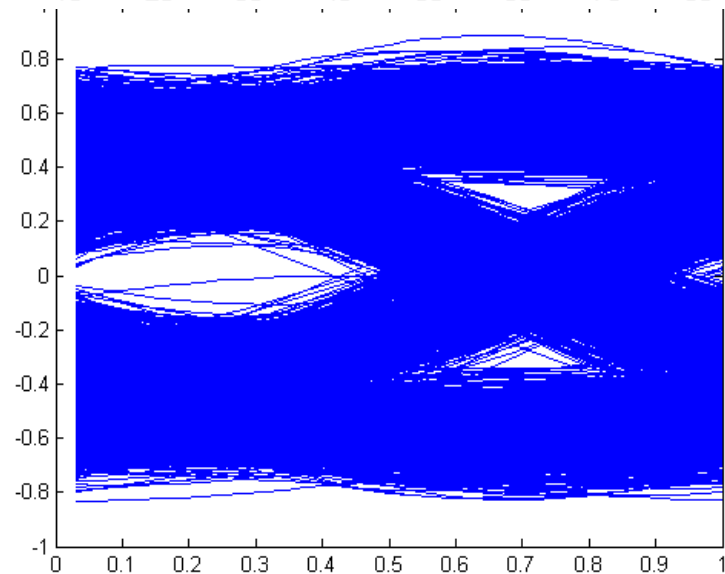
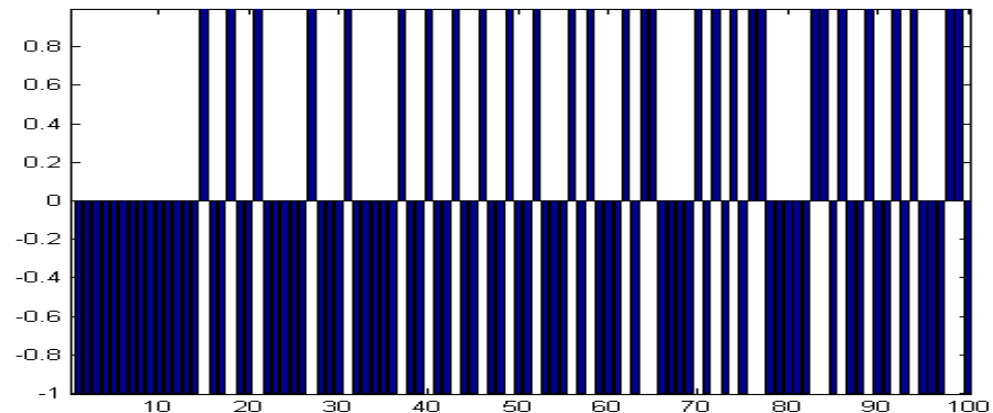
- Channel analysis function has been integrated in SI tools since 2004
 - Using channel's Impulse Response to characterize a channel
 - Avoiding long (or impossible) Spice-like simulation to obtain reliable eye counters
- Why need to predict worst bit sequence?
 - Channel simulation can still take long time when billions of bits are simulated
 - It may not catch the worst case that certain bit pattern can cause

Predict Worst Bit Pattern

- Can it be done?
 - Yes, by the worst case searching algorithm



1,000,000 PRBS. Eye remains open



10,000 PRBS with 100-bit worst sequence. Eye closed

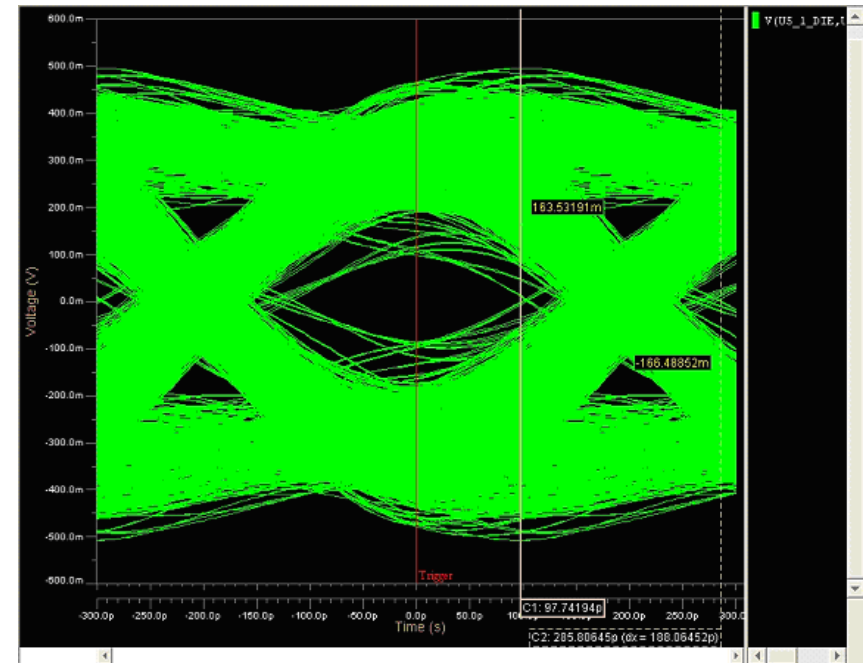
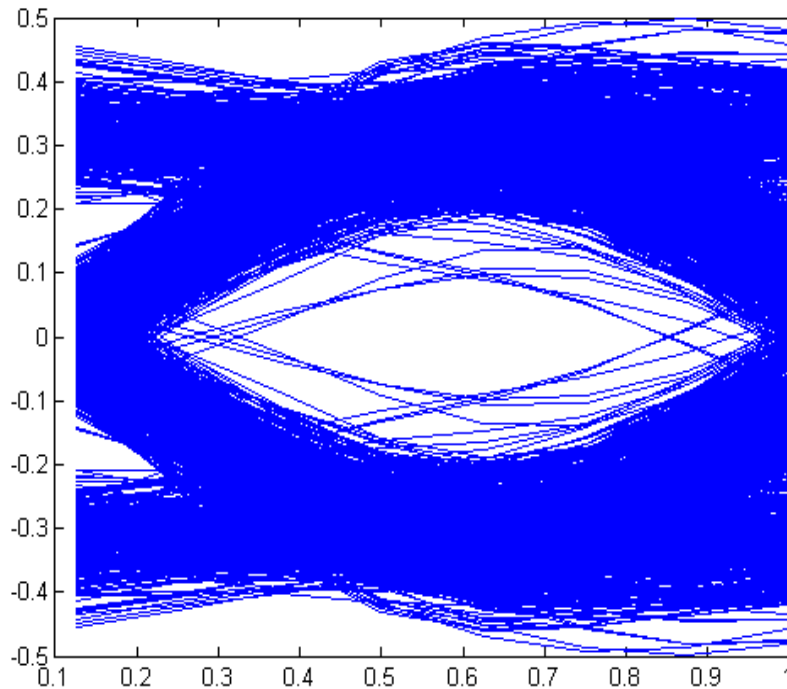


Predict Worst Bit Pattern

- Procedure overview
 - Impulse Responses generation
 - Channel simulation in time domain with certain number of bits
 - Statistical analysis
 - Combining results from channel simulation and statistical analysis to obtain worst bit pattern
 - Verifying the pattern with channel simulation

Predict Worst Bit Pattern

- Example: worst sequence solution is verified by time domain simulation
 - Hours or days of channel simulation is not needed

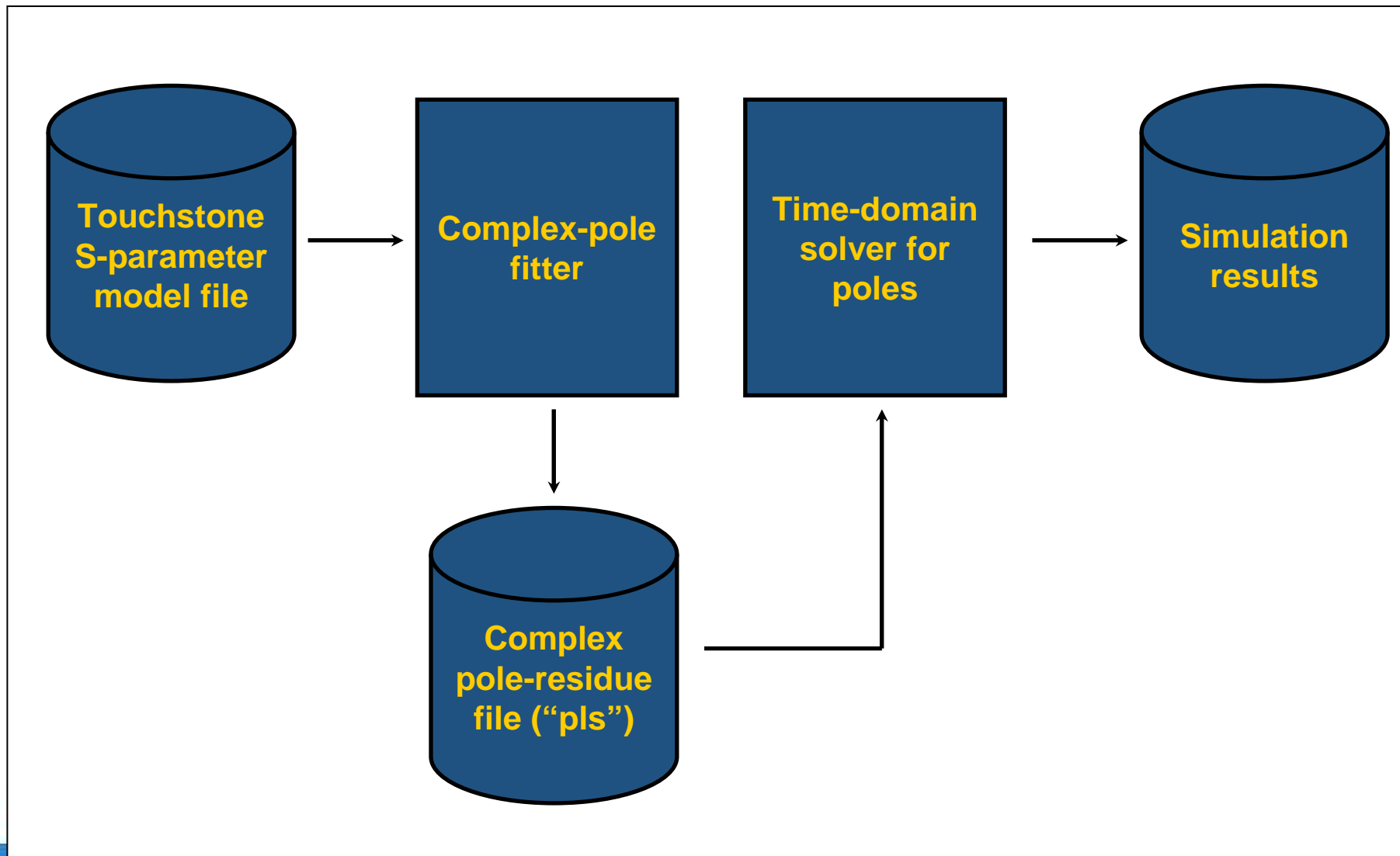


Robust and efficient S-parameter simulation

- S-parameter simulation in time domain is important in multi-Gbps signal analysis
- There are many methods available to perform the simulation
 - Direct convolution
 - Equivalent subcircuit
- A new method based on complex pole fitting (CPF)
 - S-parameters are represented in a very compact pole-residue form

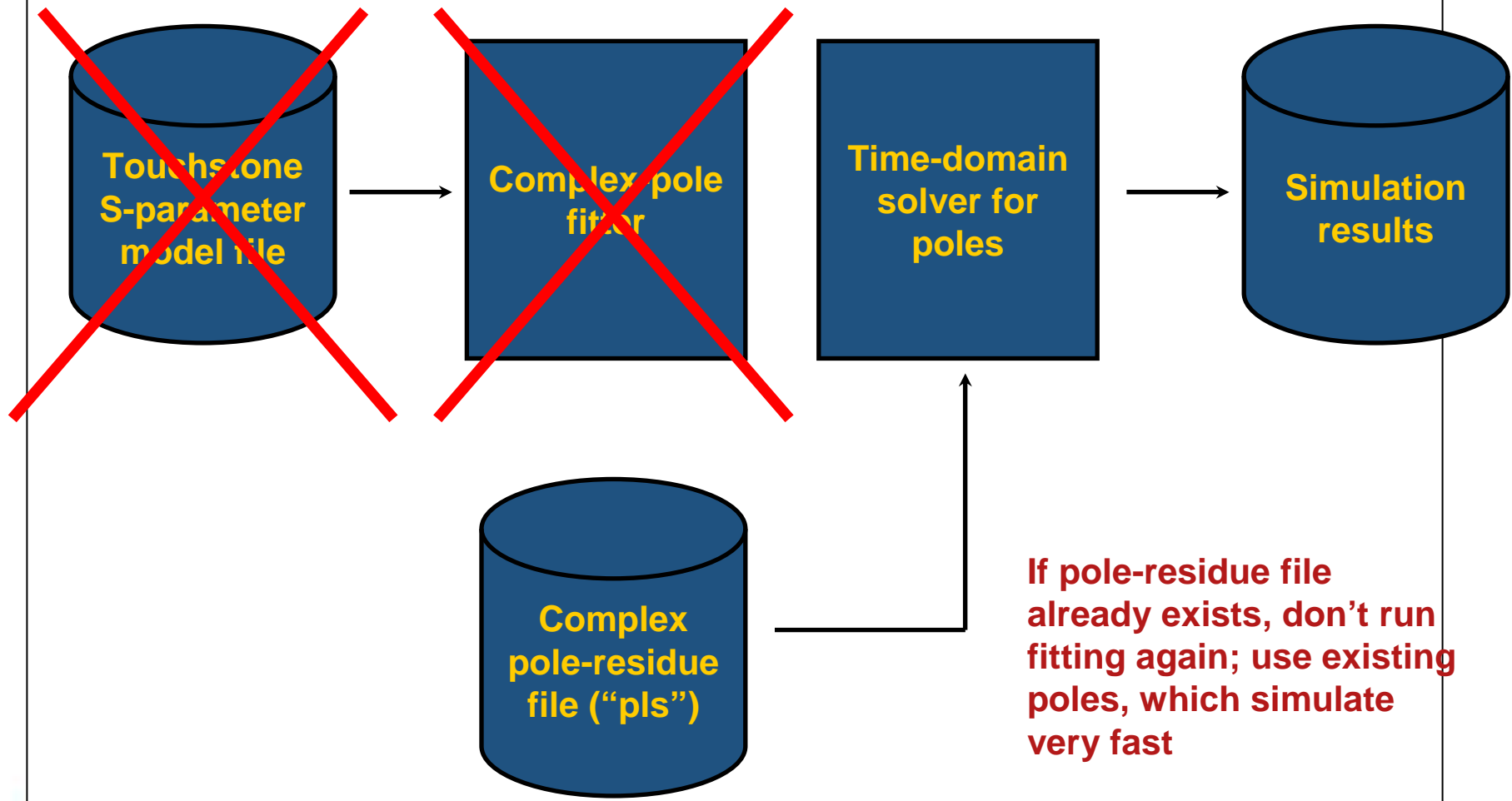
Robust and efficient S-parameter simulation

→ How does it work?



Robust and efficient S-parameter simulation

→ Pole-residue file is re-usable



Robust and efficient S-parameter simulation

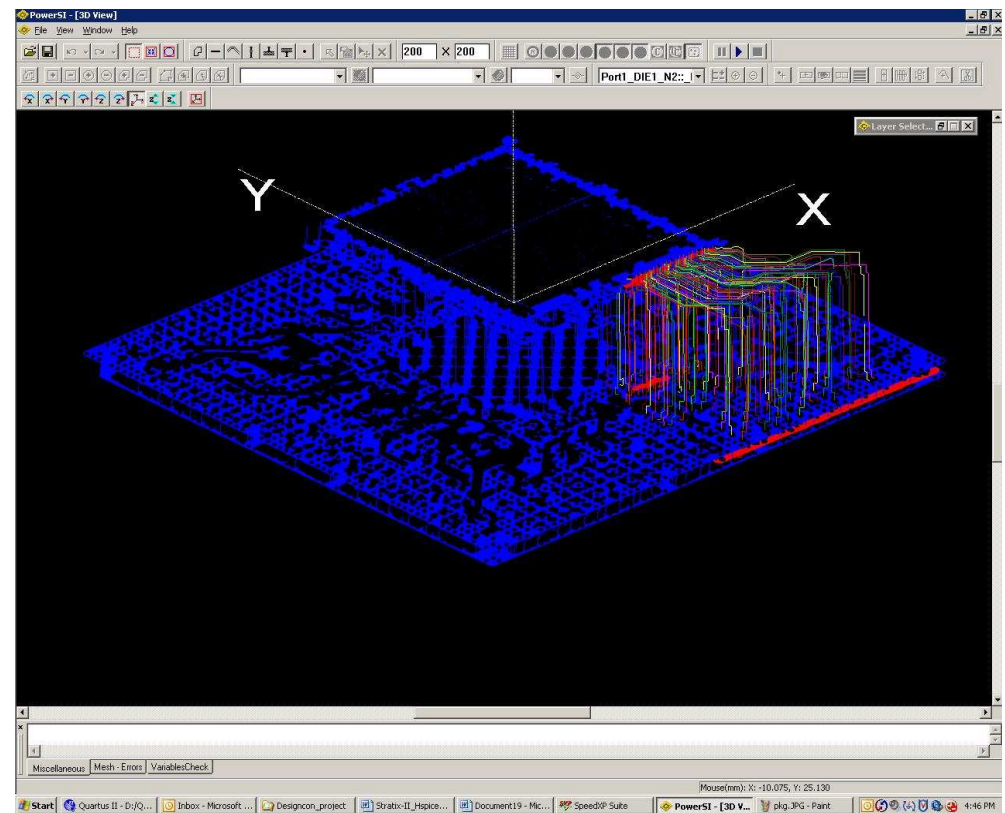
- Performance of the convolution, CPF, and equivalent circuit
 - 158-port, fully populated S-matrix
 - Size of TouchStone file: 214MB

Simulator	Solution times for different methods, min					
	Convolution-based	CPF		Equivalent circuit		
		Fitting (one-time penalty)	Transient	Creating equivalent circuit (one-time penalty)	Parsing (each-time penalty)	Transient
ELDO	failed	20.1	3.5	20.3	15.2	6.5
Base simulator	failed	N/a	N/a	N/a	510.0	7.1



Robust and efficient S-parameter simulation

- Published example (DesignCon2006)
 - Single bank of FPGA, 2S130F1508, Altera Corp.

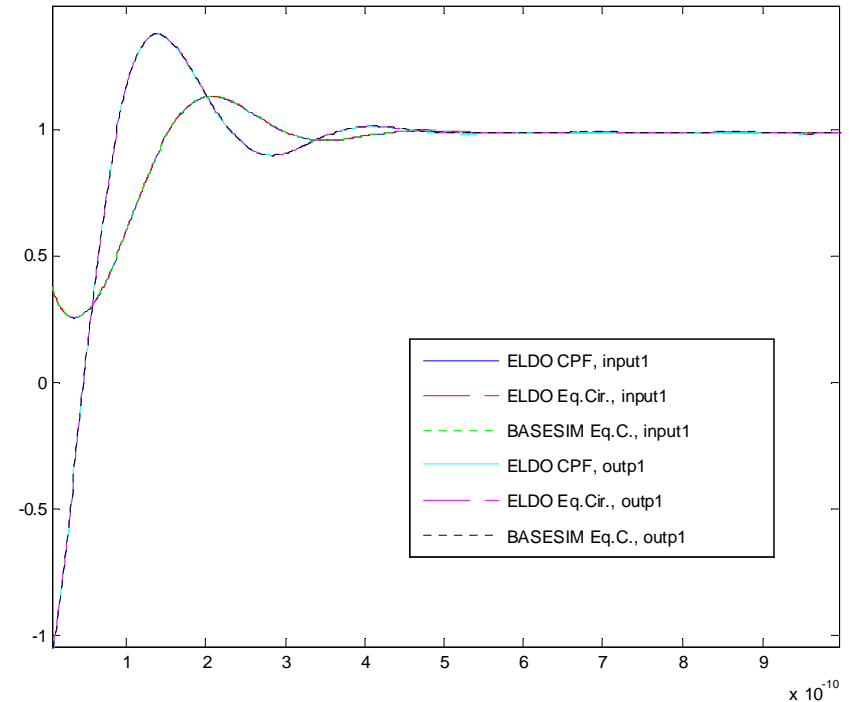


Robust and efficient S-parameter simulation

- Example of large 226-port model
 - Data extraction
 - Logarithmic scale from 1e2 to 1e8Hz then linear up to 4GHz,
 - 425 points total, file size is about 800MB
 - Symmetric fully populated matrix with $226 \times 226 = 51,076$ elements, complex-value functions of frequency
 - Fitting
 - Reading the touchstone - 12 min
 - Fitting & passivity enforcement - 4.1 and 14 min respectively
 - Resulted: 44MB pls file and 54MB sub-circuit

Robust and efficient S-parameter simulation

- Transient analysis of a test circuit
 - Only CPF and equivalent circuit can solve the problem
 - Excellent agreement between
 - solutions by CPF and equivalent circuit in ELDO and equivalent circuit in “Base” simulation



Performance comparison in parsing and solving

	<i>ELDO CPF (with PLS file)</i>	<i>ELDO, equivalent circuit</i>	<i>BASESIM, equivalent circuit</i>
<i>Read/parse/err check</i>	14 sec	38 min 05 sec	11 h 48 min
<i>DC solve</i>	6.8 sec	3 min 55 sec	4 sec
<i>Transient</i>	7 min 22 sec	46 min 09 sec	20 min 11 sec
<i>Total</i>	7 min 43 sec	1 h 28 min 10 sec	12 h 08 min 36 sec

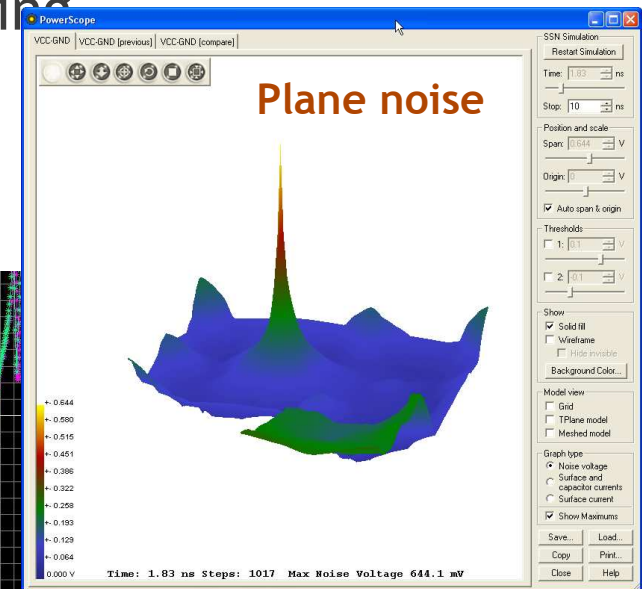
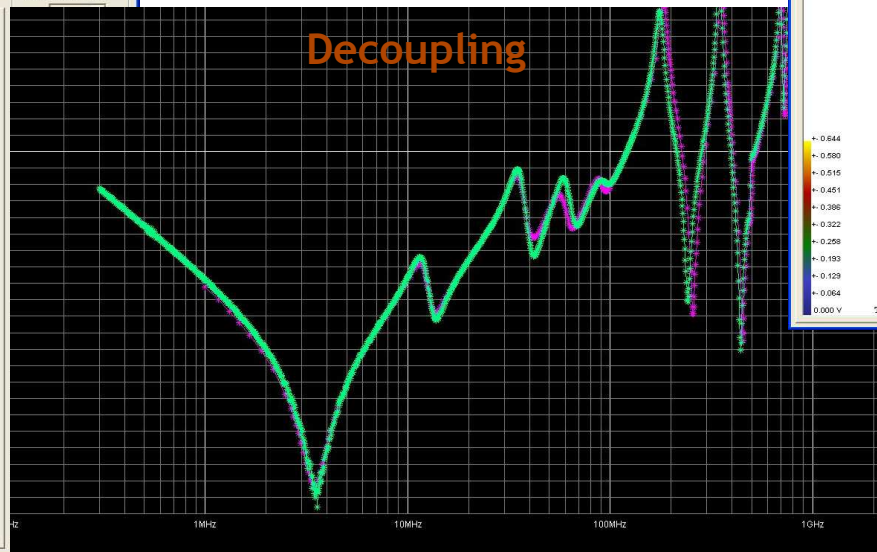
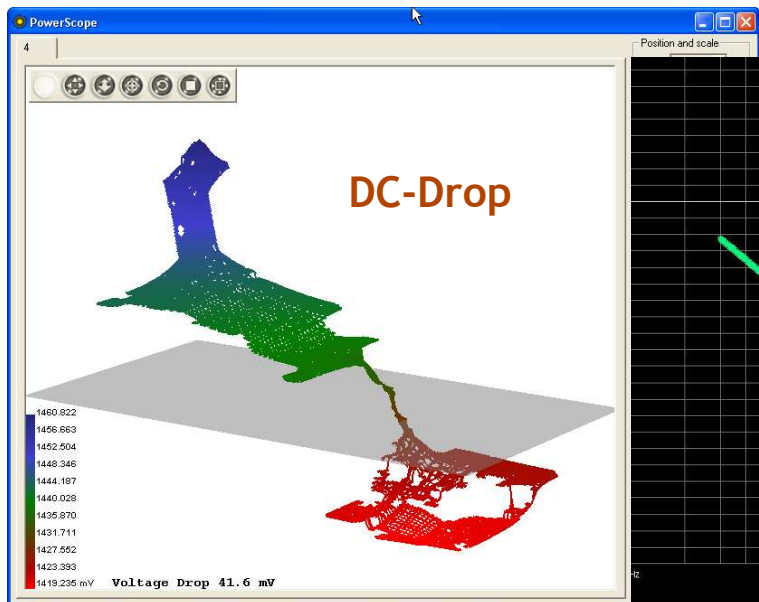


Power and signal co-simulation

- Power delivery design is important in multi-Gbps signal analysis
 - Low power components with low voltage ripple budget
- Decoupling approach and static IR-drop analysis are now available in many SI tools
- One need is to study the power noise effects on multi-Gbps signals
 - Using Power and signal co-simulation function

Power and signal co-simulation

- Designing power delivery network
 - Adequate DC voltage at IC power pins
 - PDN provides sufficient power to active devices
 - Stable voltage supplies while ICs are switching
 - Control voltage ripple

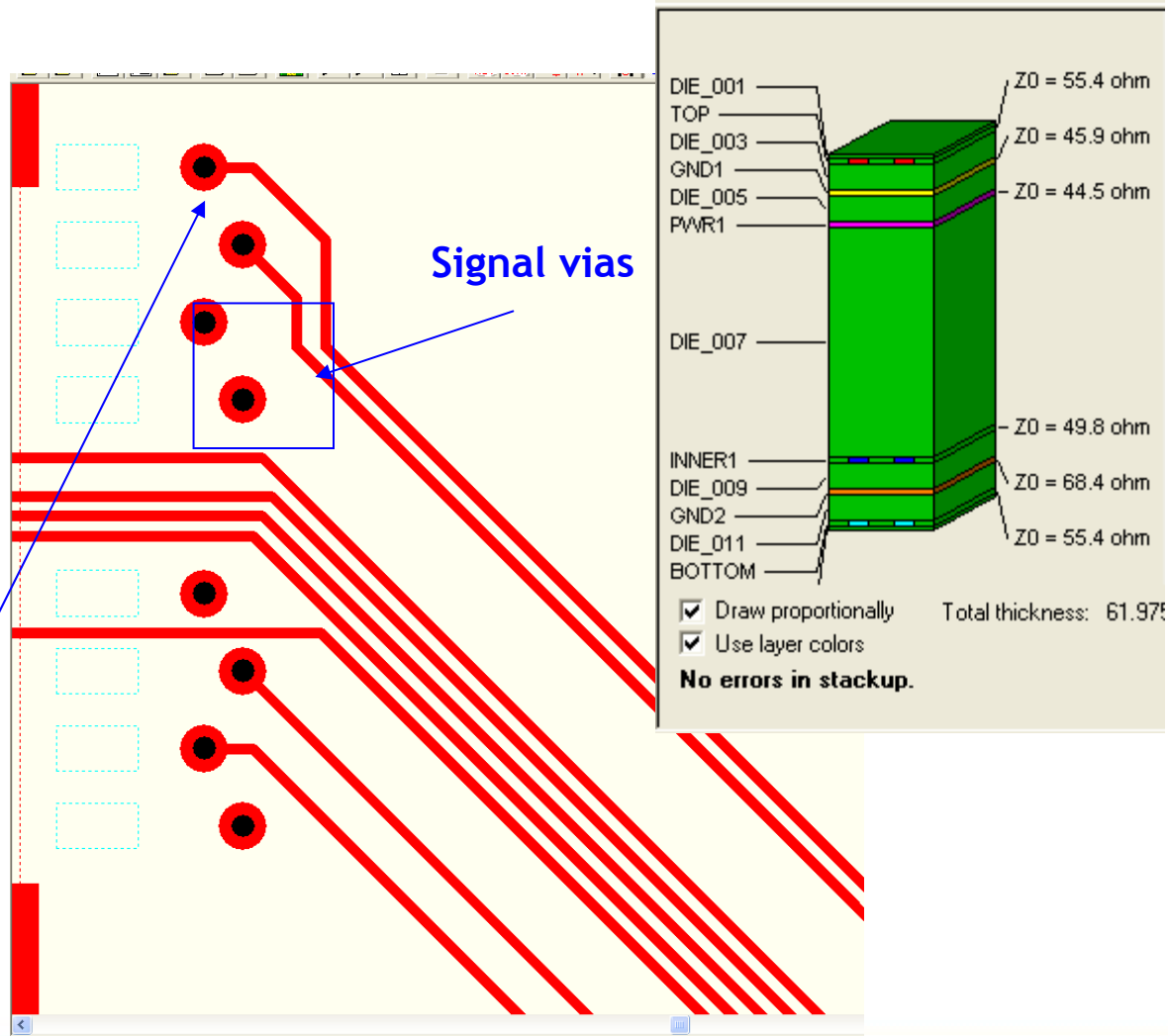


Power and signal co-simulation

→ Plane and signal via interaction affects channel behavior

→ An example of advanced models and EM solvers working together to solve multi-Gbps design problems

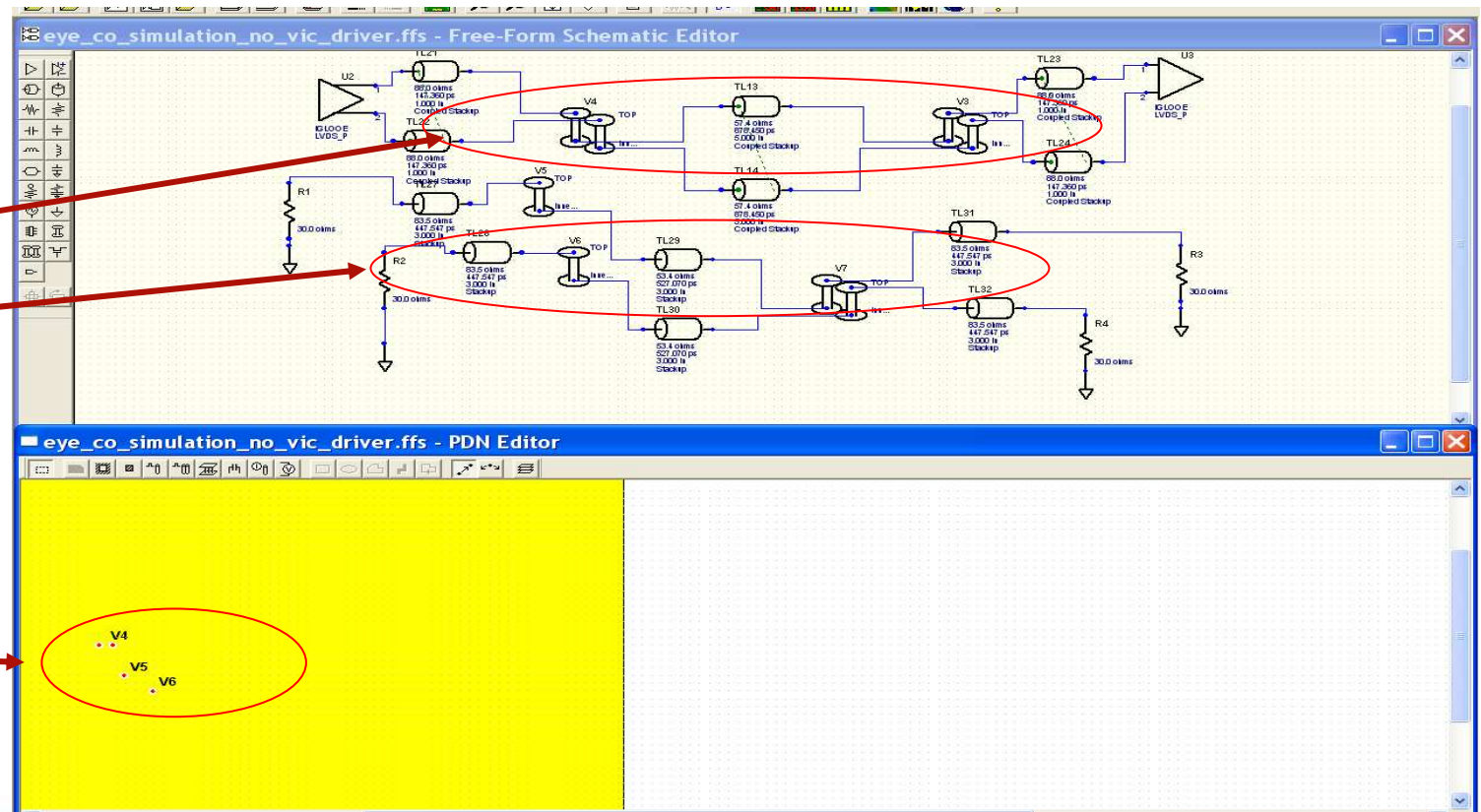
Diff. vias on channel



Power and signal co-simulation

- Extracted topology

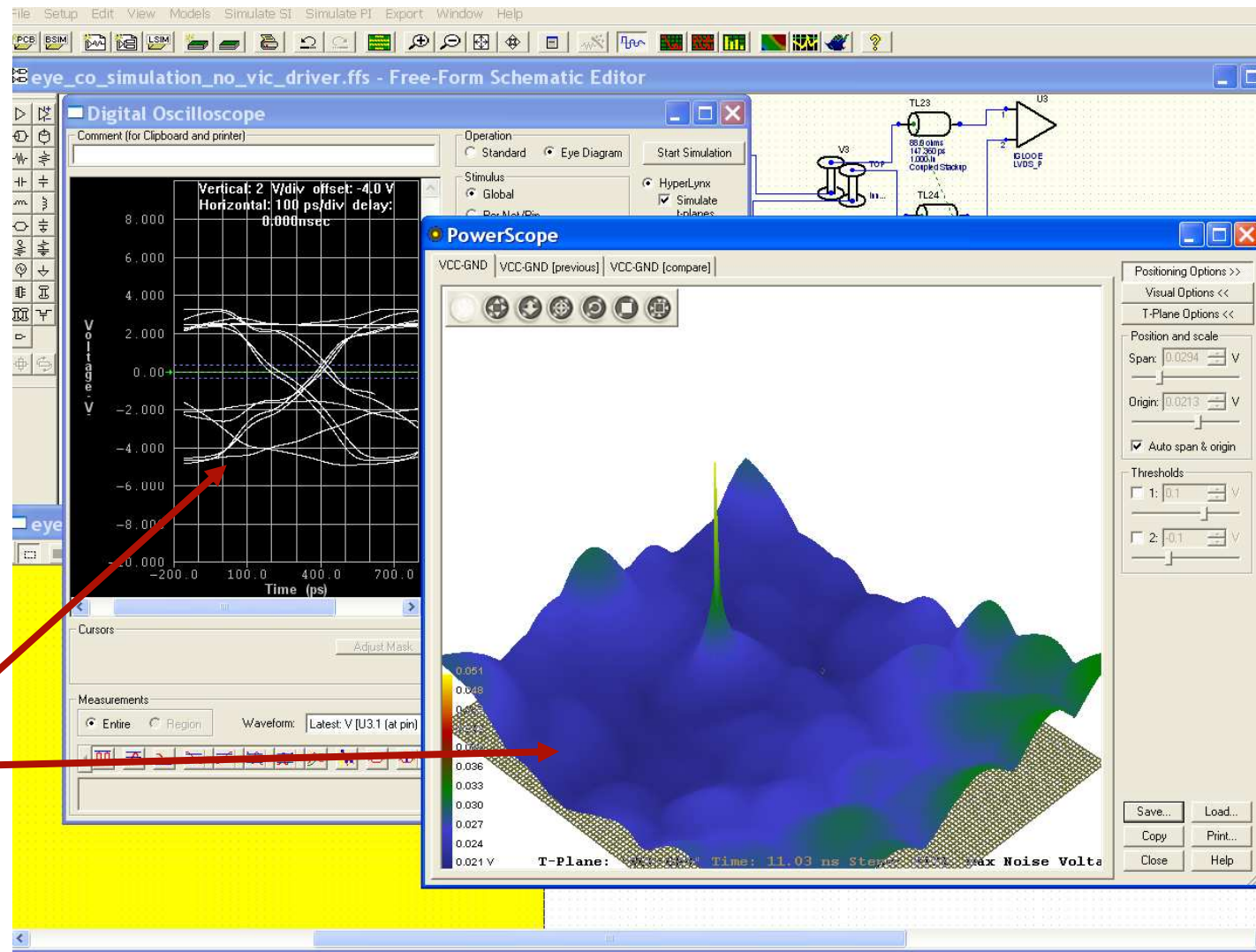
No trace coupling between these two parts



Via coupling through planes

Power and signal co-simulation

→ Co-simulation in progress

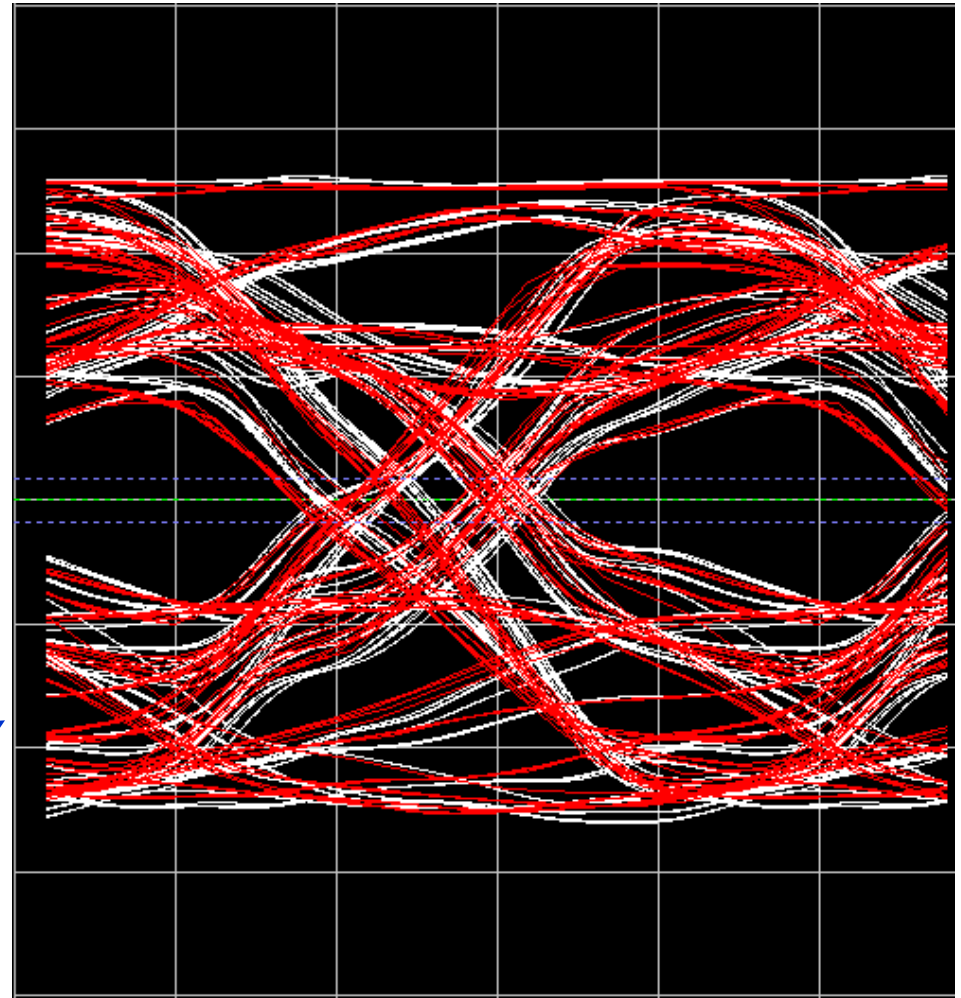


Capture additional noise with co-simulation

Power and signal co-simulation

- Via effects on eye-diagrams
 - Additional noises on an interested channel
 - Caused by interactions between other signal vias through planes

Red: no via-plane interaction
White: with via-plane interaction



Summary

- EM modeling and circuit simulation are two key components of SI tools
- Industry trend in serial link designs present new challenges to SI tools
- SI tool providers need to be prepared in
 - supporting emerging technologies in high-speed designs
 - making complicated solving capability simple (not simpler) for majority high-speed designers
 - providing seamless integration environment across all design and simulation domains
- Mentor is open to work with universities to meet new design challenges!

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