Greetings from
Georgia Tech

An Industry – Academic Collaborative Model for EM CAD Research and Development in Packaging

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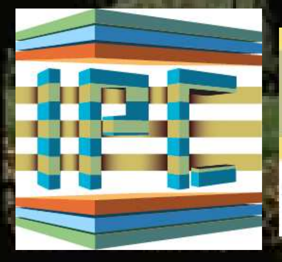


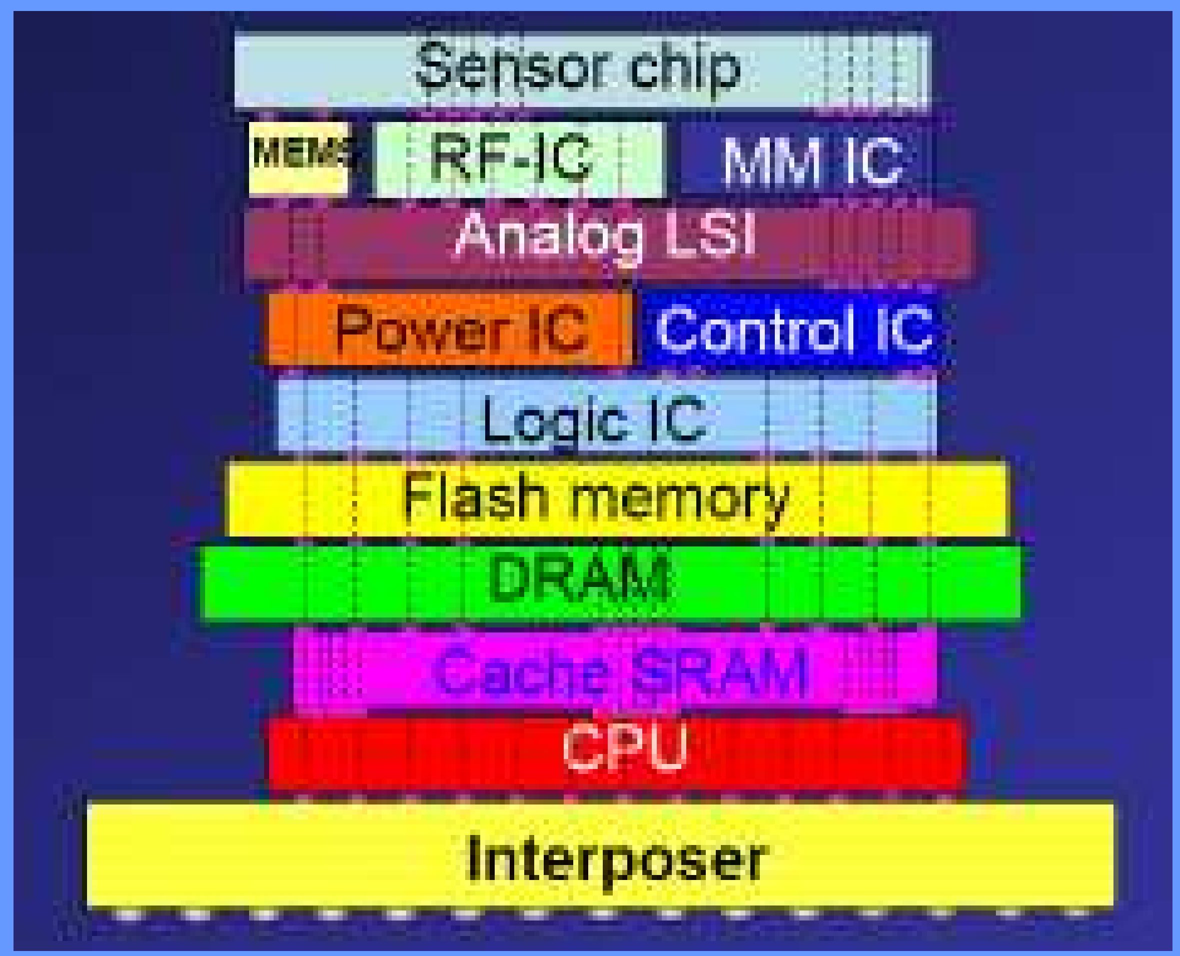
INTERCONNECT and PACKAGING CENTER

an SRC Center of Excellence at Georgia Tech

Overview

- 3D Integration
- CAD Research
- Transferring tools to Industry
- Summary

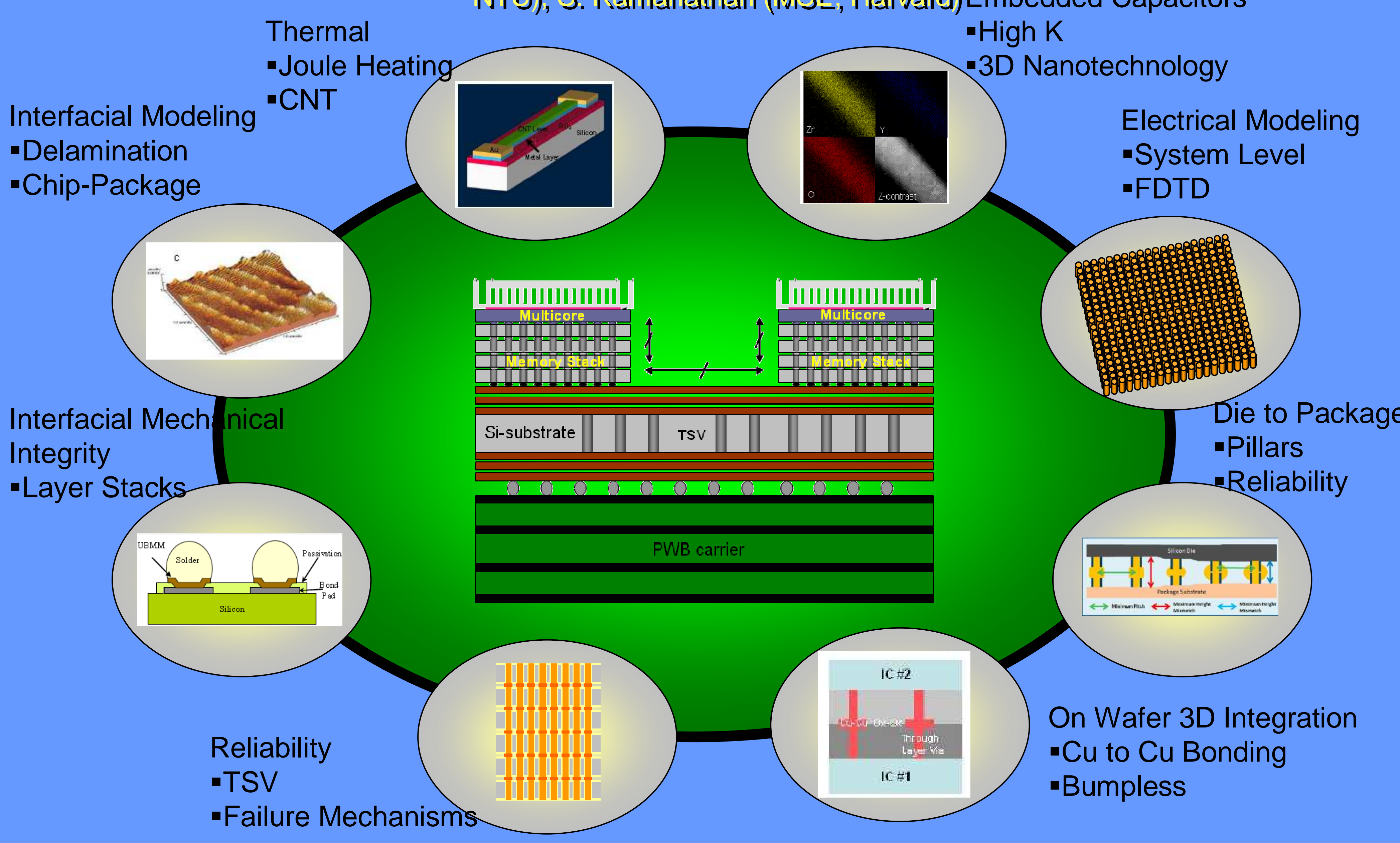
IPC Technical Focus and Vision



IPC is a multi-university center supported by SRC with research focus on 3D Technologies, positioning GT to become the academic hub for 3D IC technology innovation, exploration, and discoveries

Multi-disciplinary and Multi-university Program

Faculty: Y. Joshi (ME, GT), S. Sitaraman (ME, GT), M. Bakir (ECE, GT), Paul Kohl (ChE, GT), M. Swaminathan (ECE, GT), R. Huang (ME, UT Austin), A. Bastowros (AE, Iowa State), C. Seng Tang (ECE, NTU), S. Ramanathan (MSE, Harvard)

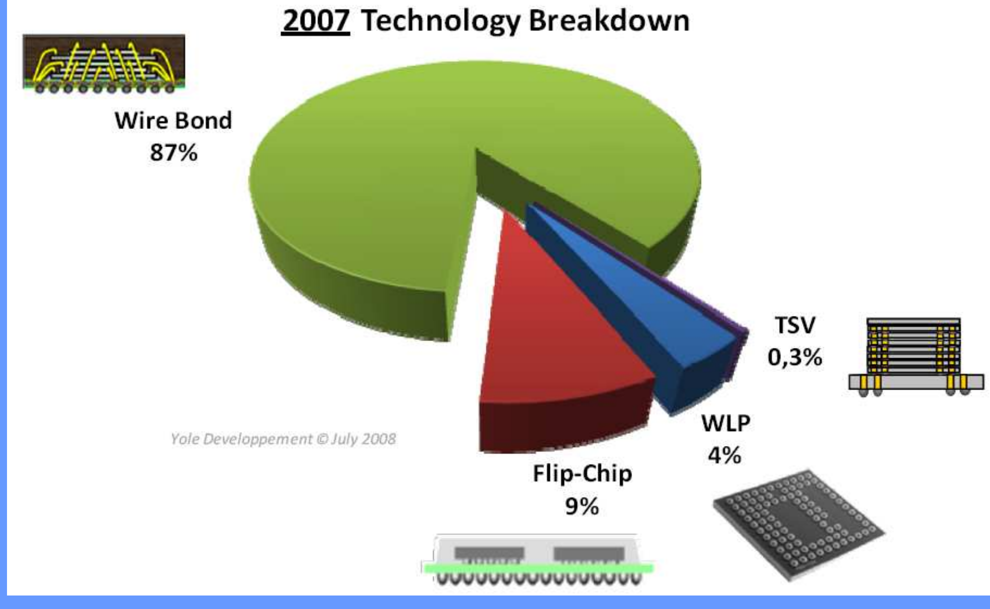


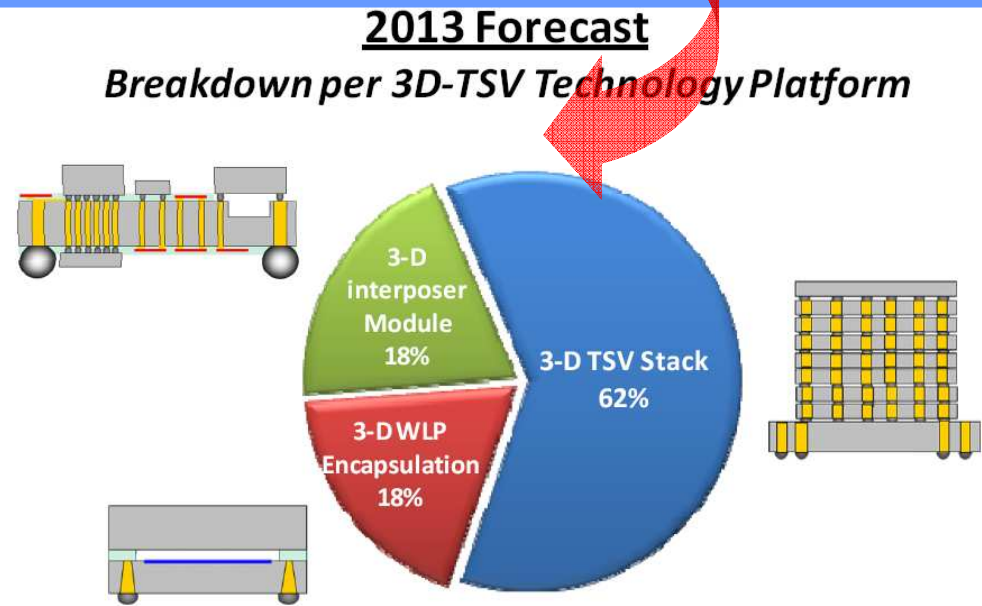
3D Technology Impact Forecast

3D-TSV Technologies Impact on Semiconductor business *(in wafers to be processed)*

Yole Developpement © July 2008

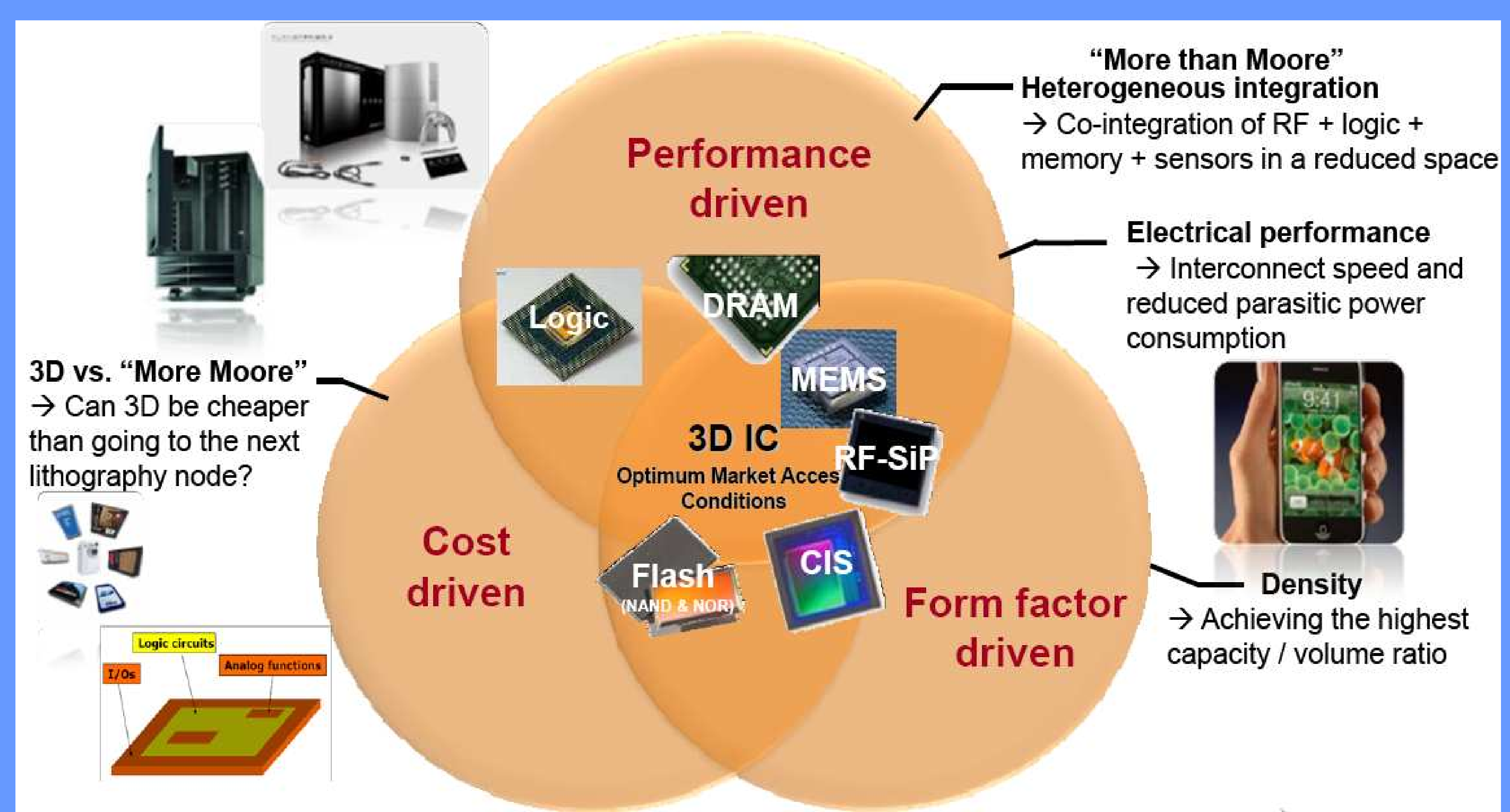
Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Share	0,4%	0,4%	0,6%	0,9%	1,4%	2,7%	4,5%	7,0%	9,9%	14,0%





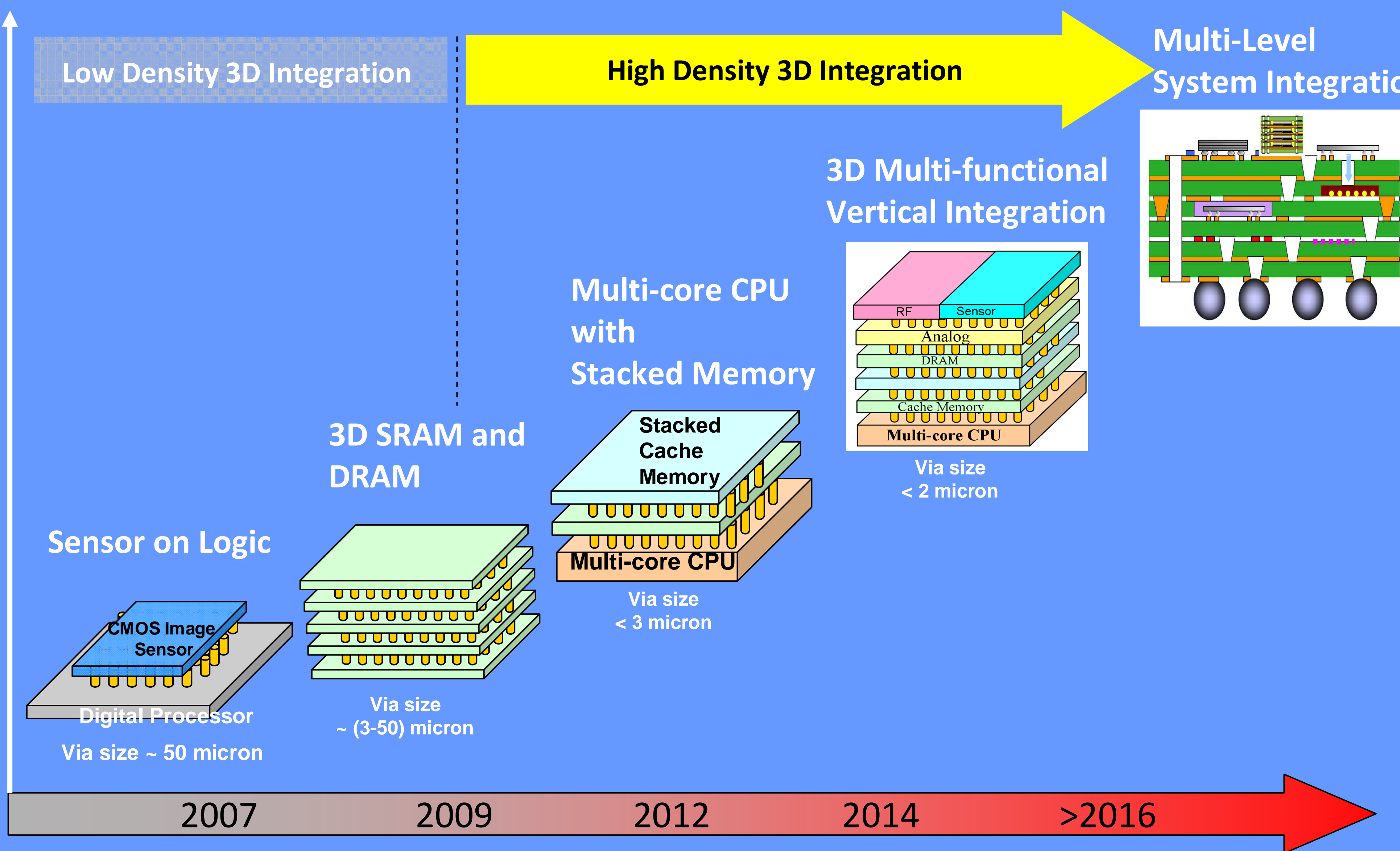
Courtesy : Yole Développement

Why 3D?
3D Integration Market Drivers



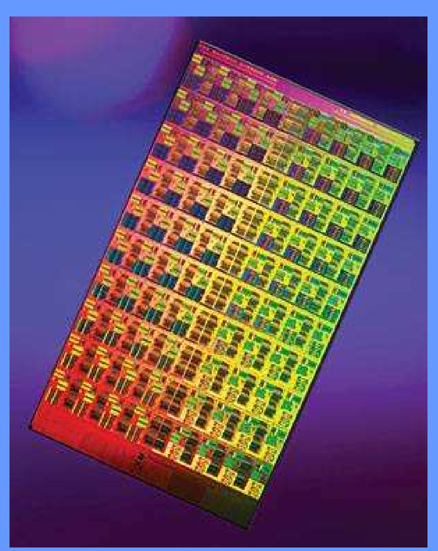
Courtesy : YOLE DÉVELOPPEMENT

3D Roadmap

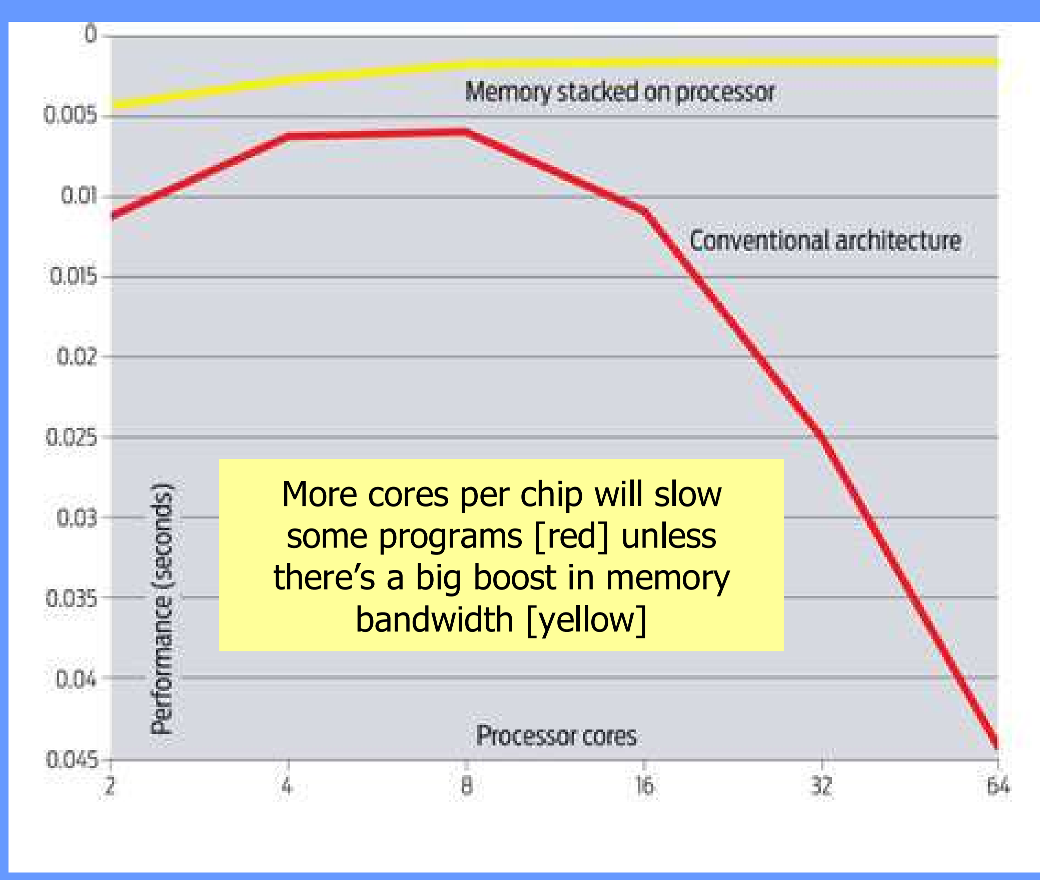


* Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits, Volume 2, edited by Philip Garrou, Christopher Bower, Peter Ramm
* SiP White Paper V9.0
* P. Leduc, "What is 3d IC integration and what metrology is needed," in Conference on Frontiers of Characterization and Metrology for Nano electronics, Mar. 2007.

Overcoming the Memory Wall
Power of the 3D Interconnect



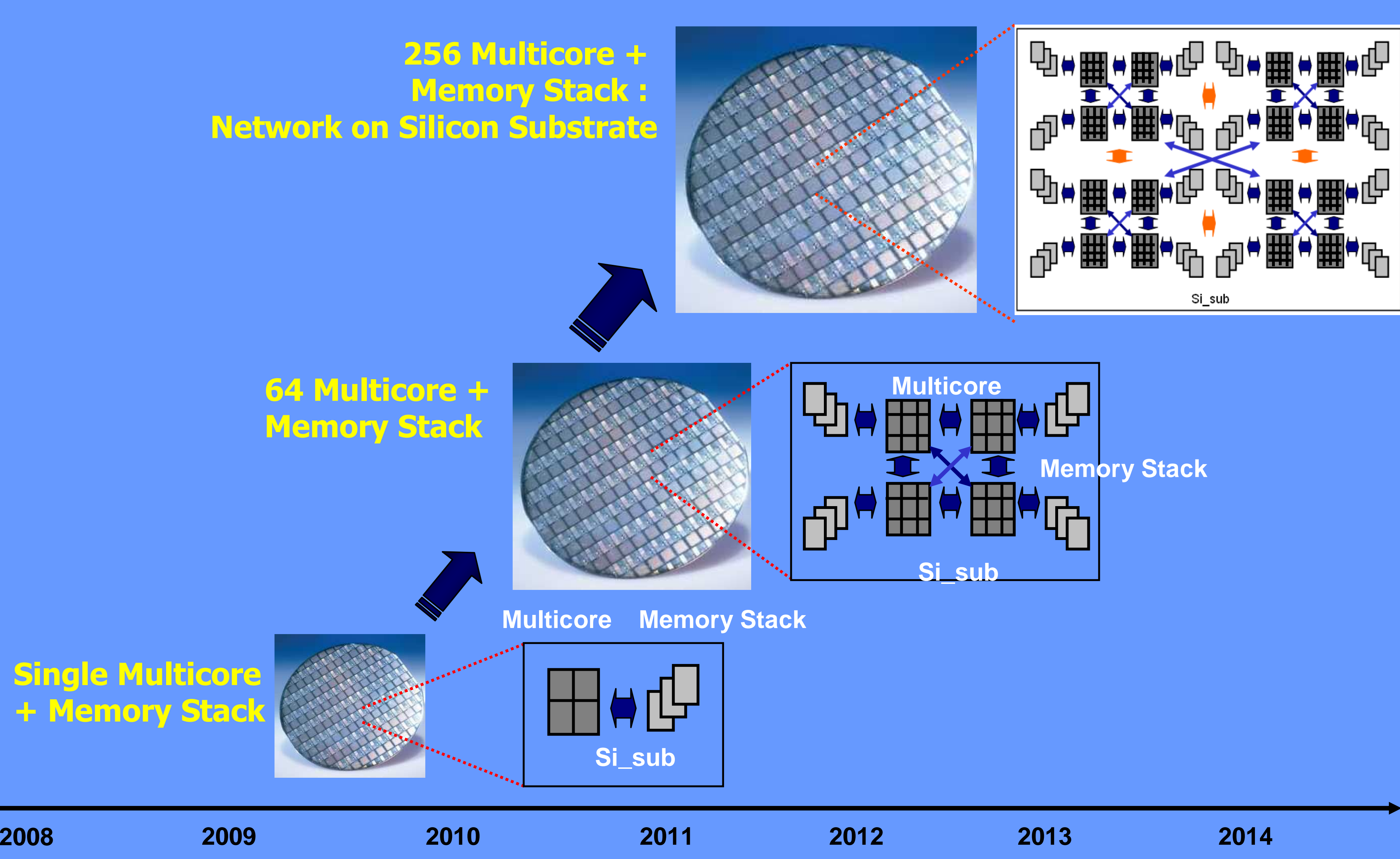
THE FUTURE: Intel's experimental chip has 80 cores.



Overcoming memory wall using shorter distance and higher density 3D interconnect

Ref : IEEE Spectrum Nov. 2008

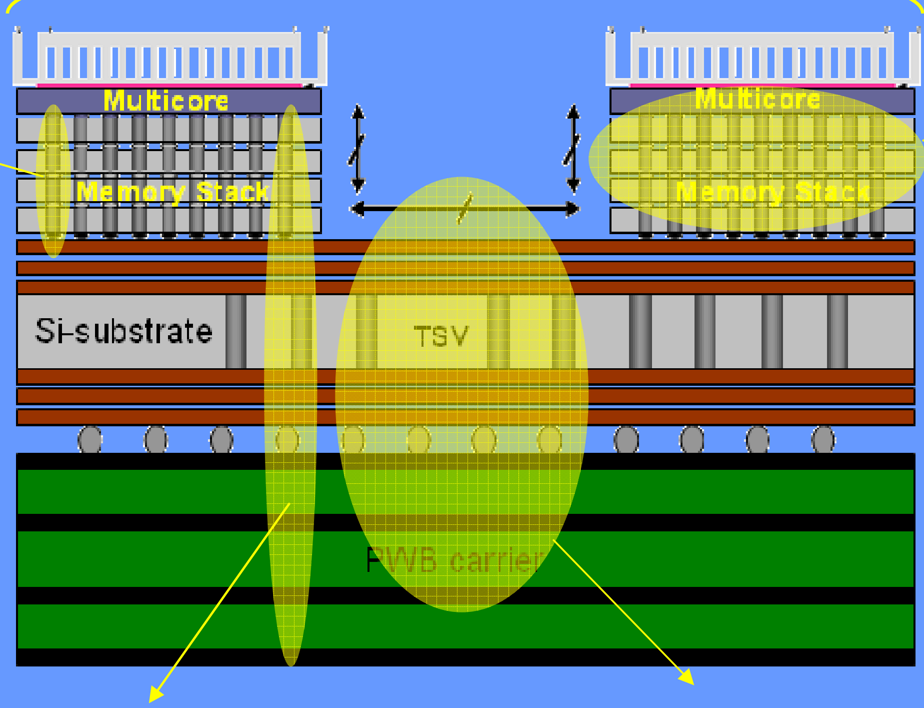
3D Multi-core System Evolution



3D Interconnect Design Research Opportunities

3D Thermal-Electrical Design
- Thermal-electrical effect in 3D integration
- DC power drop including conduction and convection mode

3D Interconnect (TSV) Modeling and Characterization
- Multiple TSV coupling
- Variable capacitance
- Signal/power optimized TSV design

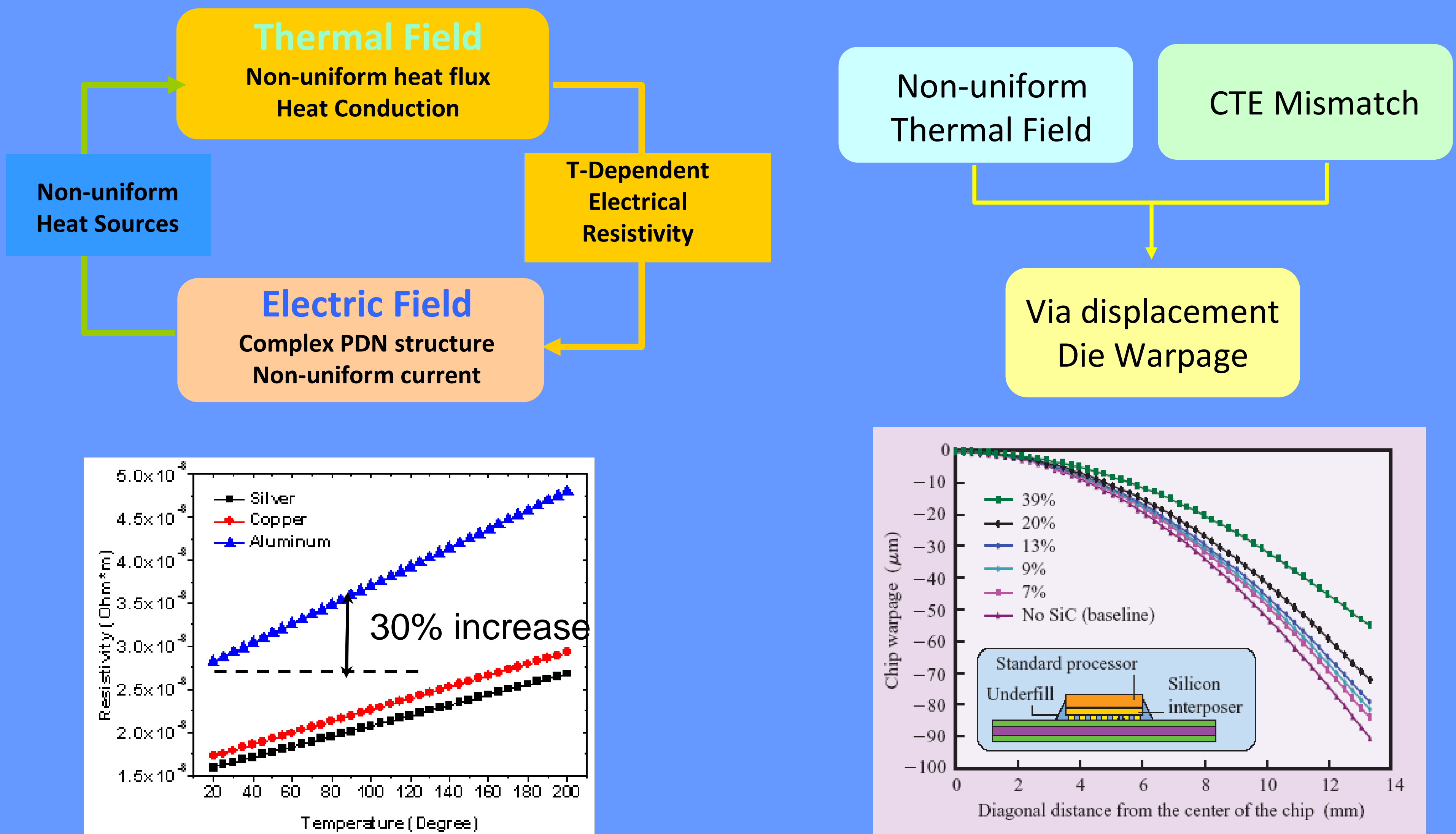


3D Clock Distribution
- Driving 10^5 I/Os with low jitter low skew
- Vertical clock distribution using TSV array

3D Power Delivery
- DC drop by TSV loss
- Power noise coupling through TSV
- TSV filter & TSV Decap

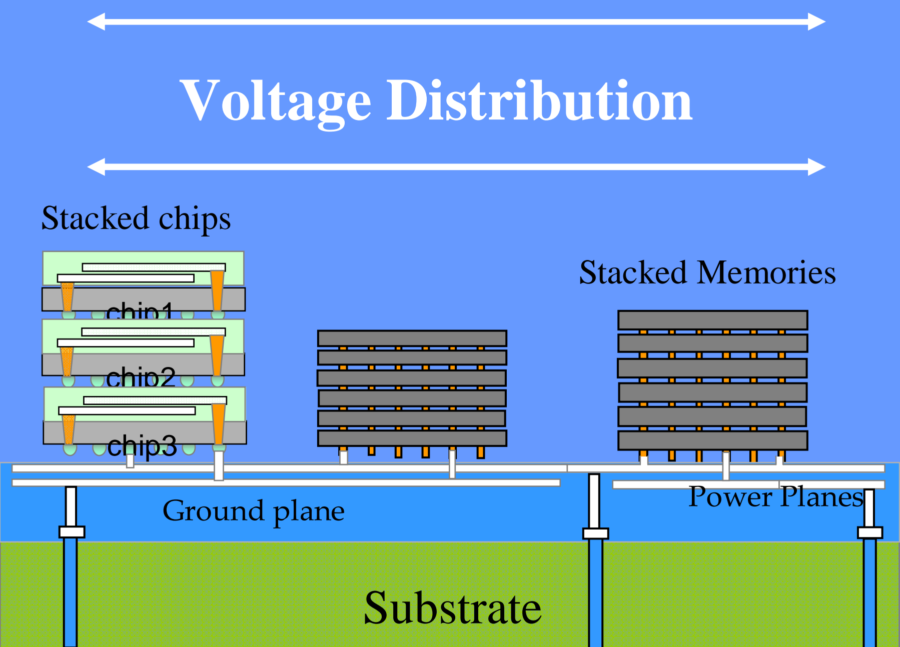
3D Signaling
- Power through the transmission line
- VRM & TSV capacitor in Si-substrate
- Removing power supply plane

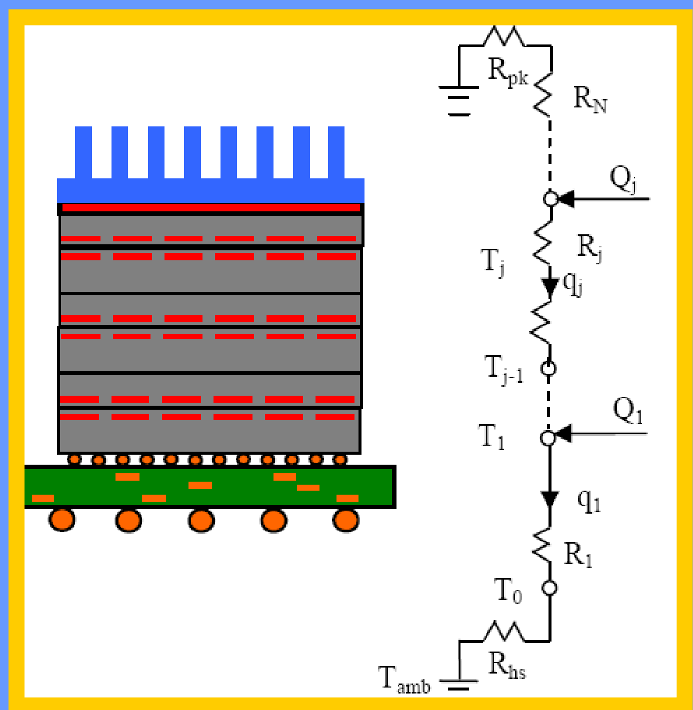
Electrical-Thermal-Mechanical Multi-physics Design in 3D



* J. Xie, D. Chung, M. Swaminathan, M. Mcallister, A. Deutsch, L. Jiang, B. J Rubin, “Electrical-thermal co-analysis for power delivery networks in 3D system integration,” IEEE International Conference on 3D System Integration (3DIC), Sept. 2009.
* S. M. Sri-Jayantha, “Thermomechanical modeling of 3D electronic packages,” IBM Journal of Research and Development, vol. 52 , no.6, Nov. 2008.

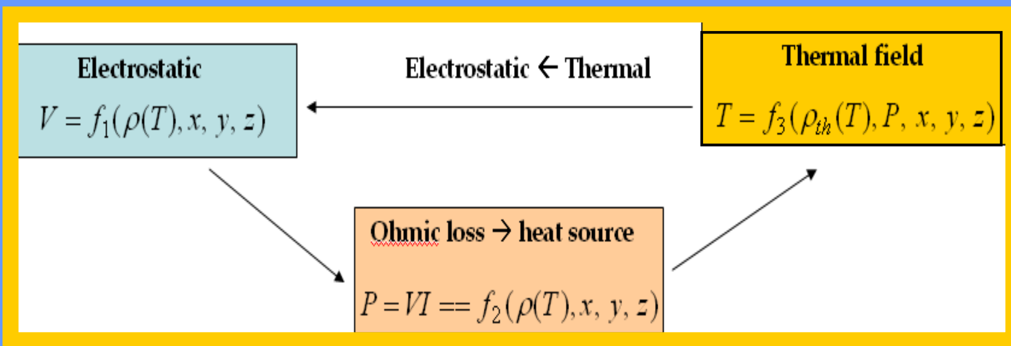
Need for Thermal-Electrical Co-Design

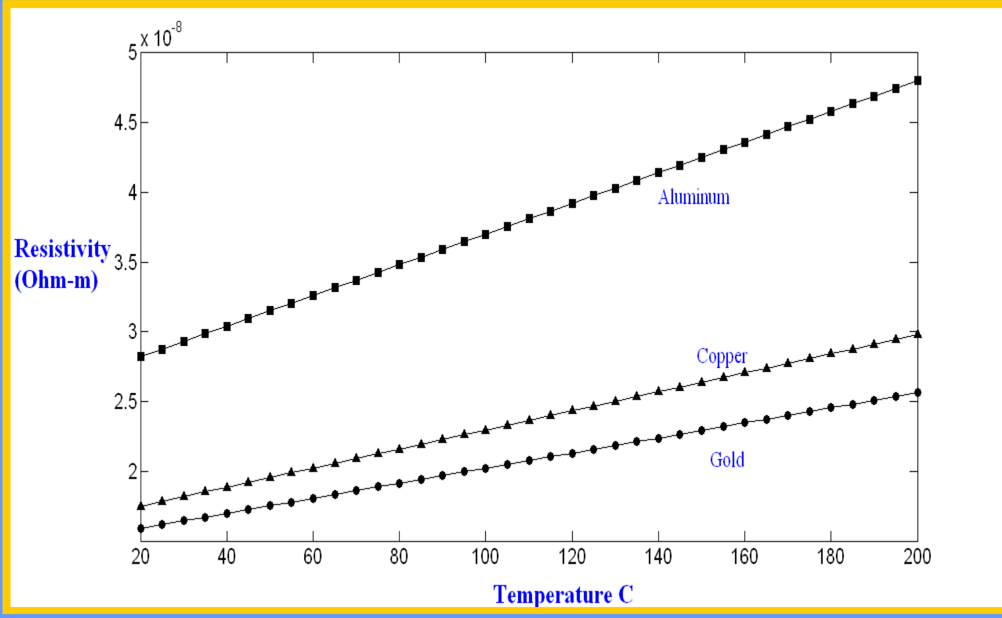


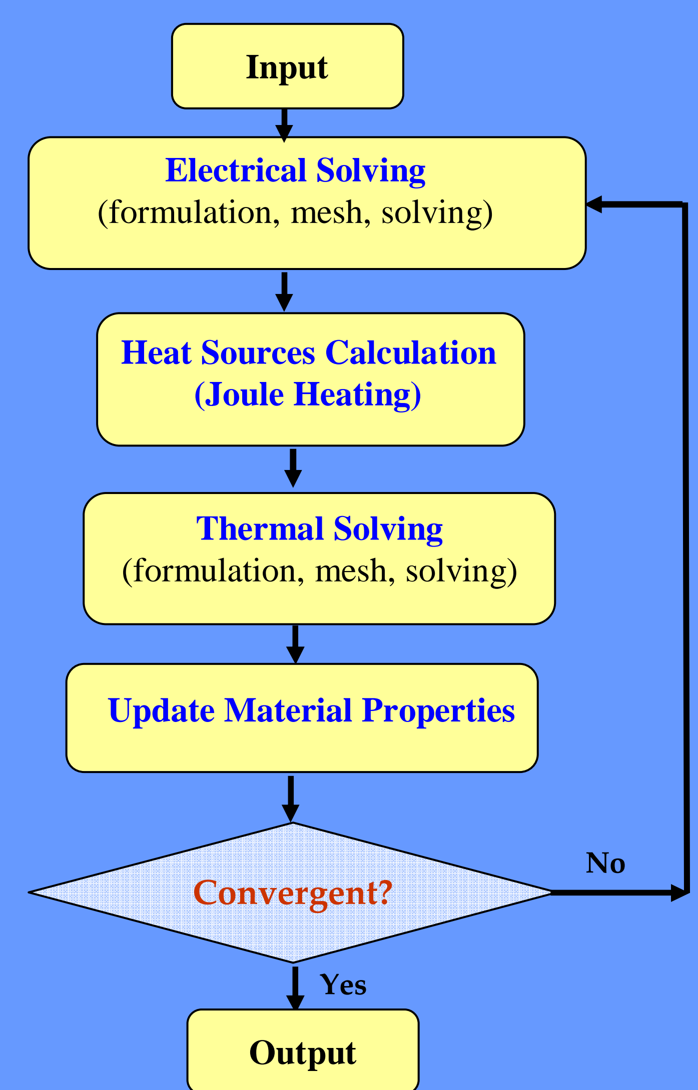


- Increasing heat flux density in 3D
- Affects power delivery
- Thermal – Electrical Interaction

Importance of Joule Heating

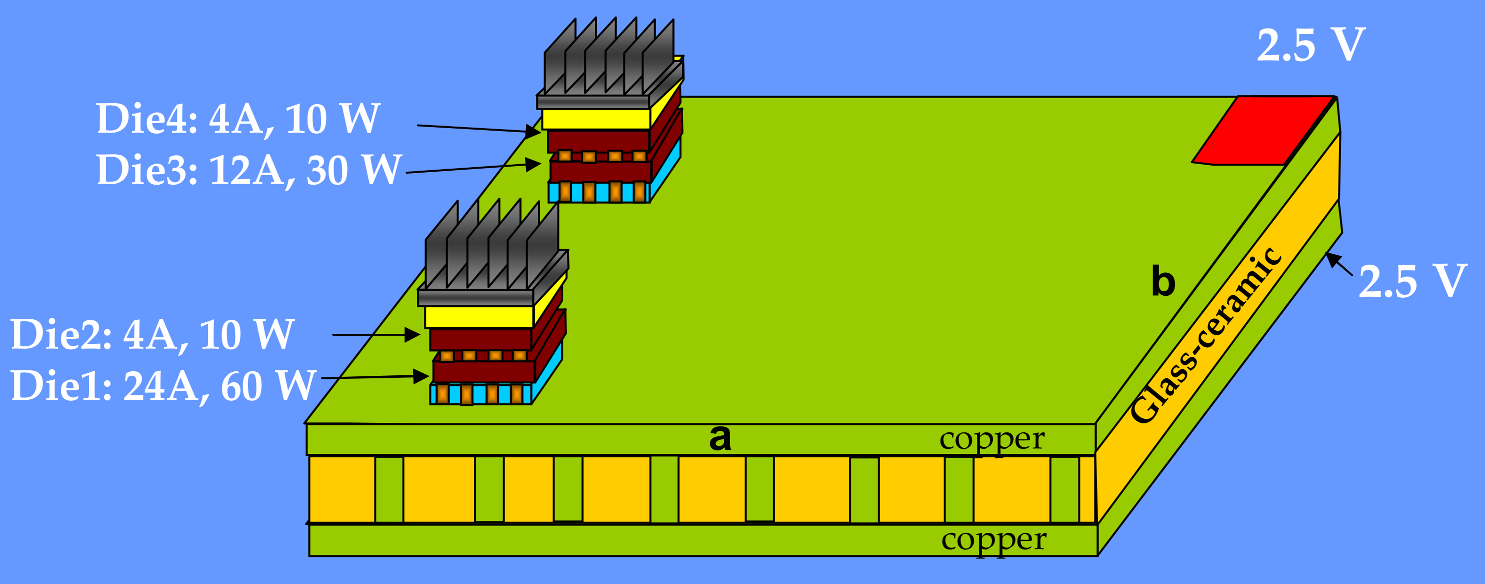




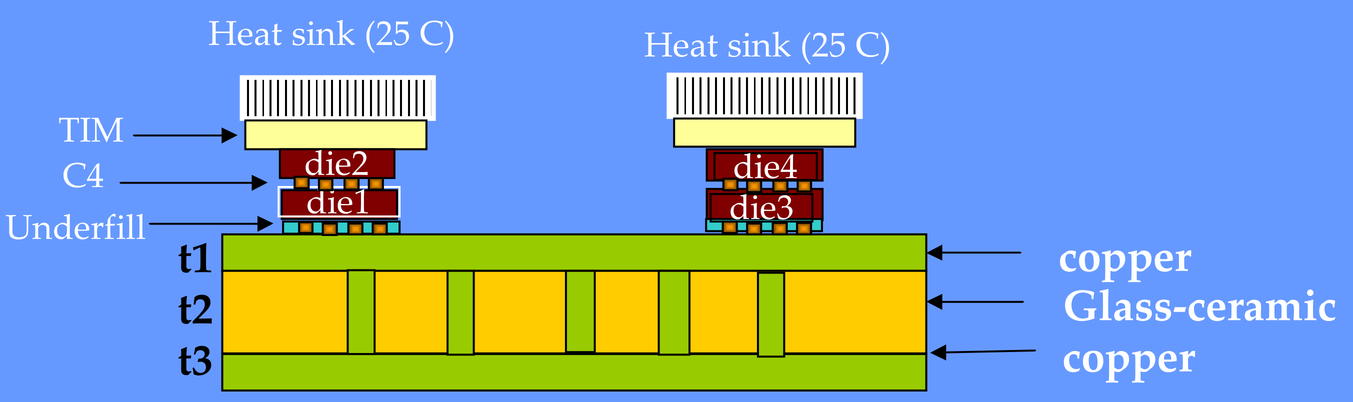


- Thermal profile causes change in material resistivity which changes DC drop

3D Thermal-Electrical Design
An Example



Cross section view:



Geometry Parameters:

a= 20 cm, b= 20 cm
t1 = 36 micron
t2 = 350 micron
t3 = 36 micron
t_tim = 200 micron
t_die = 500 micron
t_underfil = 200 micron

Electrical Resistivity:

$$\rho_{C4_Sn-0.7Cu} = 15e-8\ \Omega \cdot m$$

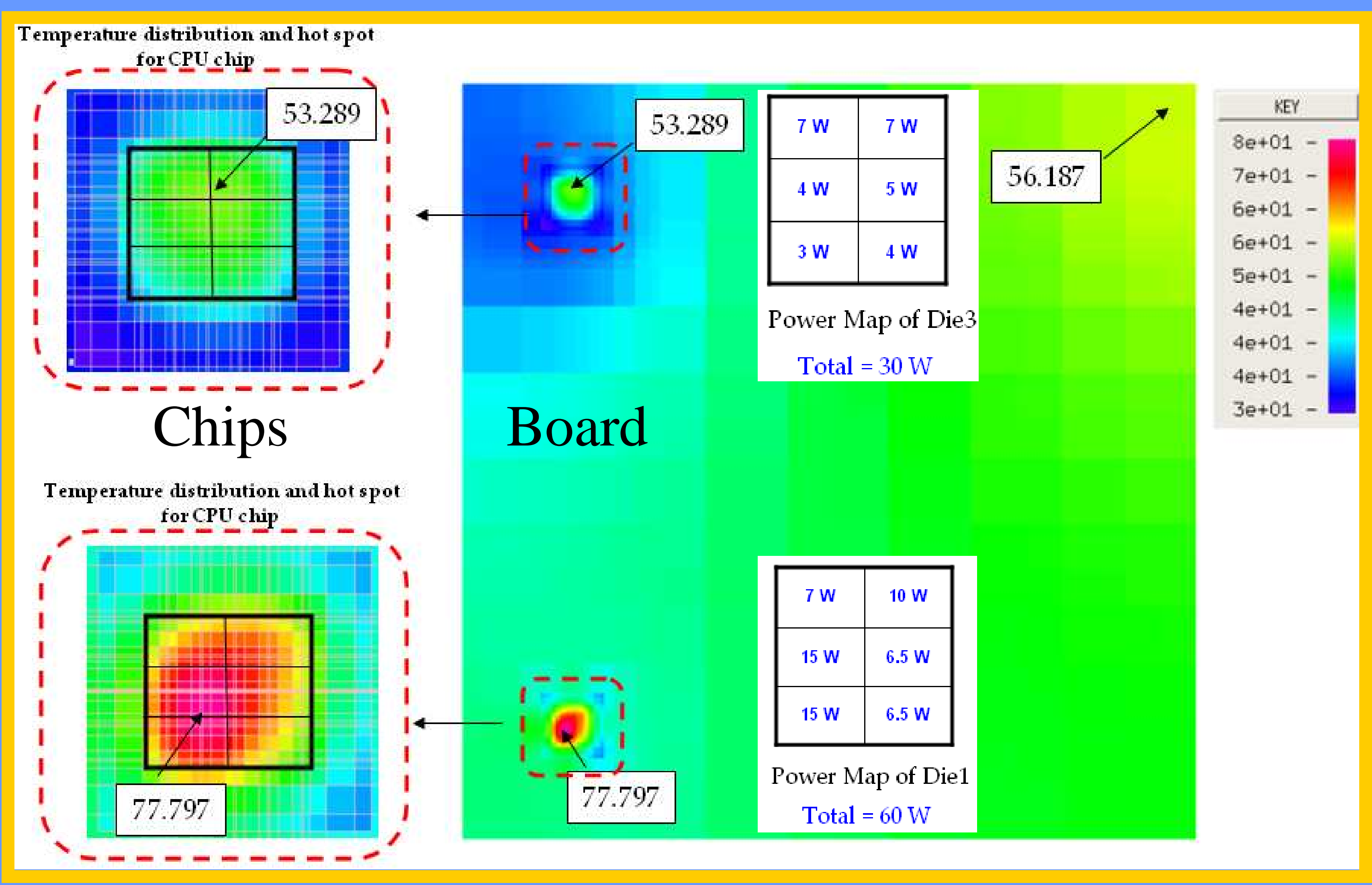
$$\rho_{Cu} = 1.8e-8\ \Omega \cdot m$$

$$\rho_{Tungsten} = 5.6e-8\ \Omega \cdot m$$

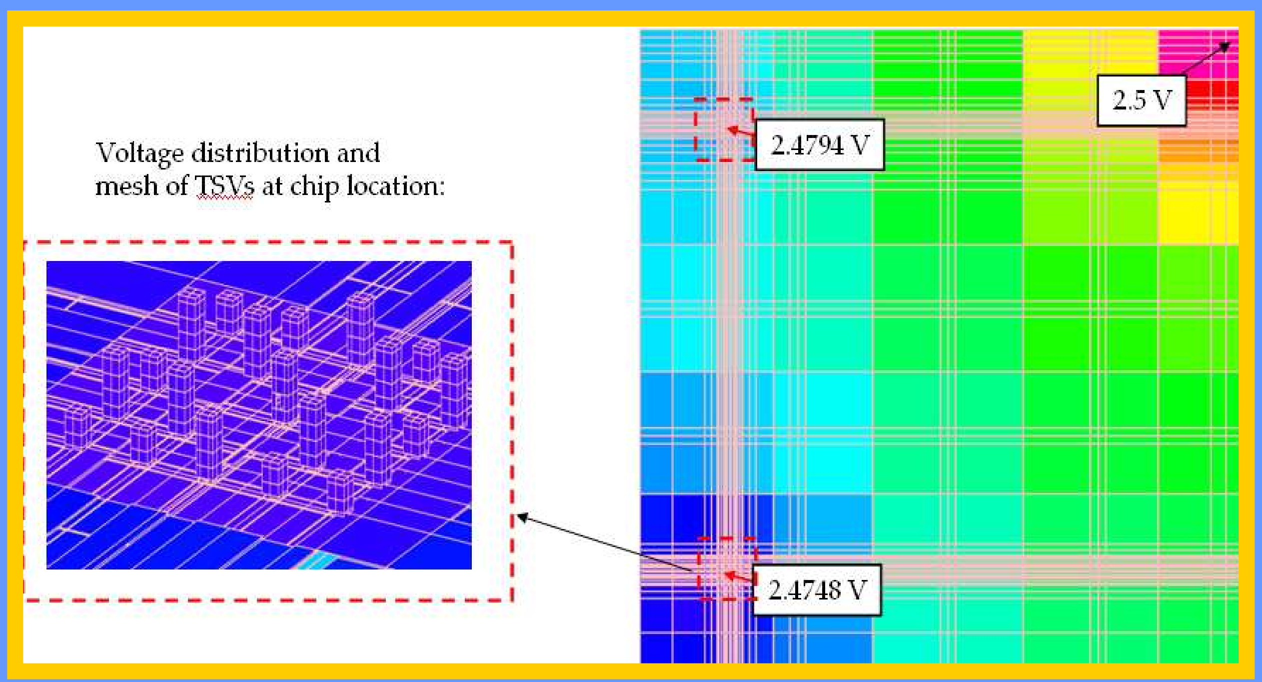
Thermal conductivities:

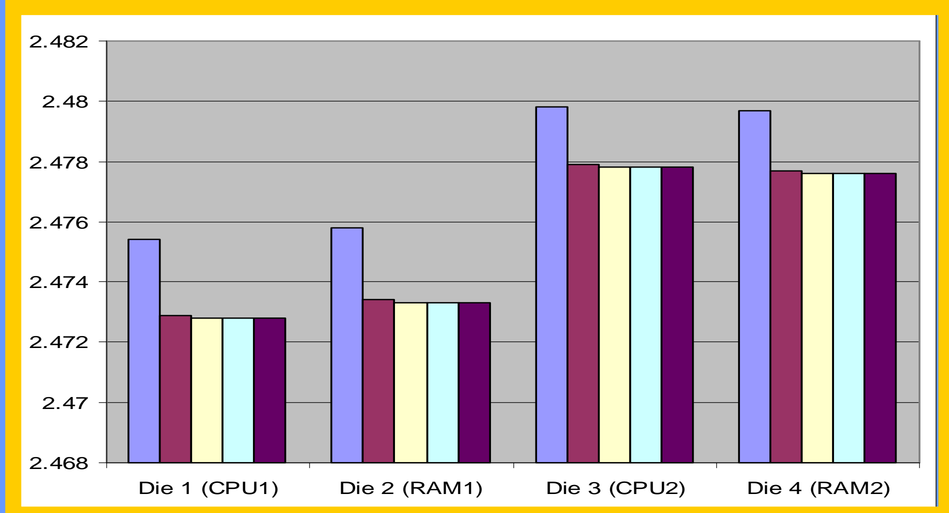
K_tim = 2 W/m-K
K_die = 110 W/m-K
K_underfil = 4.3 W/m-K.
K_glass-ceramic = 5 W/m-K
K_C4 = 40 W/m-K

Thermal Profile



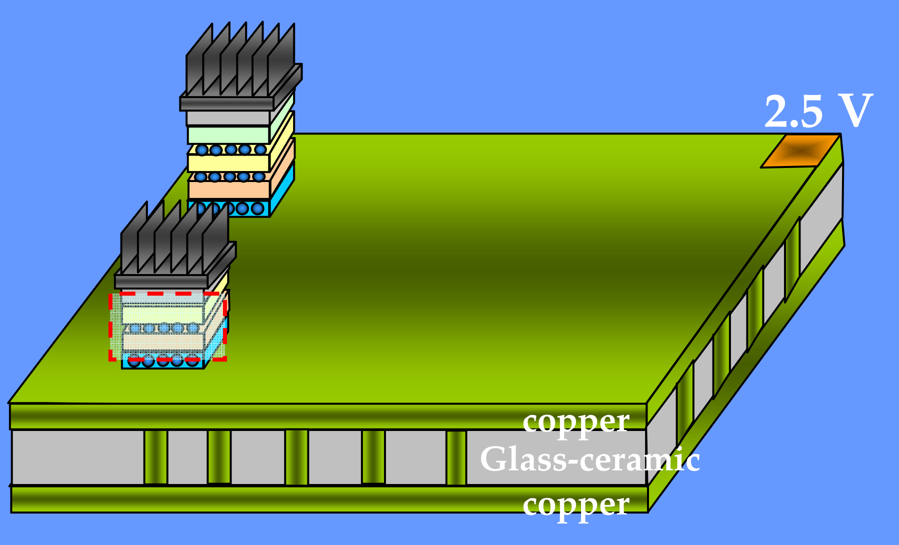
DC Drop Variation

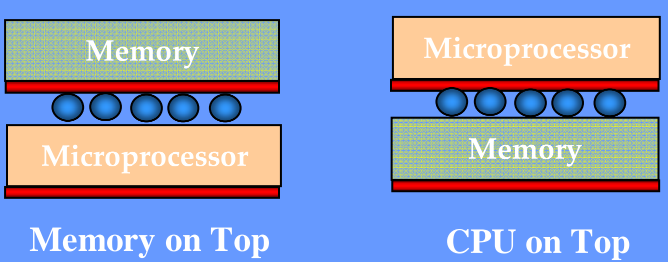




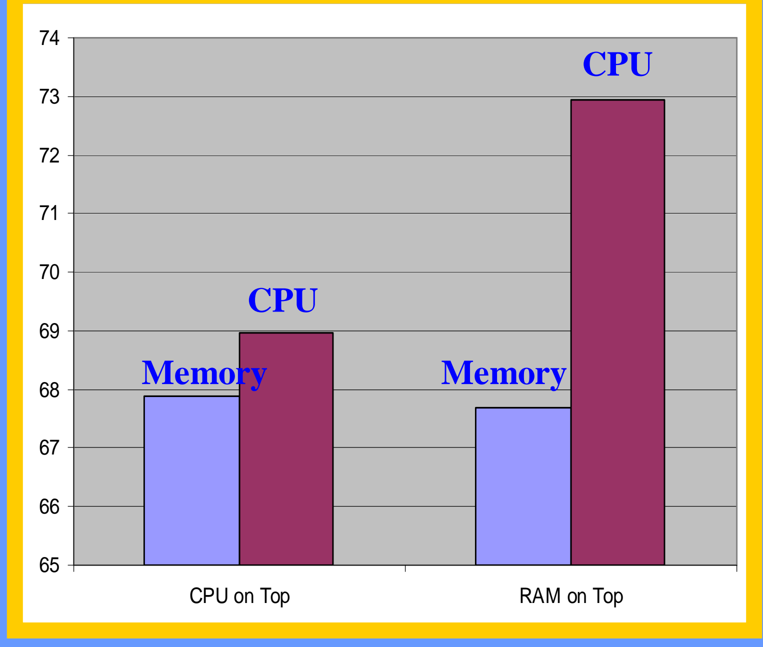
Increased DC due to Joule heating effect

Stacking Order : Which is better ?





Hot spot analysis



- CPU on top has lower hot spot (as expected)
- Does this lead to acceptable DC drop ?

Buffer Sizing with TSV

Without TSV

p/n=8/4um

in

out

p/n=8/4um

p/n=8/4um

With TSV

in

TSV

(Large capacitive TSV)

out

p/n=8/4um

p/n=8/4um

in

out

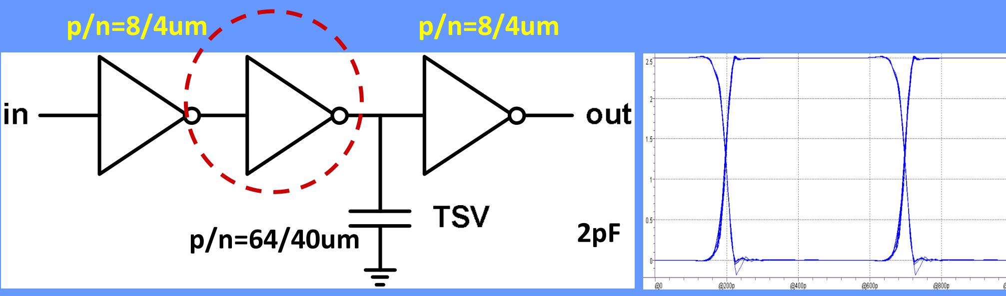
p/n=8/4um

TSV

2pF

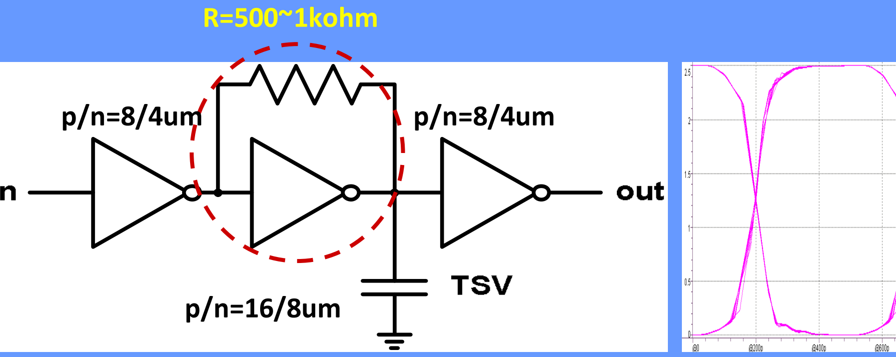
Driving VC-TSV can corrupt signal

Large Buffer



Large buffer consumes area &power

Small Swing Buffer

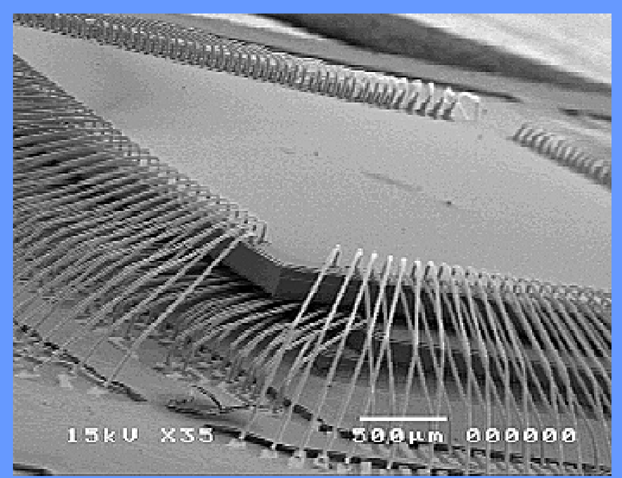


Small swing buffer consumes less area and less power

3D Interconnections

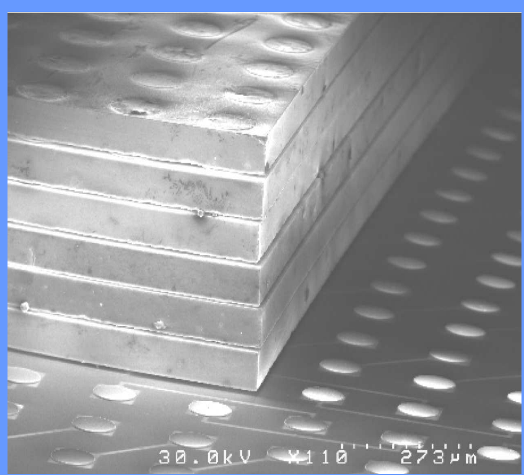
❑ Bonding wires

(courtesy of Amkor Technology, Inc.)

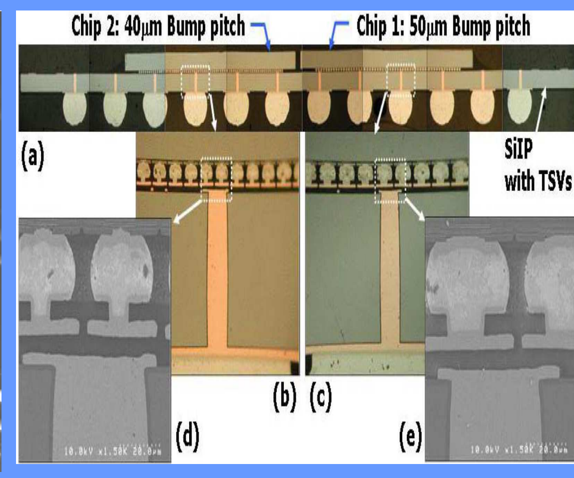


❑ TSVs

(J.U. Knickerbocker et al., ECTC 2008)



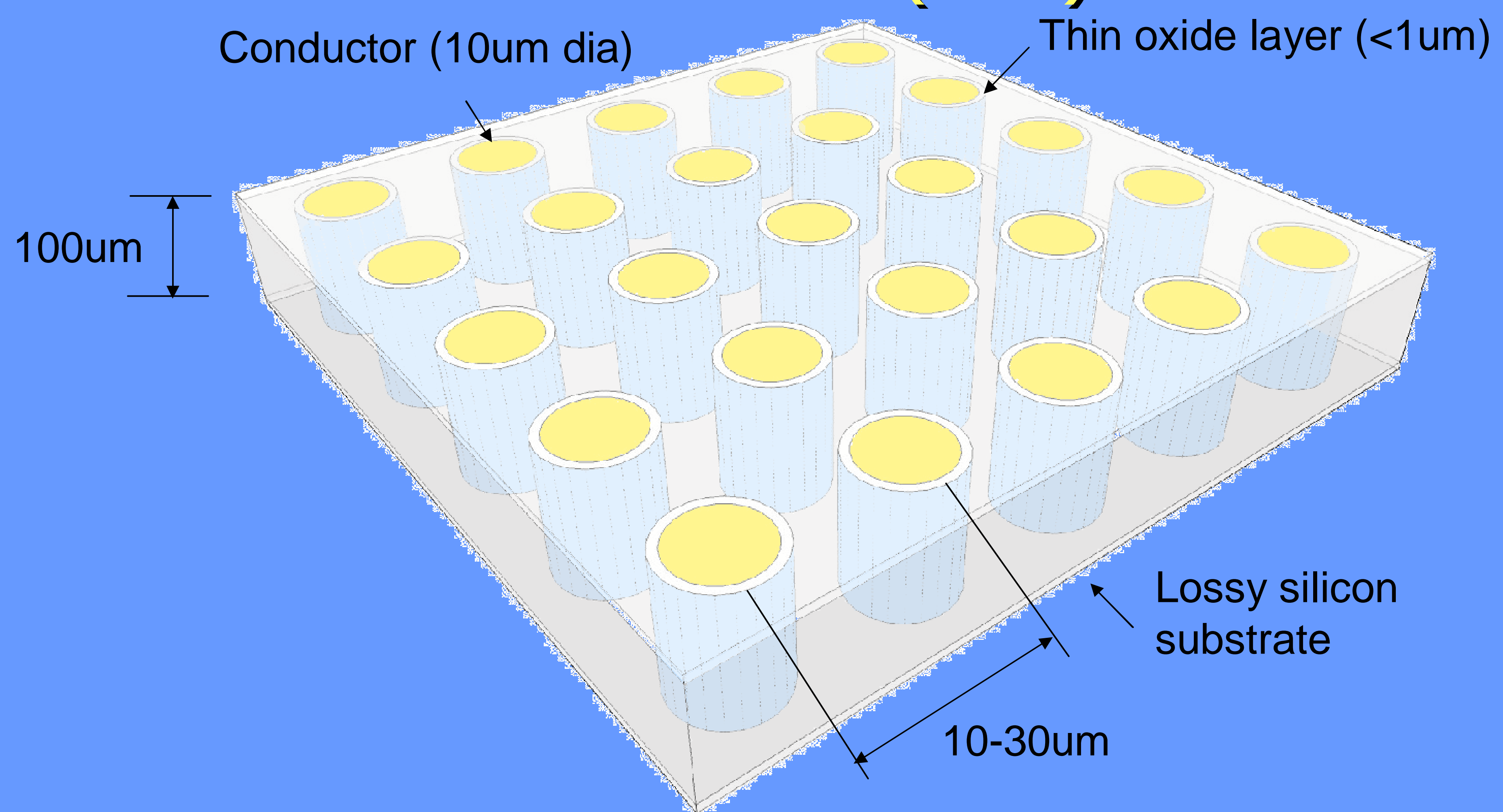
(K. Kumagai et al., ECTC 2008)



Objective

Developing an efficient method to extract broadband parasitics of 3-D interconnection structures including TSVs

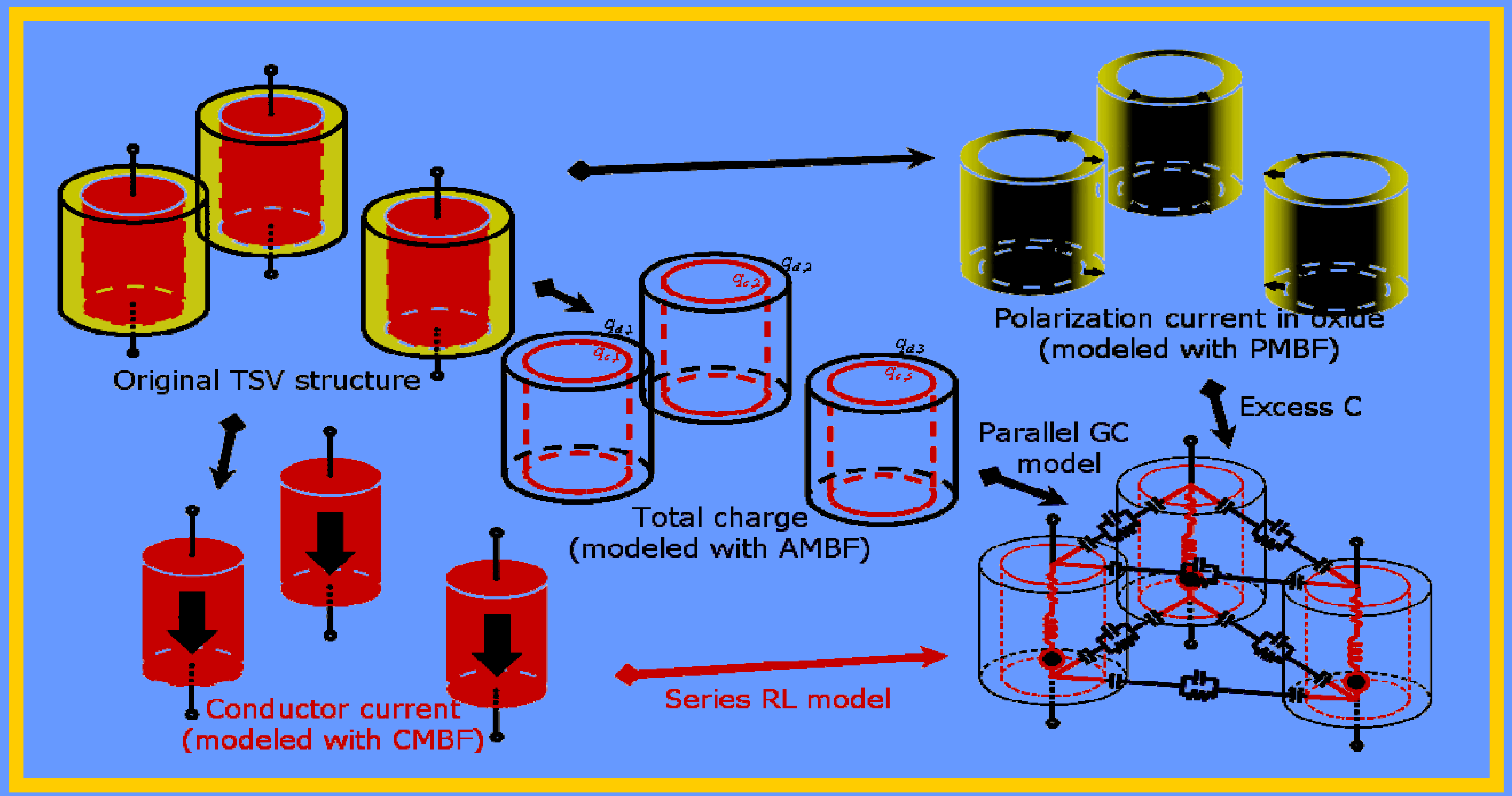
Rapid Electromagnetic Modeling of Through Silicon Vias (TSV)



Number of coupled vias can be large

Commercial EM Tools will have trouble due to the aspect ratio of these structures

Modeling Concept



❖ **Using global modal basis functions reduces the required number of basis functions.**

- **Free from the inefficient mesh issue.**
- **Computational cost to model a large number of TSVs is considerably reduced.**

Modeling of Current and Charge

$$\frac{\vec{J}(\vec{r},\omega)}{\sigma}+j\omega\frac{\mu}{4\pi}\int_{V'}G(\vec{r},\vec{r}\,')\vec{J}(\vec{r}\,',\omega)dV'=-\nabla\Phi(\vec{r},\omega)$$

IE with vector potential

$$\vec{J}_j(\vec{r},\omega)\cong\sum_{n,q}I_{jnq}\vec{w}_{jnq}(\vec{r},\omega)$$

Approximate current using **cylindrical CMBF**

$$\vec{w}_{i0}=\frac{\hat{z}_i}{A_{i0}}J_0(\alpha(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i)$$

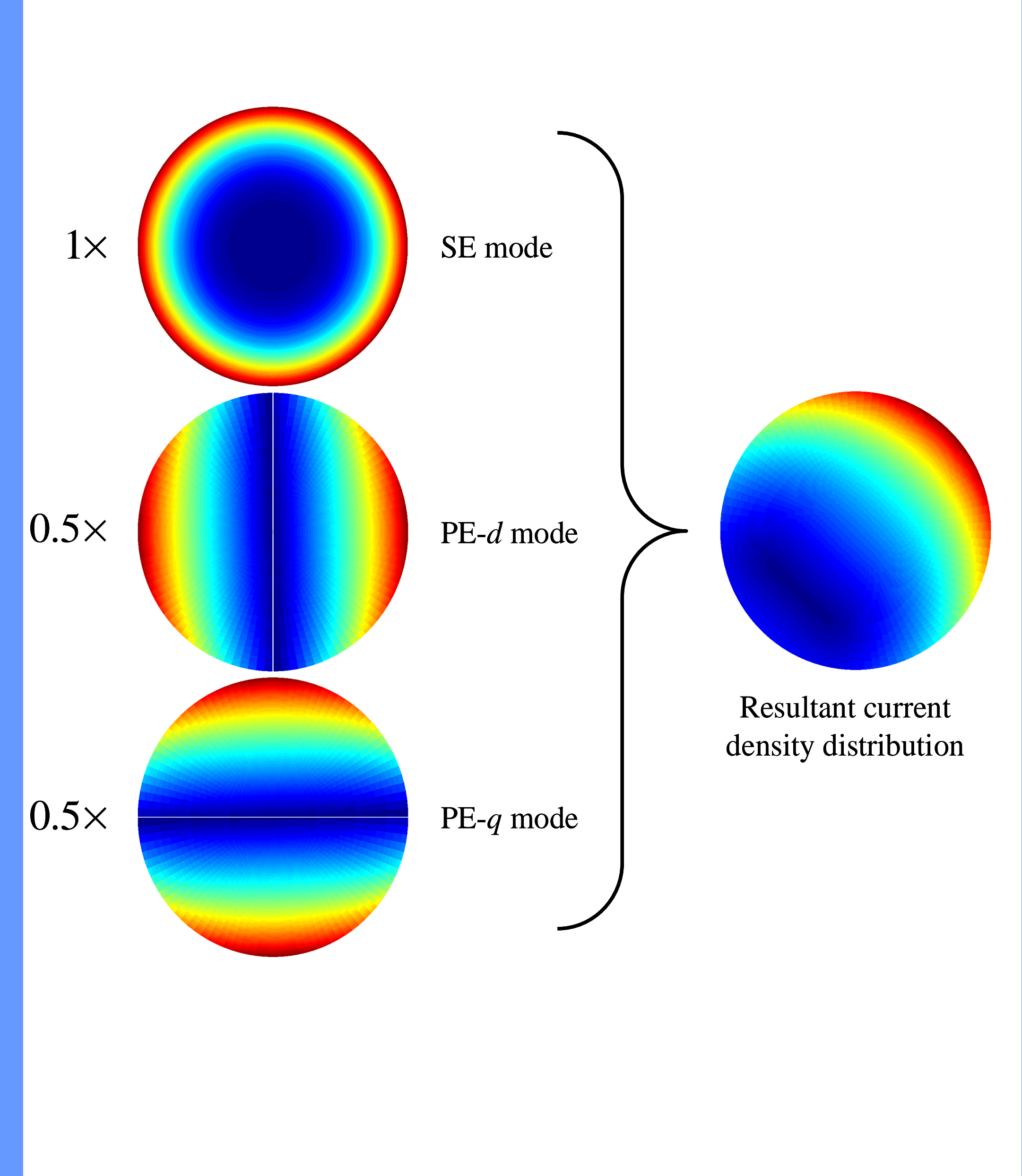
(SE mode)

$$\vec{w}_{in\{d,q\}}=\frac{\hat{z}_i}{A_{in}}J_n(\alpha(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i)\begin{Bmatrix}\cos(n\varphi_i)\\ \sin(n\varphi_i)\end{Bmatrix}$$

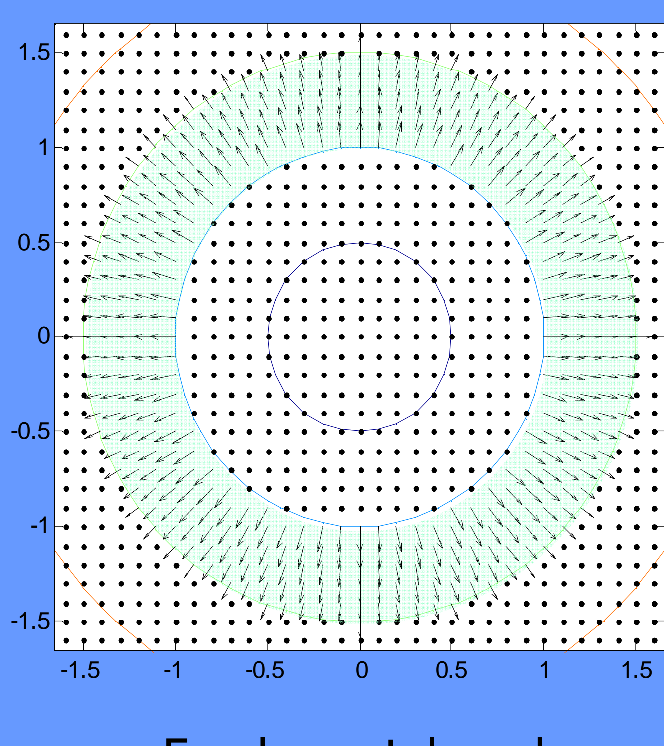
(PE mode)

$$\sum_{n,q}I_{jnq}R_{imd,jnq}+j\omega\sum_{n,q}I_{jnq}L_{imd,jnq}=\Delta V_{imd}$$

Voltage equation between two interconnect nodes

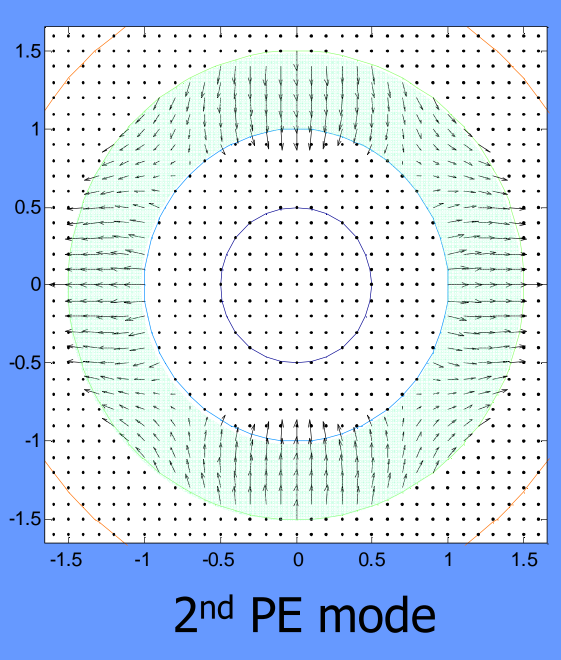


Cylindrical PMBFs for Modeling Thin Oxide

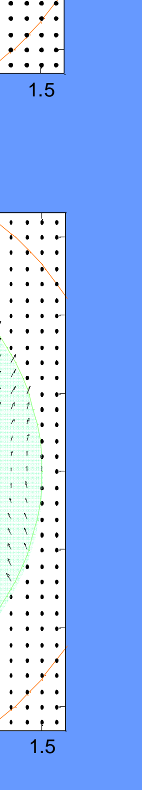


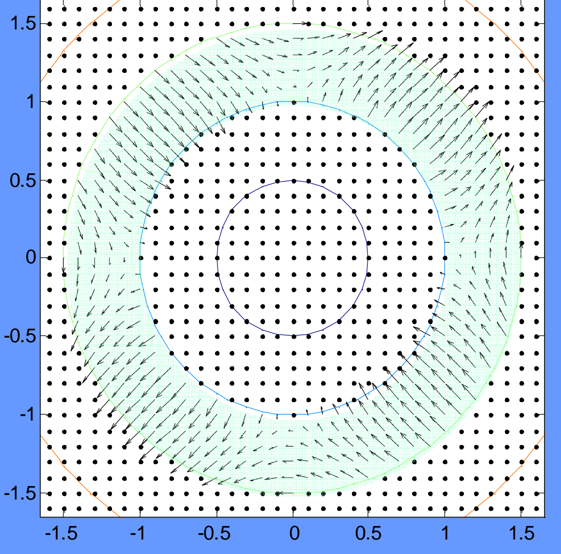
Fundamental mode

1st PE mode

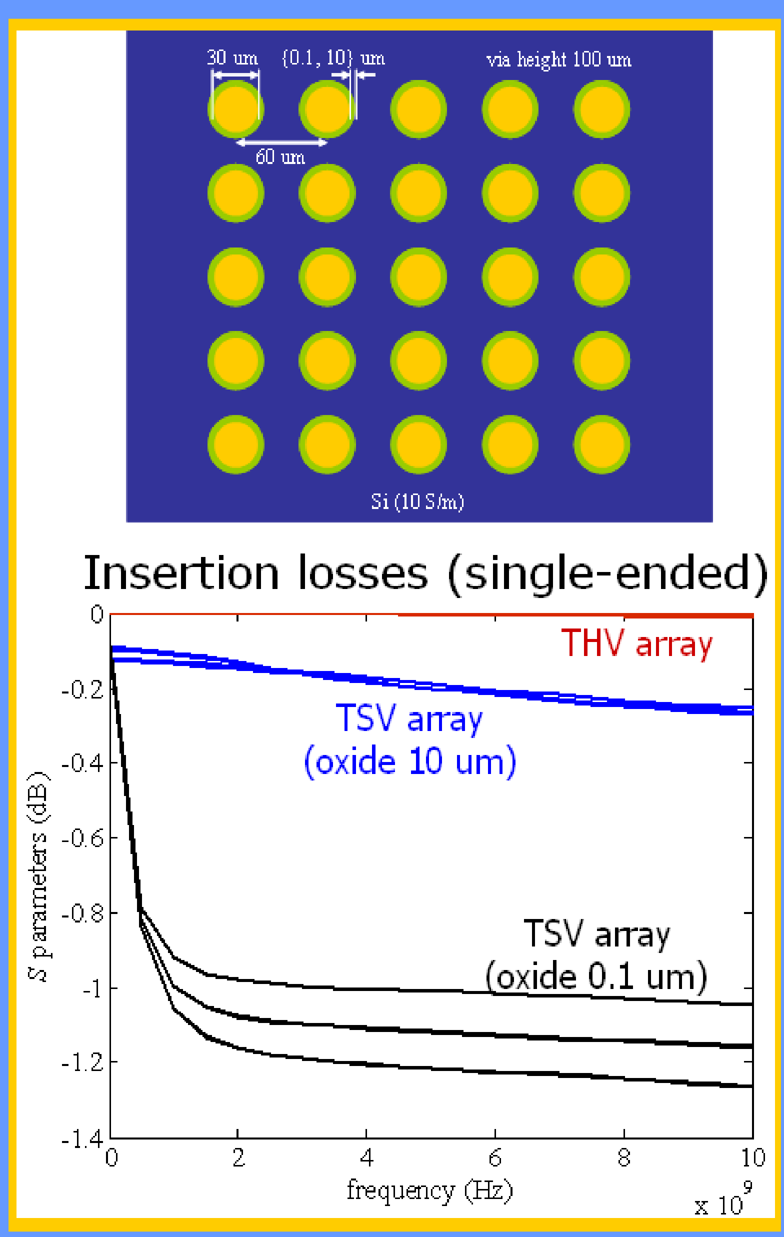


2nd PE mode

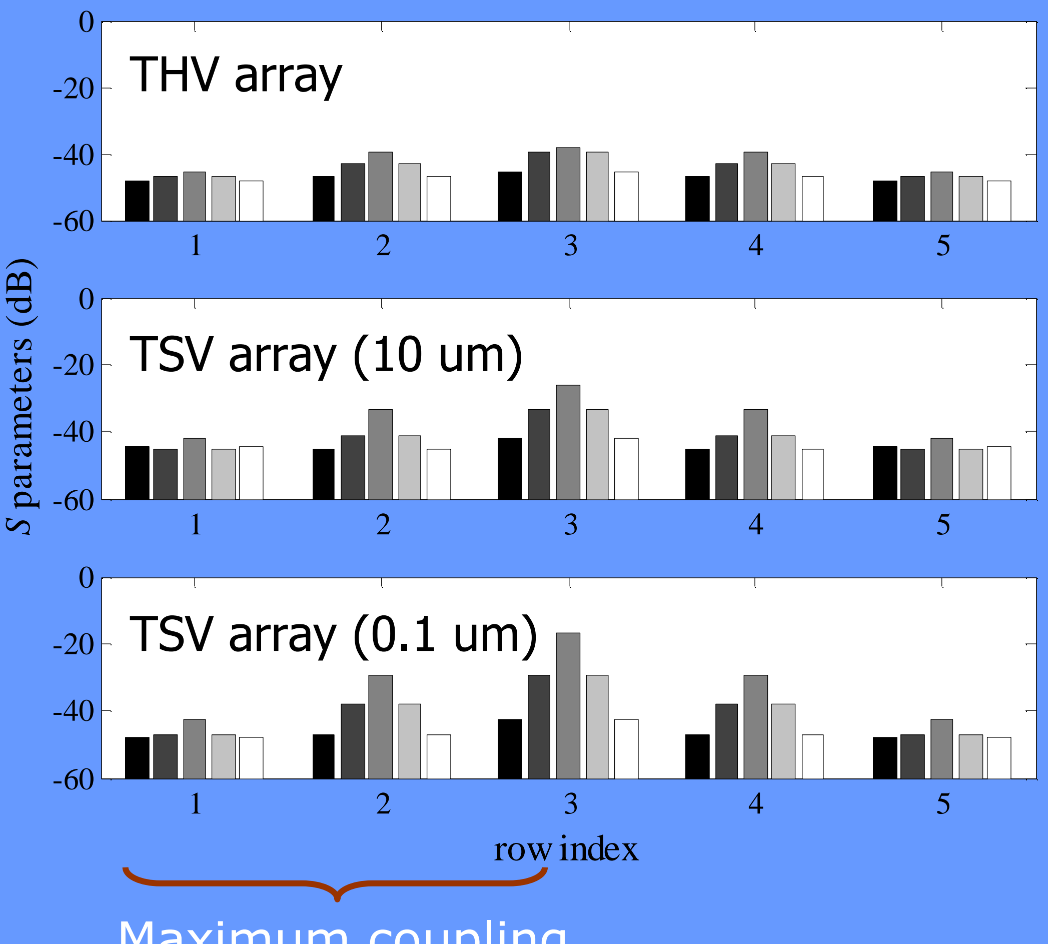




5x5 TSV Array

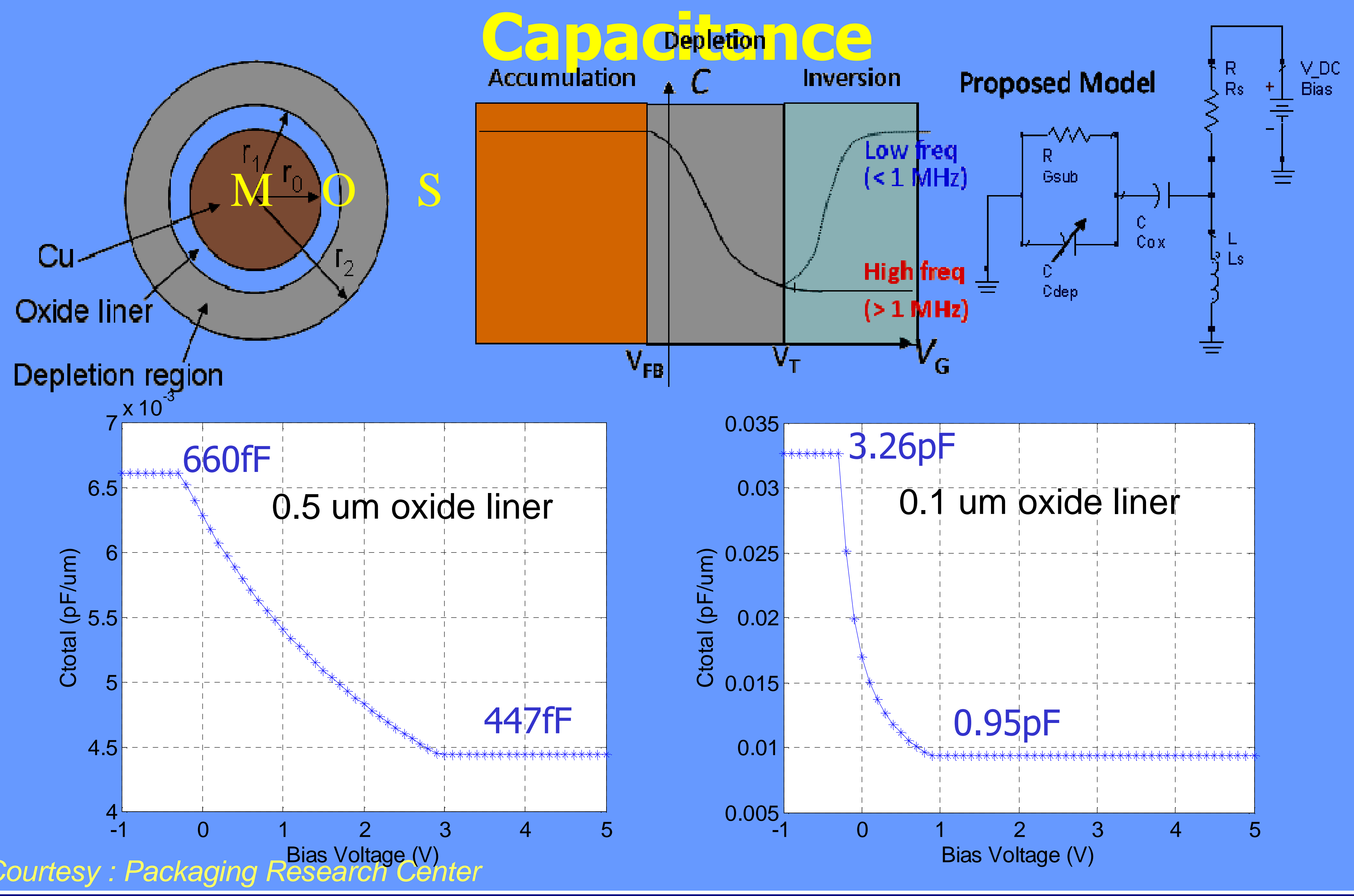


Near-end coupling to the center conductor at 10 GHz



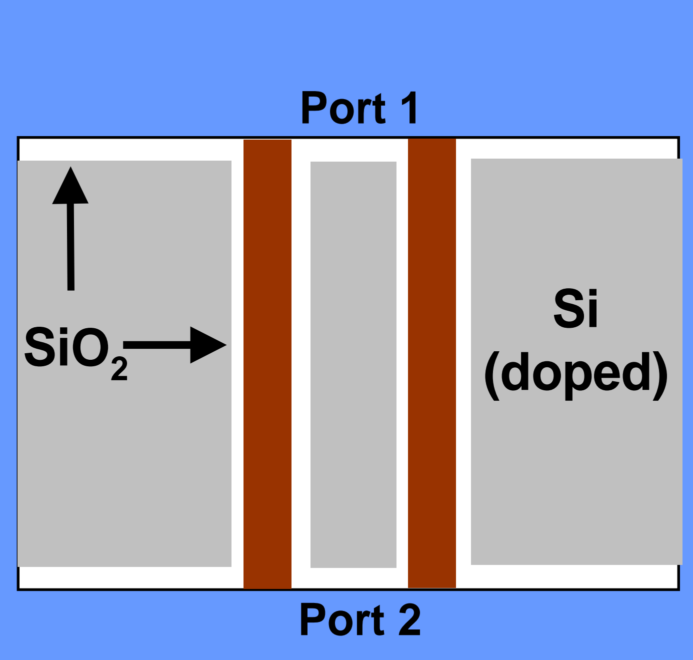
Maximum coupling level is about -29 dB when thin oxide is used.

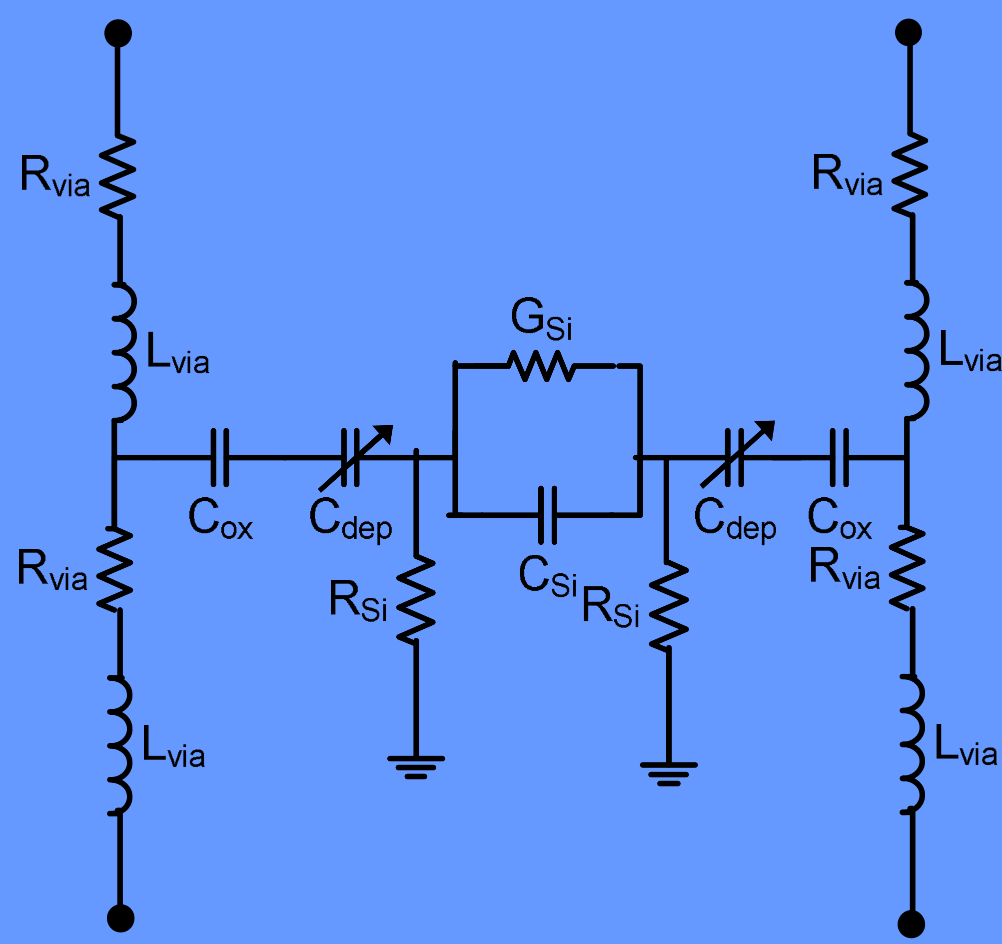
Effect of Substrate Bias on TSV Capacitance



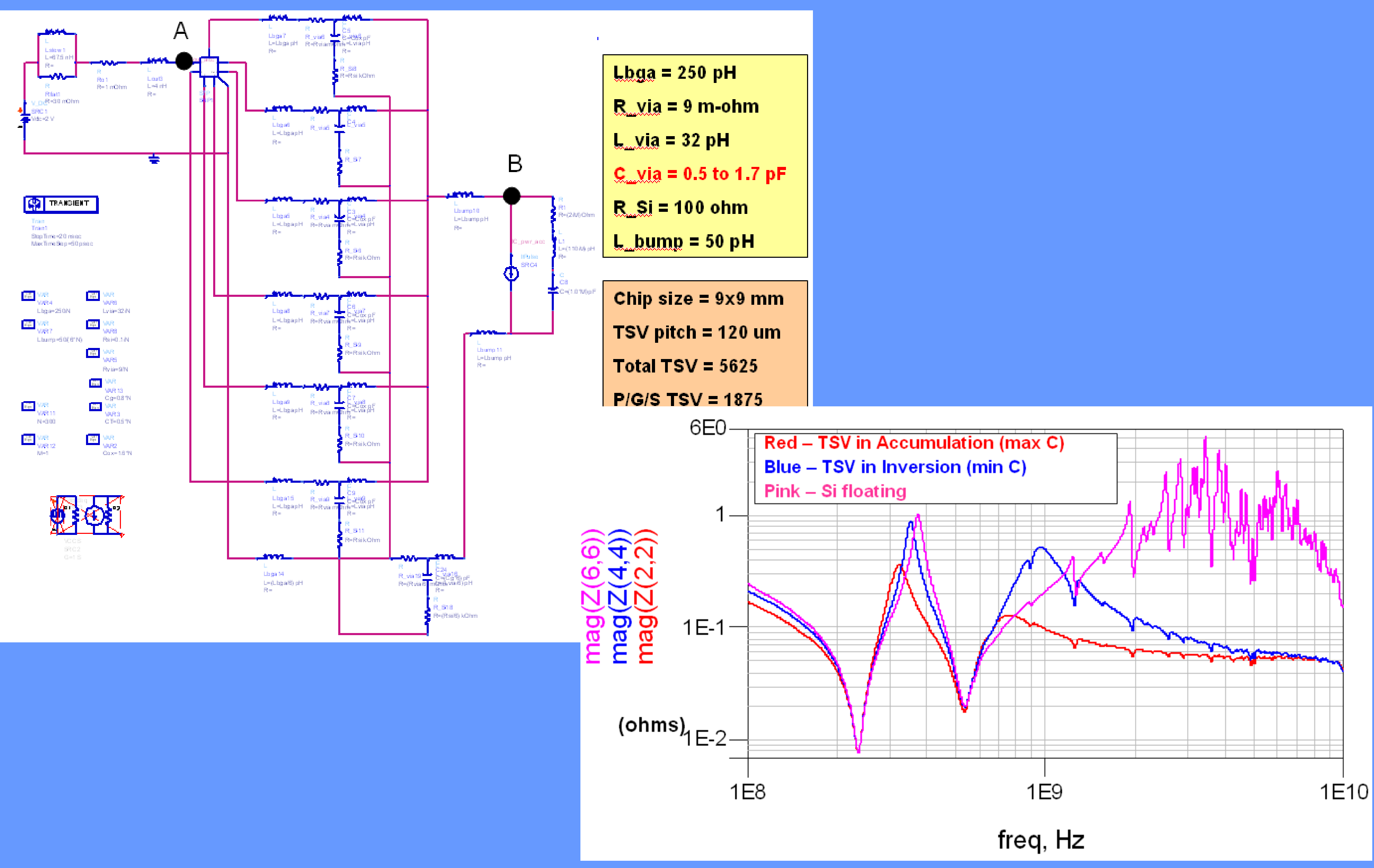
Courtesy : Packaging Research Center

Modified TSV Model



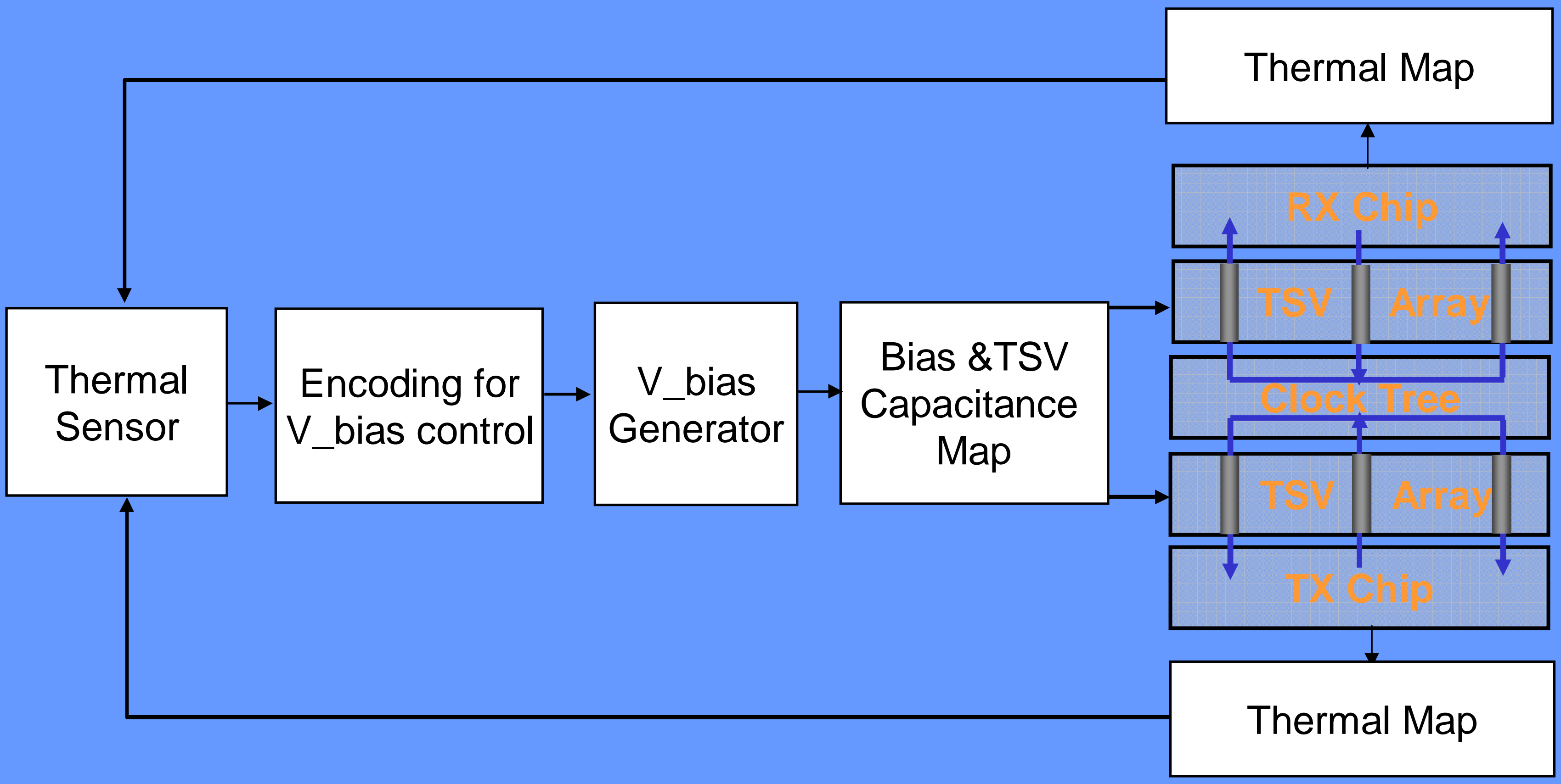


Power Delivery with Variable TSV Capacitance



Courtesy : Packaging Research Center

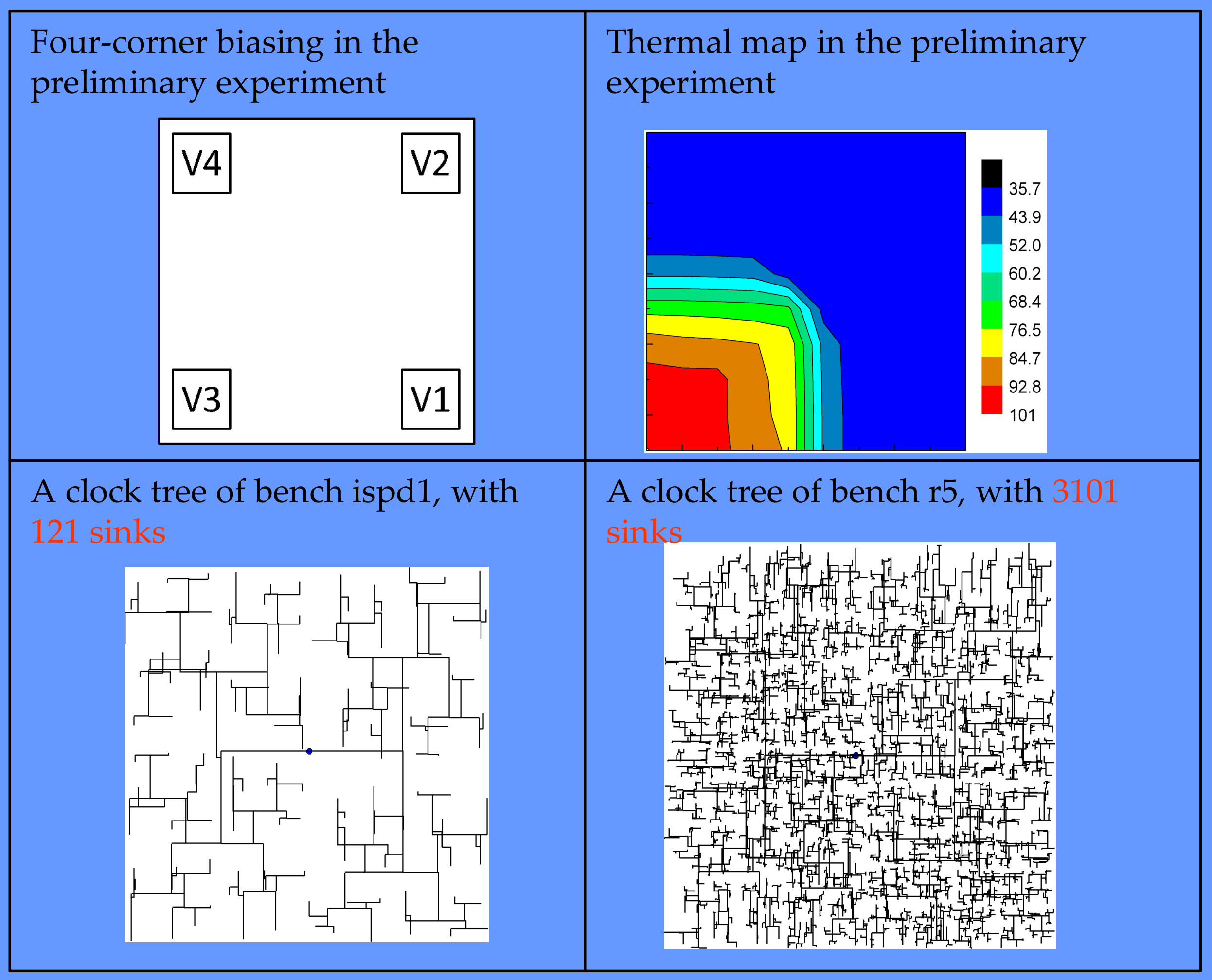
Thermal Aware Clock Distribution



Static/Dynamic Control for Thermal variation

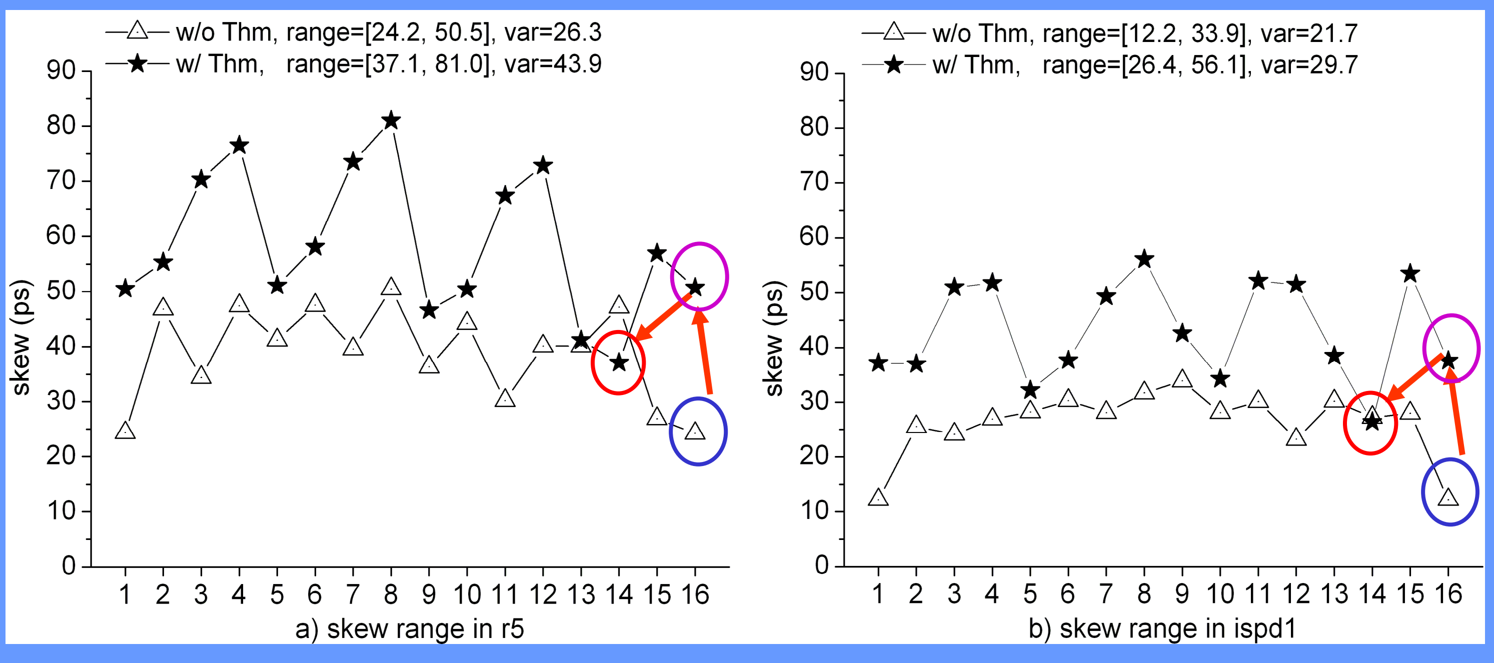
3D clock distribution for power/thermal noise isolation

3D Clock Tree with Voltage Controlled TSV



In collaboration with Prof. Sungkyu Lim, Georgia Tech

Clock Skew Adjustment with Thermal & Bias Effect

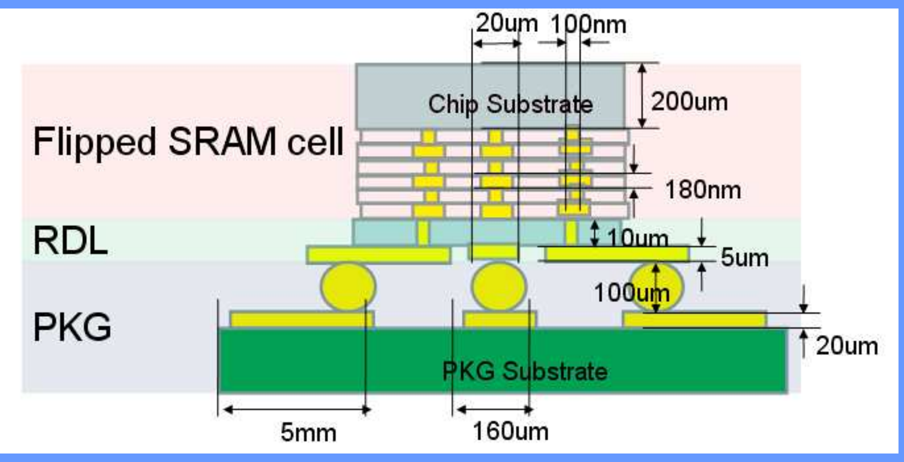


- Optimized skew under constant thermal profile
- Increase skew due to active thermal profile
- Re-optimized skew using VC-TSV bias control

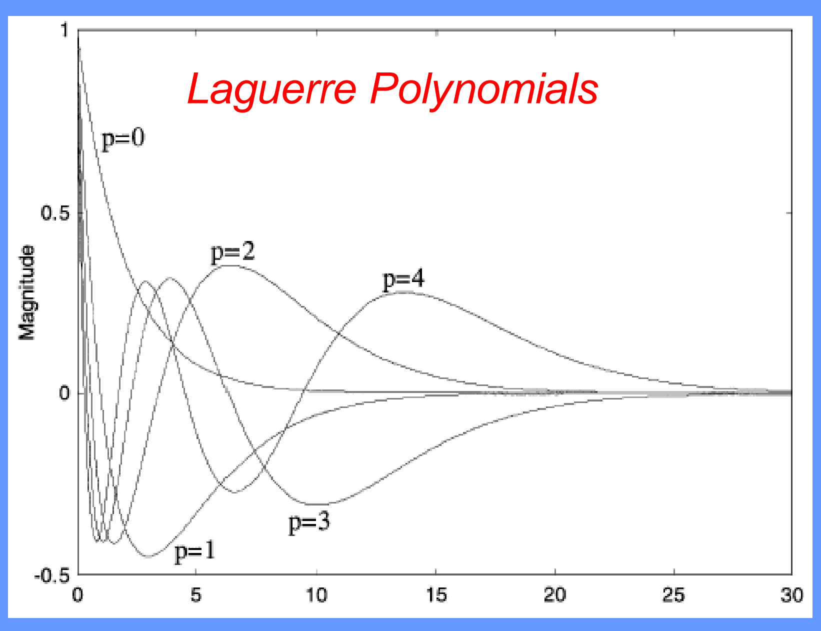
In collaboration with Prof. Sungkyu Lim, Georgia Tech

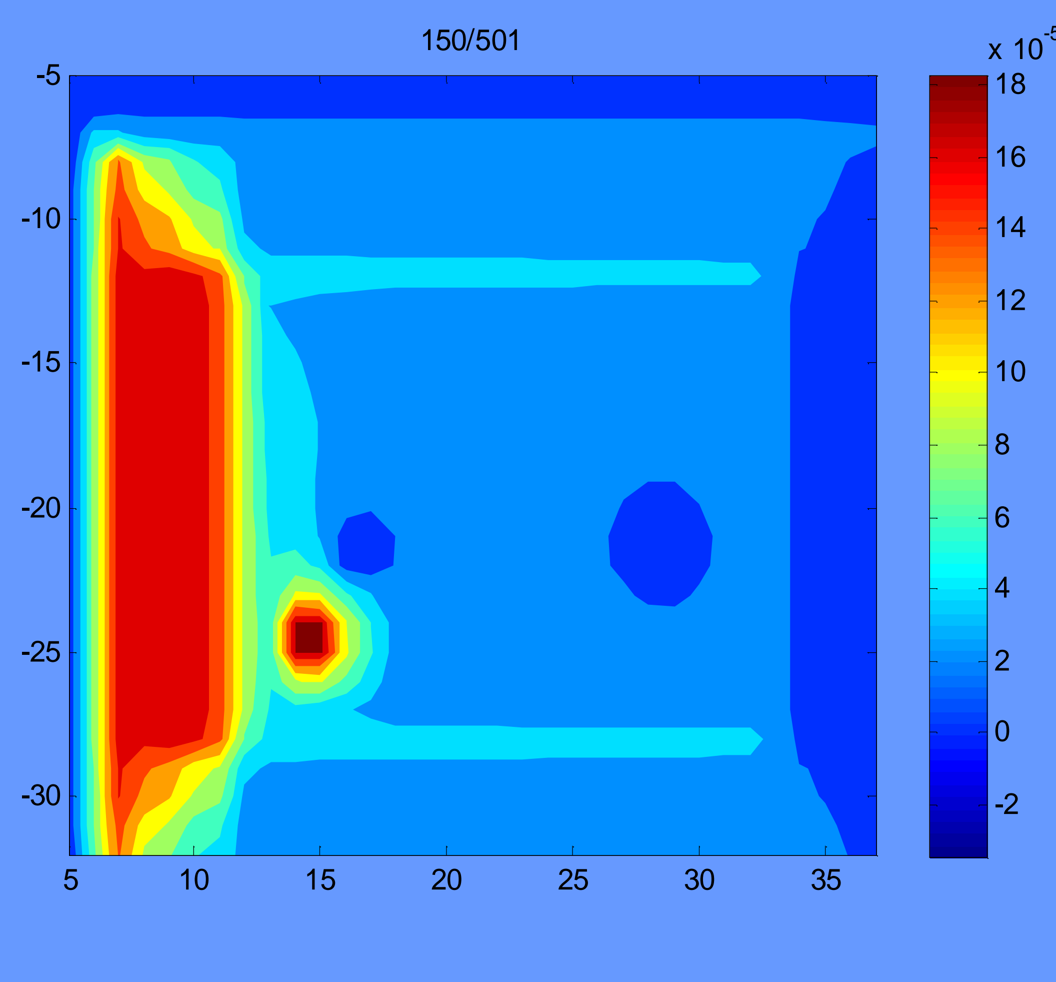
Multi-scale System Level Modeling

Chip-Package Multi-scale Structures



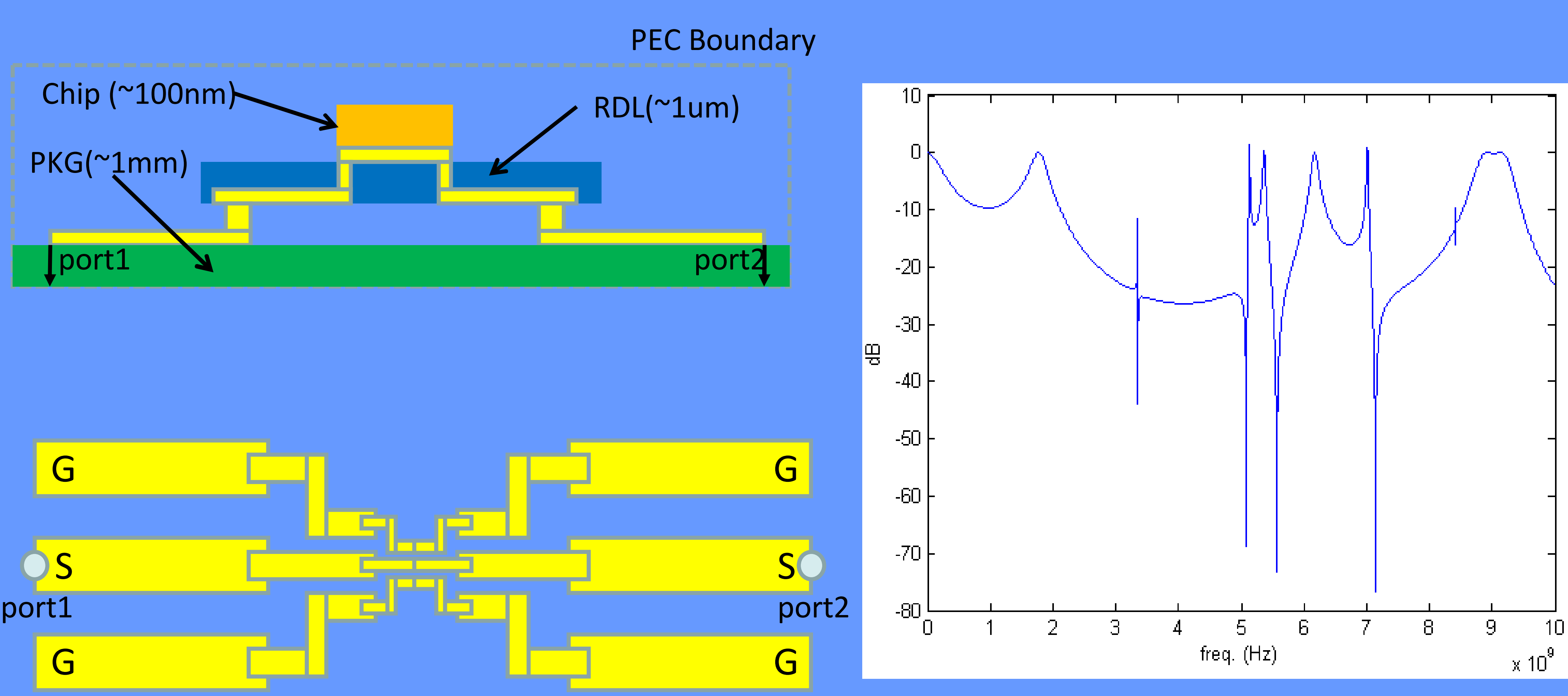
Ratio of Dimensions = 5mm/100nm = 50000





M. Ha, K. Srinivasan, M. Swaminathan, "Chip-Package Co-Simulation with Multiscale Structures ,"IEEE Electrical Performance of Electronic Packaging, 27-29 Oct. 2008 Page(s):339 - 342

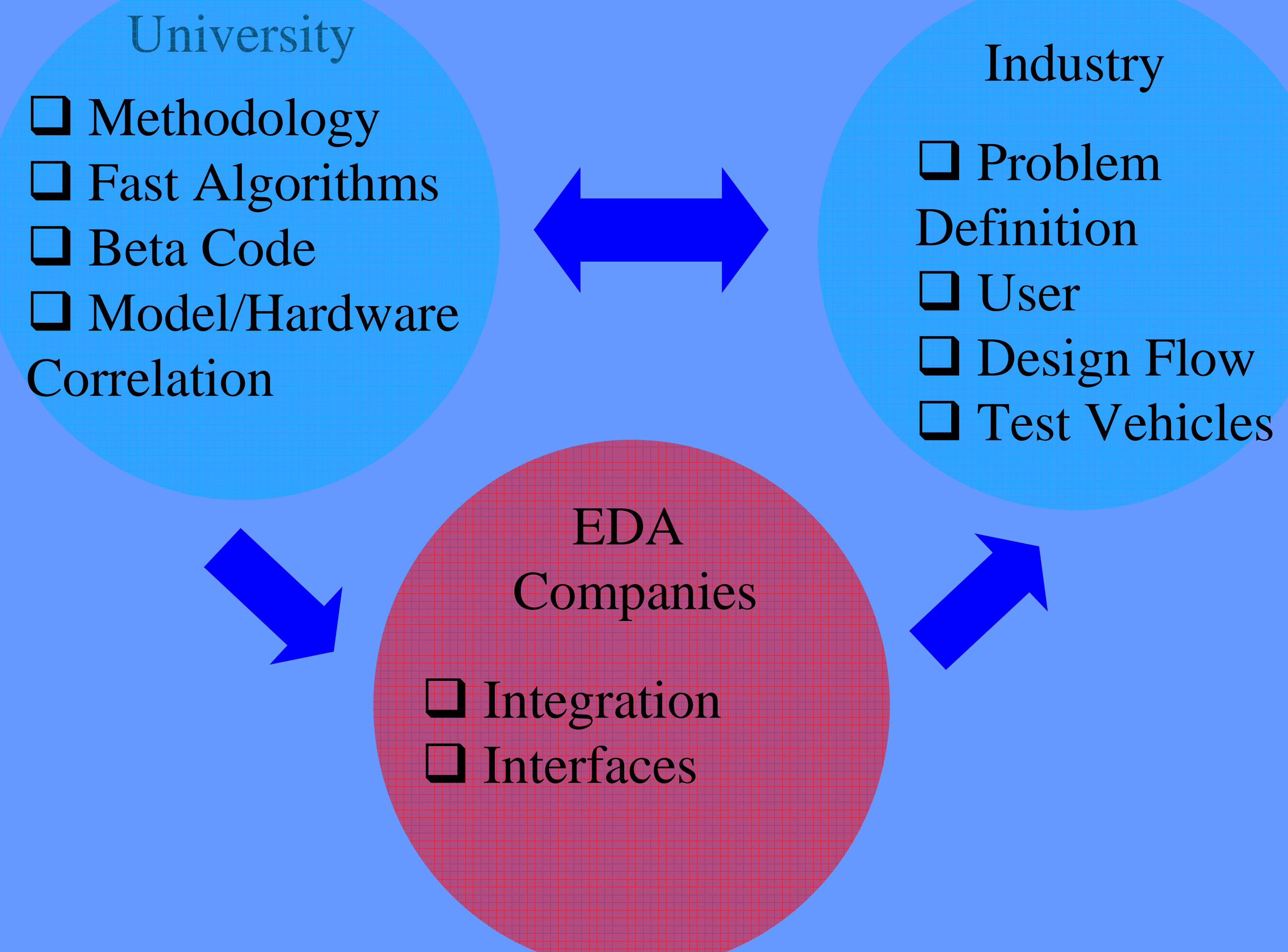
Chip – Package Transitions



Length scale 1:10,000

How do you make the tools available to computer designers ?

Mixed Signal Design Tools - Initial Consortium Idea
Packaging Research Center

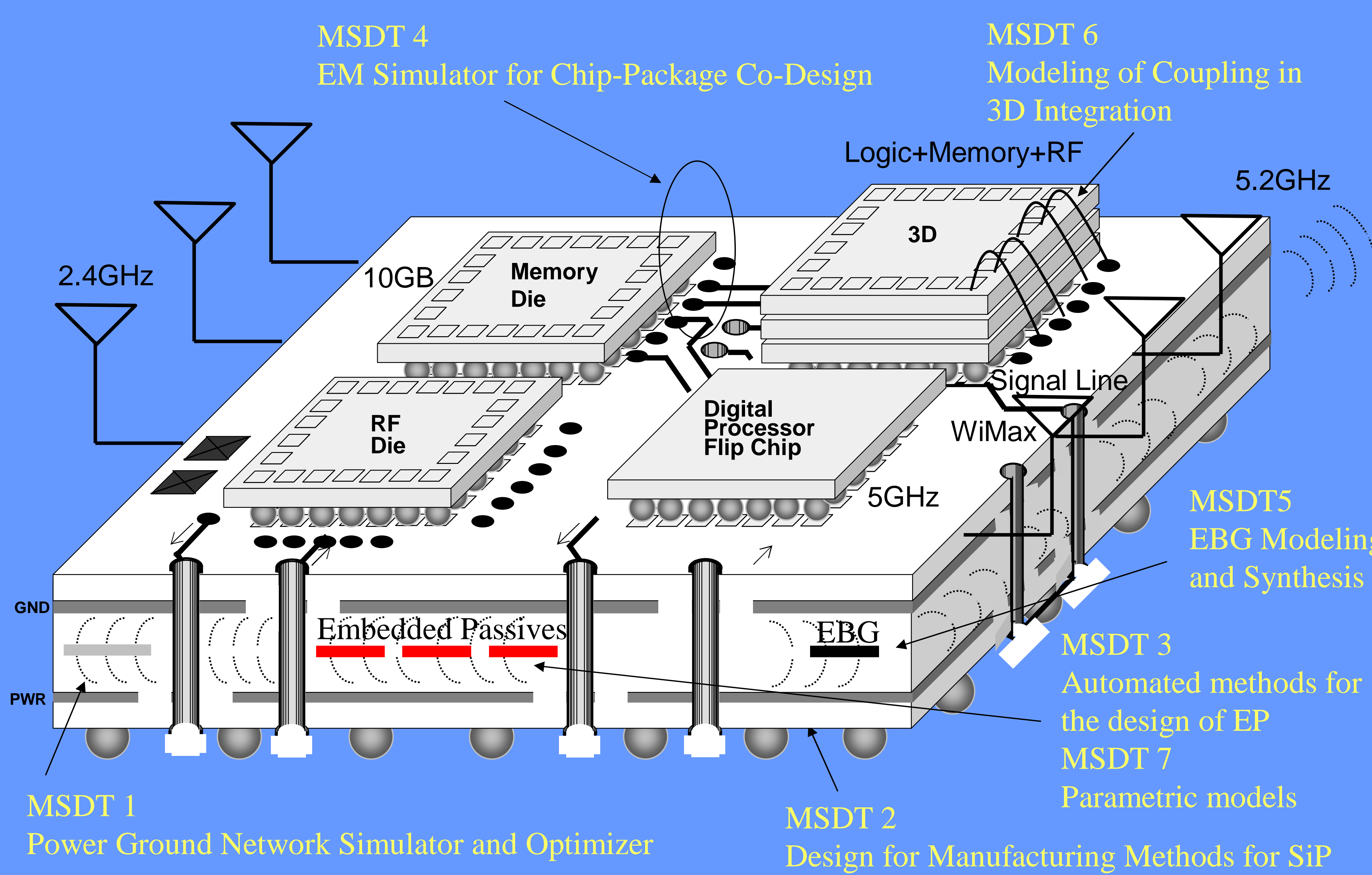


Mixed Signal Design Tools Consortium

- Consortium Model
  - Multiple companies join by paying membership fee
  - Money is pooled to fund a group of projects
  - Company members get to mentor projects and help in defining direction
  - Pre-competitive research
  - Non-exclusive, royalty free license provided to all members
  - Deliverables are design/modeling tools

- Mixed Signal Design Tools Consortium
  - Joint collaboration between Georgia Tech and Politechnico di Torino
  - 2 years (2007 – 2009)
  - 5 companies
  - ~$1M funding

Ultra-Miniaturized Mobile Computing Platform



Mixed Design Tool Consortium
Collaboration between Industry, GT and P. di Torino

- ❑ EPCOS
- ❑ Infineon
- ❑ Sameer
- ❑ Panasonic
- ❑ NXP

MSDT Projects

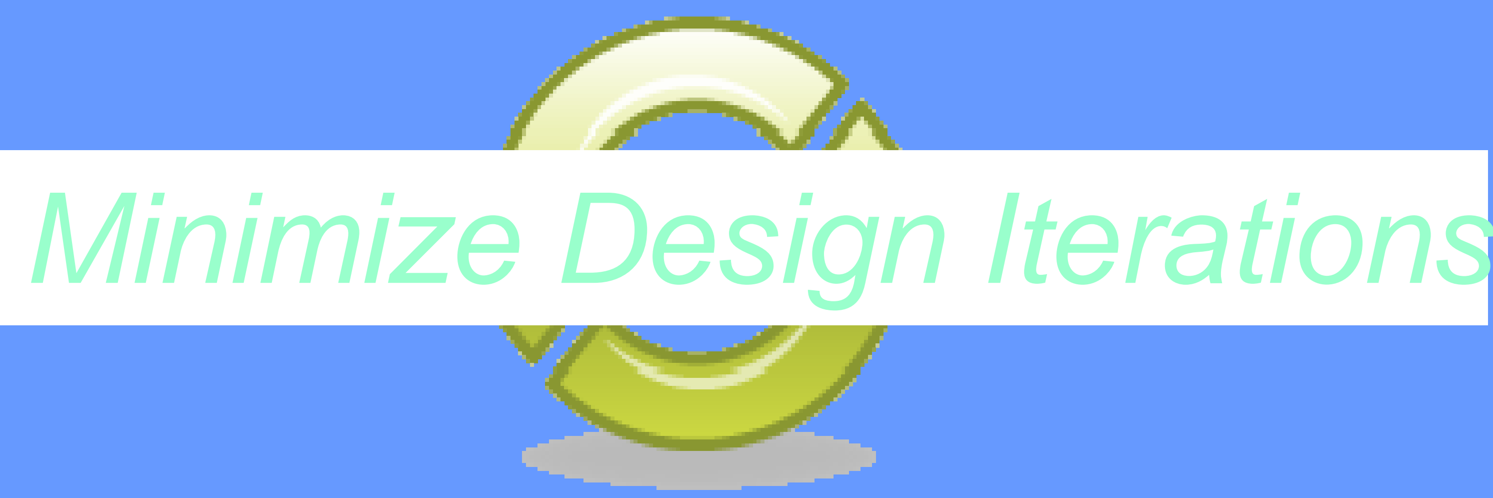
Project	Problem Addressed	Solution Technique
MSDT 1	Signal and Power Integrity	M-FDM
MSDT 2	Layout level DFM	Response Surface, convolution and DOE
MSDT 3.1	Automated library dev. for RF Passives	Augmentation with Fast Circuit Based EM Solver
MSDT 3.2	Place & Route for RF Passives	Simulated Annealing & Partitioning
MSDT 4	Multiscale EM Simulation	Laguerre Polynomials and FDTD/MNA
MSDT 5	Automated design of EBG	Genetic Algorithm
MSDT 6	RLC extraction of 3D structures	Conduction and Accumulation Mode Basis Functions
MSDT 7	Parameterization	Rational Functions

Tools with Input and Output Interfaces

- Based on Input from MSDT Members
- Each MSDT Tool has ASCII Input Format
- And ASCII (Standard – Touchstone; Spice) Output Format
- Input and Output Formats defined and made available to MSDT Members
- Members can write interfaces to any Physical CAD tool
- Interfaces developed by MSDT Consortium
    - DXF
    - Cadence .mcm and .brd

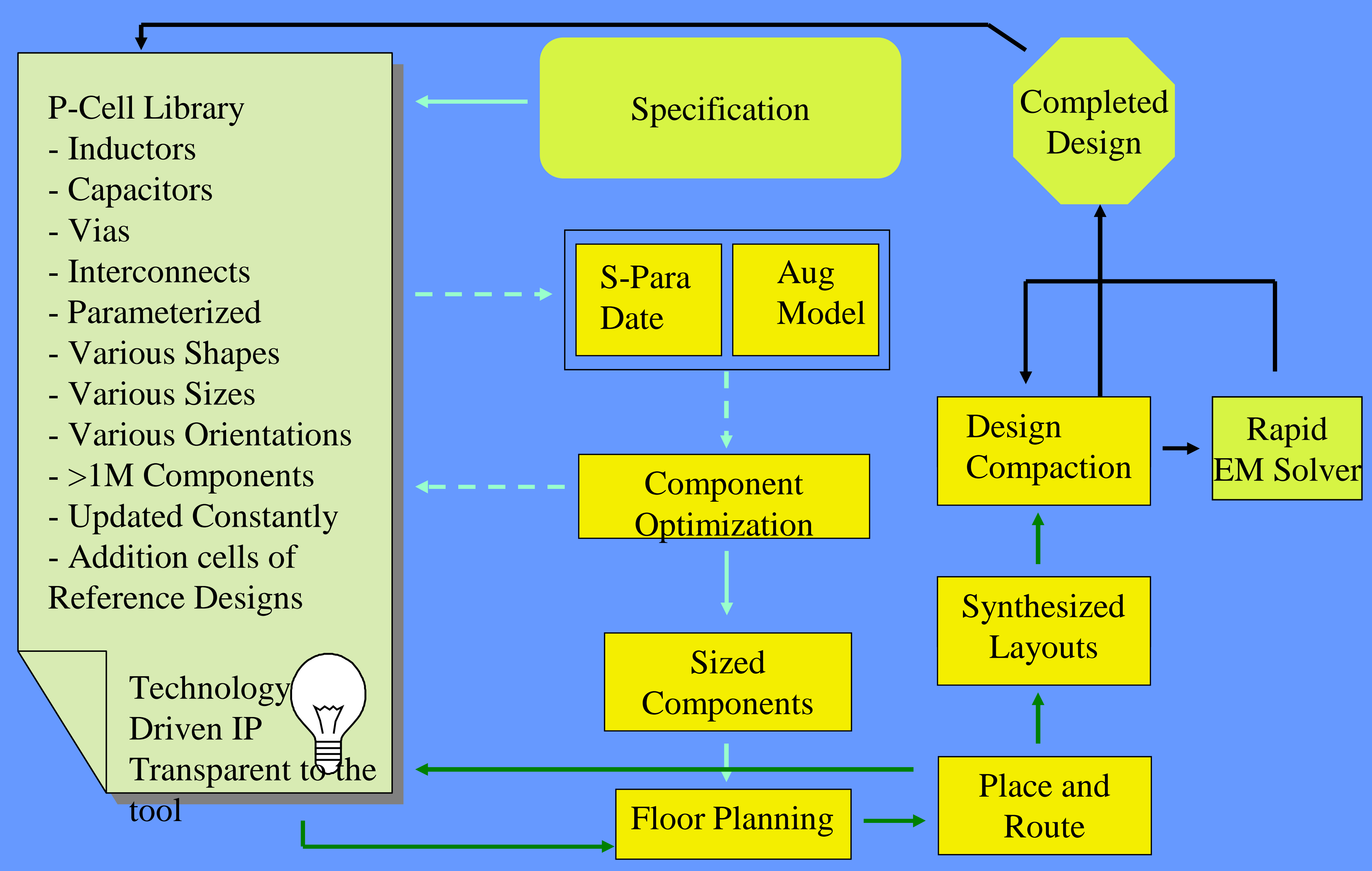
Design Automation for Embedded Passives

Specification

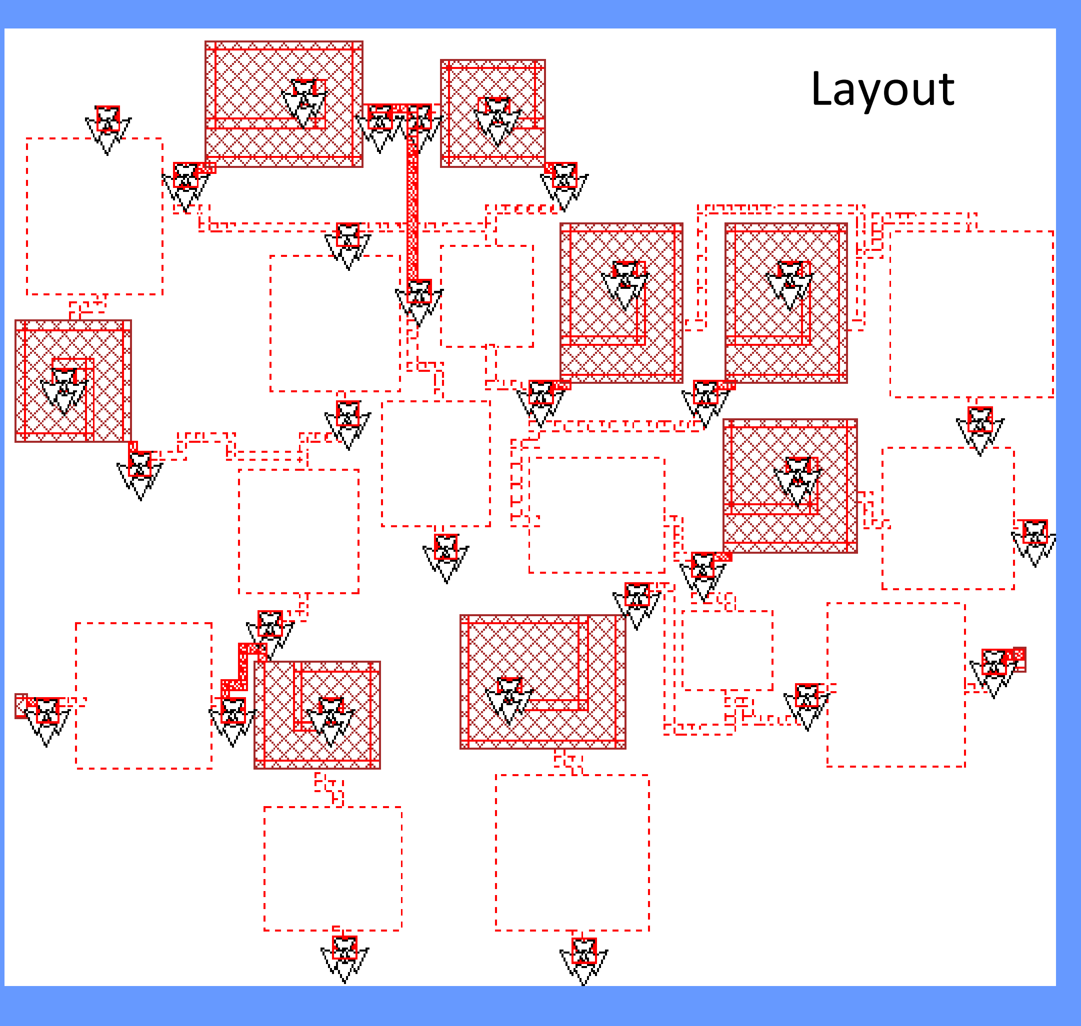


RF Layout

Automated Design Flow for Embedded Passives



21 Component Embedded High Pass Filter Automatic Place and Route (MSDT 3.2)



Response

dB(S(2,1))
dB(S(4,3))
dB(S(6,5))

freq, GHz

- Ideal Schematic response having no net and component parasitic
- EM response of placed and routed circuit using Sonnet
- Response of Placed and routed circuit using circuit models
- RF Spec, the discrete frequency points where the circuit was optimized

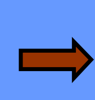
3D Finite Difference Frequency Domain Method
EM Solver - Simfony

Yee-grid (Frequency Domain)

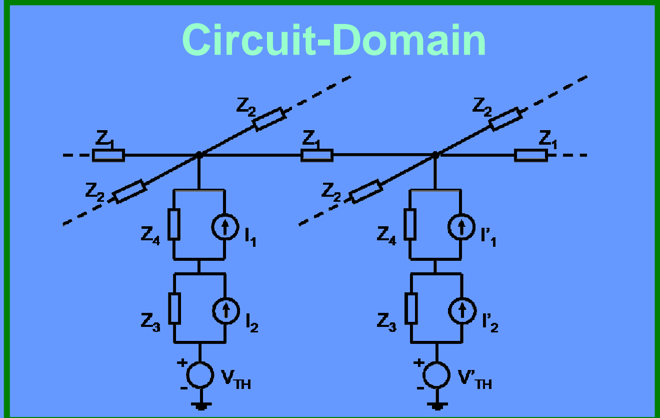
$$\nabla \times \mathbf{E} = -j\omega \mathbf{B}$$

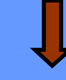
$$\nabla \times \mathbf{H} = j\omega \mathbf{D}$$

Δx
Δy
H_z
H_y
E_z



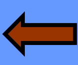
Circuit-Domain





Krylov Subspace

$$K_n(v_1, A) = \text{span}\{v_1, Av_1, \ldots\ldots A^{m-1}v_1\}$$



Iterative Solution

O(N) memory and O(N(logN)) speed

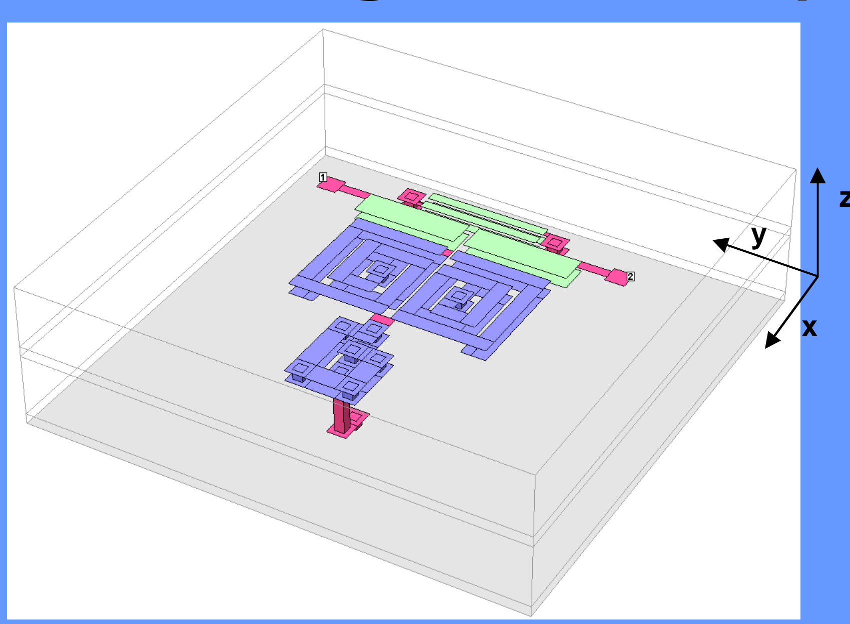
Two-sided Lanczos Algorithm

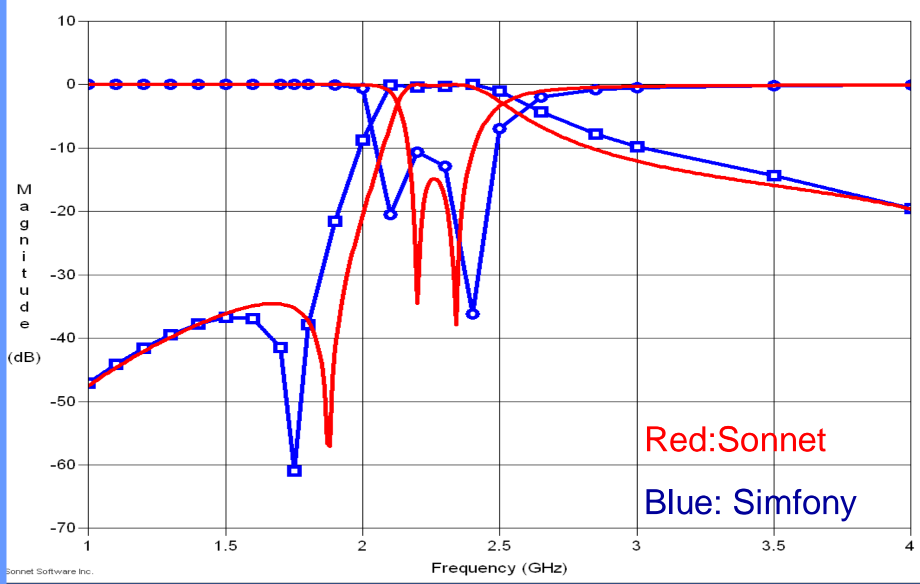
1. *Compute* $r_0 = b - Ax_0$ *and* $\beta = \|r_0\|_2$
2. *Generate the biorthogonal Lanczos vectors*
3. *Compute* $y_m = T_{m-1}$ *and* $x_m = x_0 + V_m y_m$

Features of circuit-based frequency-domain formulation

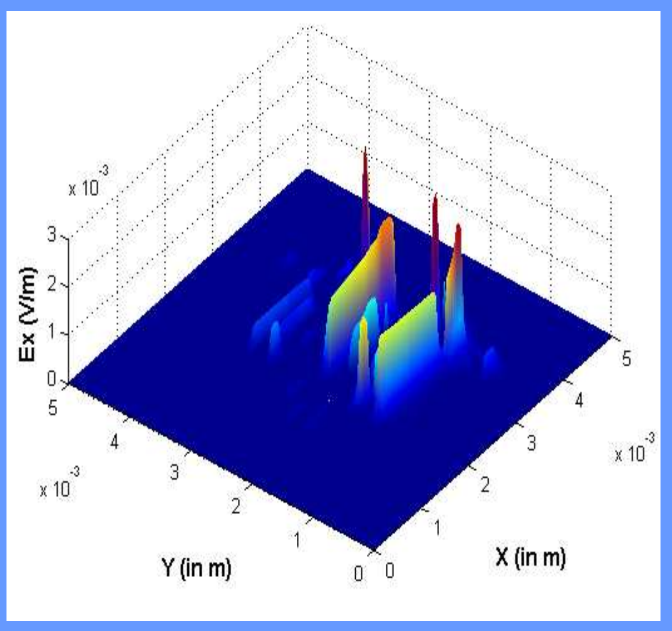
1. Spice-like tool for full-wave 3D-EM/lumped-element cosimulation
2. Fast memory-efficient iterative solution for large problems
3. No post-processing steps necessary (for time-to-frequency conversion)

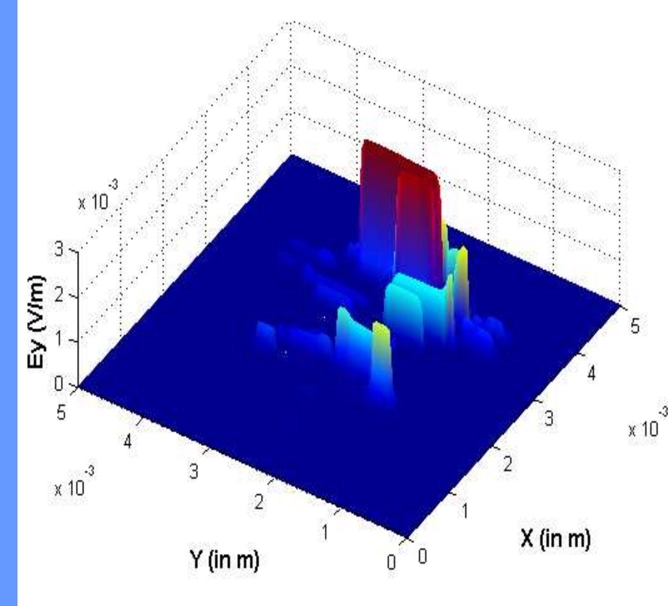
Modeling of Band-pass Filter with MSDT 3.1

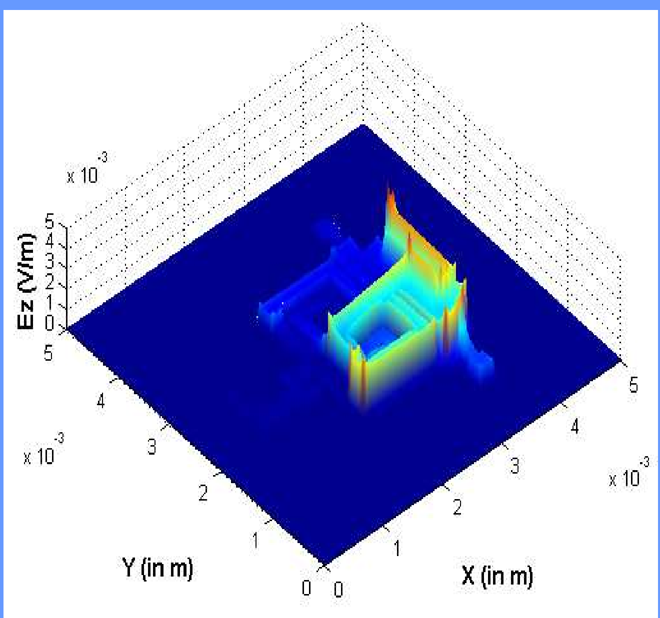




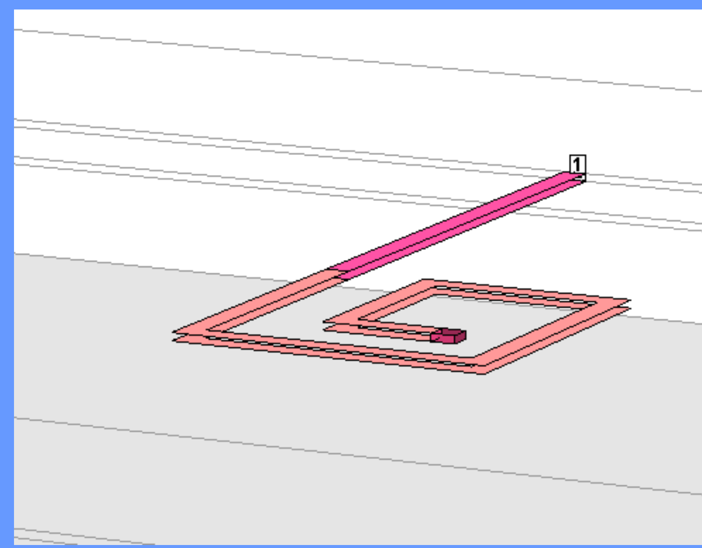
Electric Field Distributions on 1st Metal Layer at 2GHz







Parameterized Library Development (MSDT 7)



Multi-layered
Spiral Inductors

S_{22}, magnitude

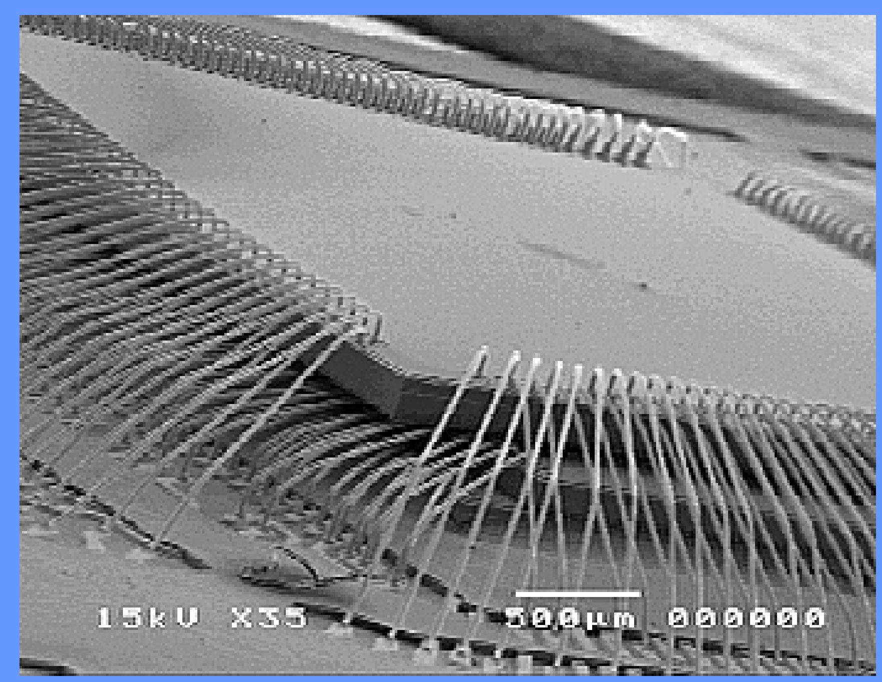
0.8
0.6
0.4
0.2
0
0 2 4 6 8 10 12

S_{22}, phase (degrees)

200
100
0
-100
-200
0 2 4 6 8 10 12

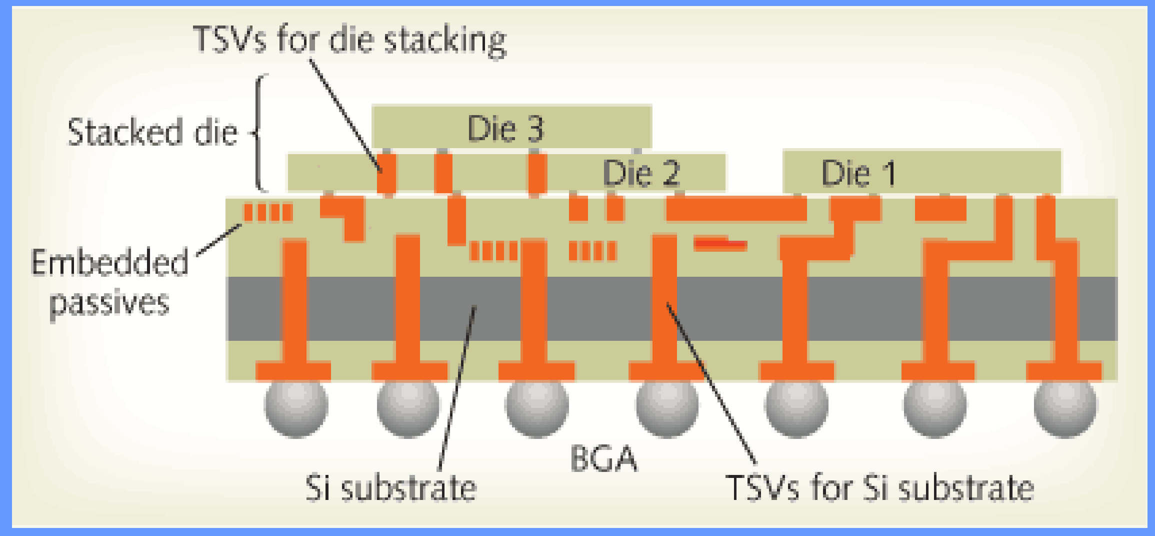
Frequency [GHz]

3D Stacking



Stacking using Wirebond

Stacking using TSV



Ref: R. Chatterjee, R. Tummala, "The 3DASSM Consortium: An Industry/ Academia Collaboration," online article in http://ap.pennnet.com

Rapid EM Modeling of Cylindrical Structures (TSVs, Wirebonds, Vias, Transitions ....)

$$\frac{\vec{J}(\vec{r},\omega)}{\sigma} + j\omega\frac{\mu}{4\pi}\int_{V'} G(\vec{r},\vec{r}\,')\vec{J}(\vec{r}\,',\omega)dV' = -\nabla\Phi(\vec{r},\omega)$$

IE with vector potential

$$\vec{J}_j(\vec{r},\omega) \cong \sum_{n,q} I_{jnq}\vec{w}_{jnq}(\vec{r},\omega)$$

Approximate current using
cylindrical CMBF

$$\vec{w}_{i0} = \frac{\hat{z}_i}{A_{i0}} J_0(\alpha(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i)$$

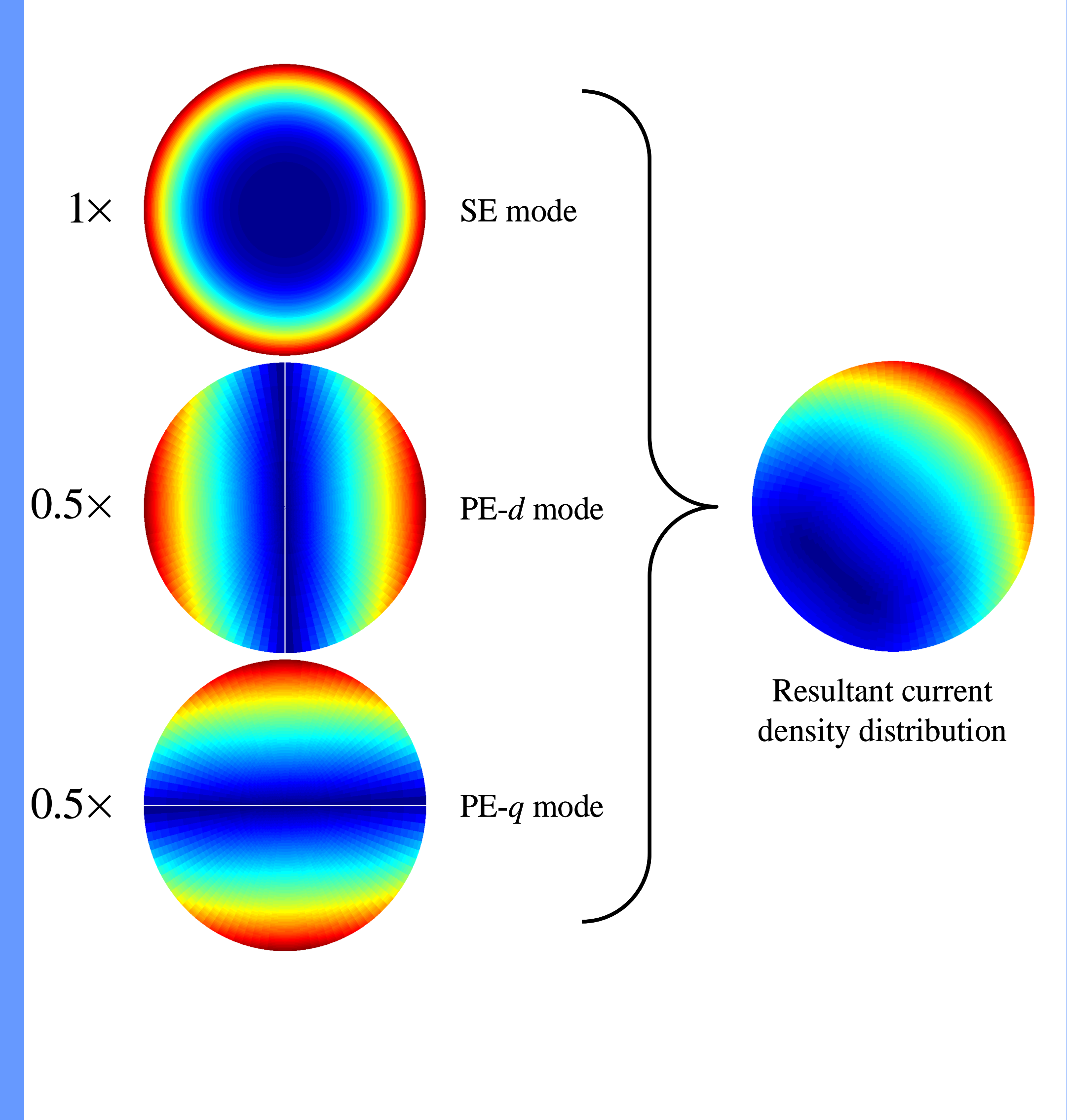
(SE mode)

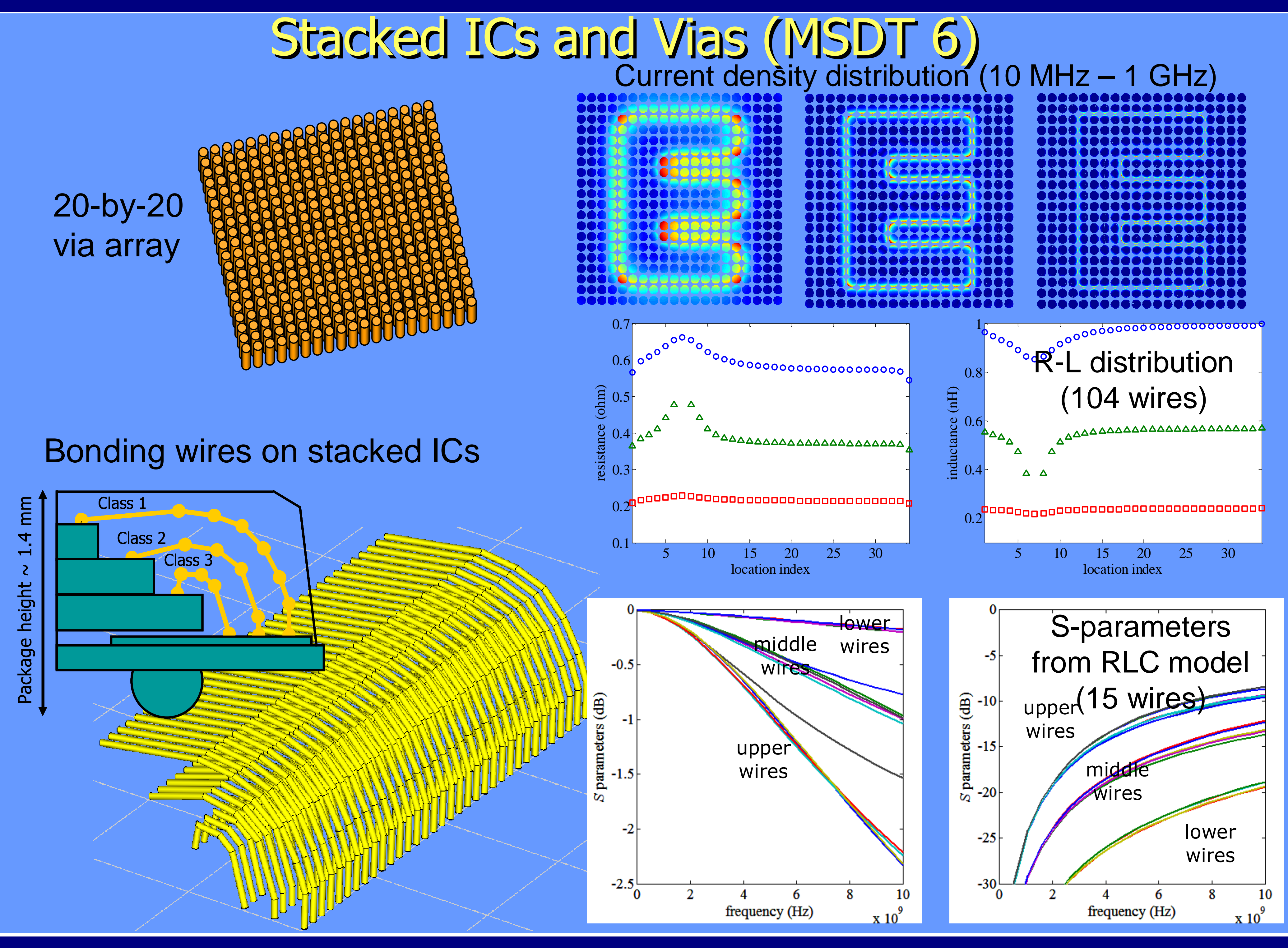
$$\vec{w}_{in\{d,q\}} = \frac{\hat{z}_i}{A_{in}} J_n(\alpha(\vec{r}-\vec{r}_i)\cdot\hat{\rho}_i)\begin{Bmatrix}\cos(n\varphi_i)\\ \sin(n\varphi_i)\end{Bmatrix}$$

(PE mode)

$$\sum_{n,q} I_{jnq}R_{imd,jnq} + j\omega\sum_{n,q} I_{jnq}L_{imd,jnq} = \Delta V_{imd}$$

Voltage equation
between two interconnect nodes




Stacked ICs and Vias (MSDT 6)
20-by-20
via array
Current density distribution (10 MHz – 1 GHz)
R-L distribution
(104 wires)
resistance (ohm)
inductance (nH)
location index
Bonding wires on stacked ICs
Package height ~ 1.4 mm
Class 1
Class 2
Class 3
S-parameters
from RLC model
(15 wires)
lower
wires
middle
wires
upper
wires
S parameters (dB)
frequency (Hz)
x 10^9

Spin-Off

- No EDA company would join the consortium
- Support and further development for MSDT tools – major issu
- Led to spin-off company – E-System Design
  - Based on consultation with MSDT members

VISIT E-SYSTEM DESIGN BOOTH AT EPEPS

For further information:

www.epsilonlab.ece.gatech.edu
www.e-systemdesign.com