Fast 3D EM Simulation for Digital System Design

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Outline

- Digital system simulation requirement
- SiP, 3D IC and TSV
- 3D fullwave EM solution progress review
- Chip modeling (from RTL to GDS) for system level EM analysis

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Scope and Challenge

- What is ***System Level*** EM simulation?
  - RTL to GDS
  - Chip, Package/SiP and PCB
- ***Driven*** by
  - Cost and margin
  - Risk mitigation and first time success
- ***Challenges***
  - Accuracy and Capacity
  - Multi-domain physics
  - Next generation chip-package designs

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IC Technology Impact on Package/PCB

$$Z_{target} = (Vdd \times 0.05)/(I \times 50\%)$$

Year	Technology	Power (W)	Vdd (V)	Current (A)	Target Impedance (mΩ)
2004	90nm	84	1.2	70	1.7
2007	65nm	103	0.9	115	0.7
2010	45nm	119	0.6	198	0.3

System design margin is becoming Less and Less!

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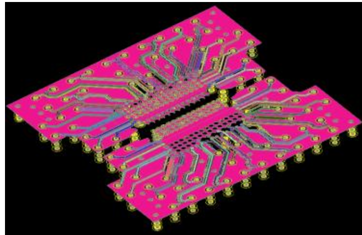
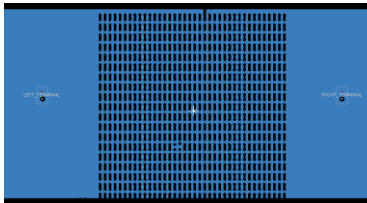
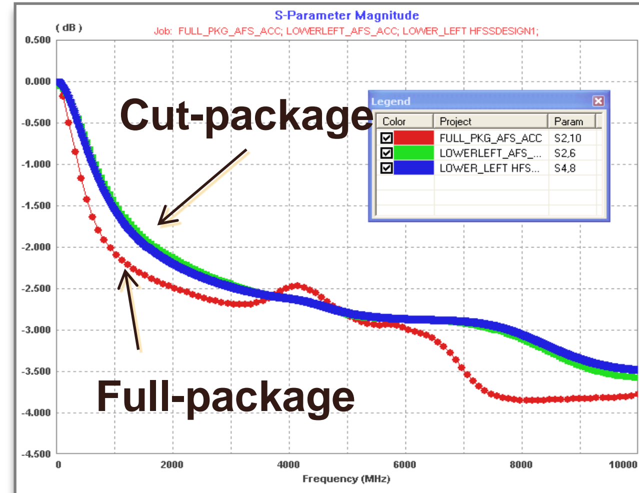
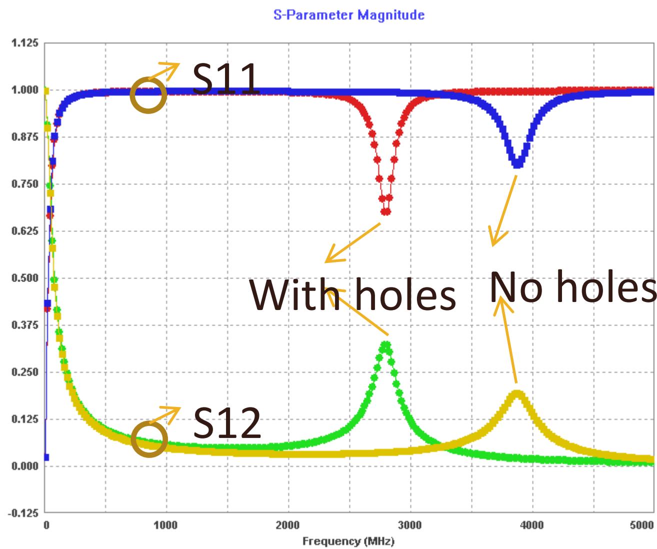
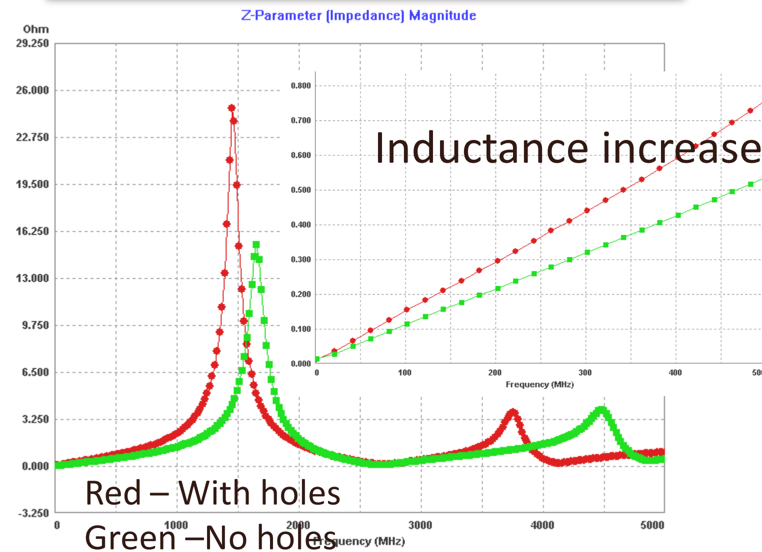
EM Accuracy Impact on Design Margin











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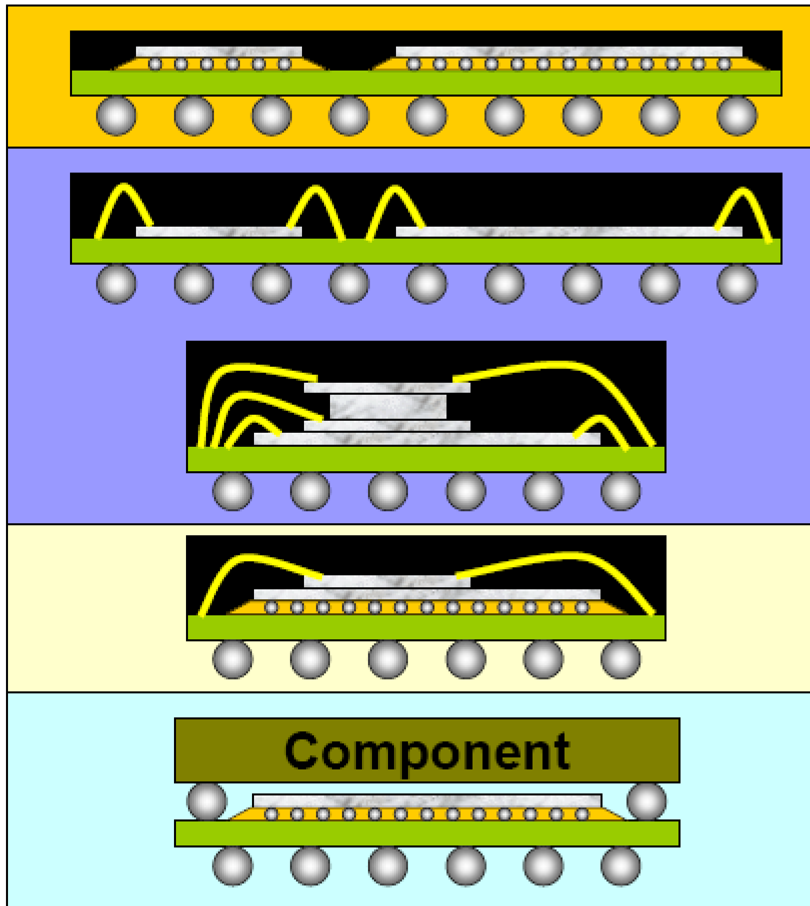
Traditional SiP Configurations



- FC Side by side
- WB side by side
- Stacked WB
- Hybrid stack
- PoP stack

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SiP Opportunities

SoC	SiP
Single tech node	Multiple tech node
All IP's ported to same technology node	Mix of IP's in diff technology nodes
Horizontal partitioning	Horizontal & Vertical partitioning

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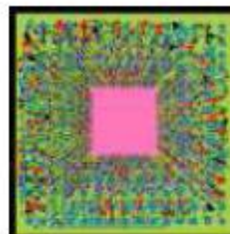
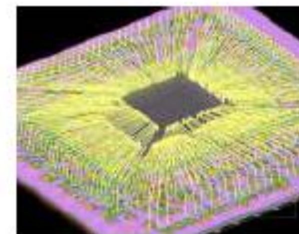
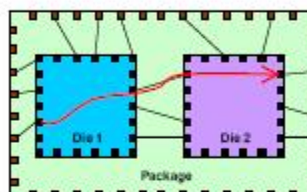
SiP Design Flow: Reference Flow 10.0

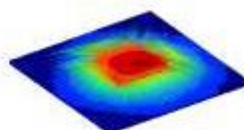
- Basic Implementation
  - SiP Elec Design/Connectivity
  - SiP Package Physical Design



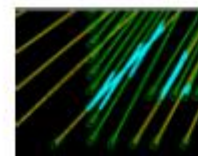


- Analysis
  - SiP Package Electrical Extraction
  - SiP Static Timing Analysis (STA)
  - SiP IR Drop
  - SiP Signal Integrity (SI) & Simultaneous Switching Noise (SSN)
  - SiP Thermal





- Verification
  - SiP Design Rule Check (DRC)
  - SiP Layout Versus Schematic (LVS)



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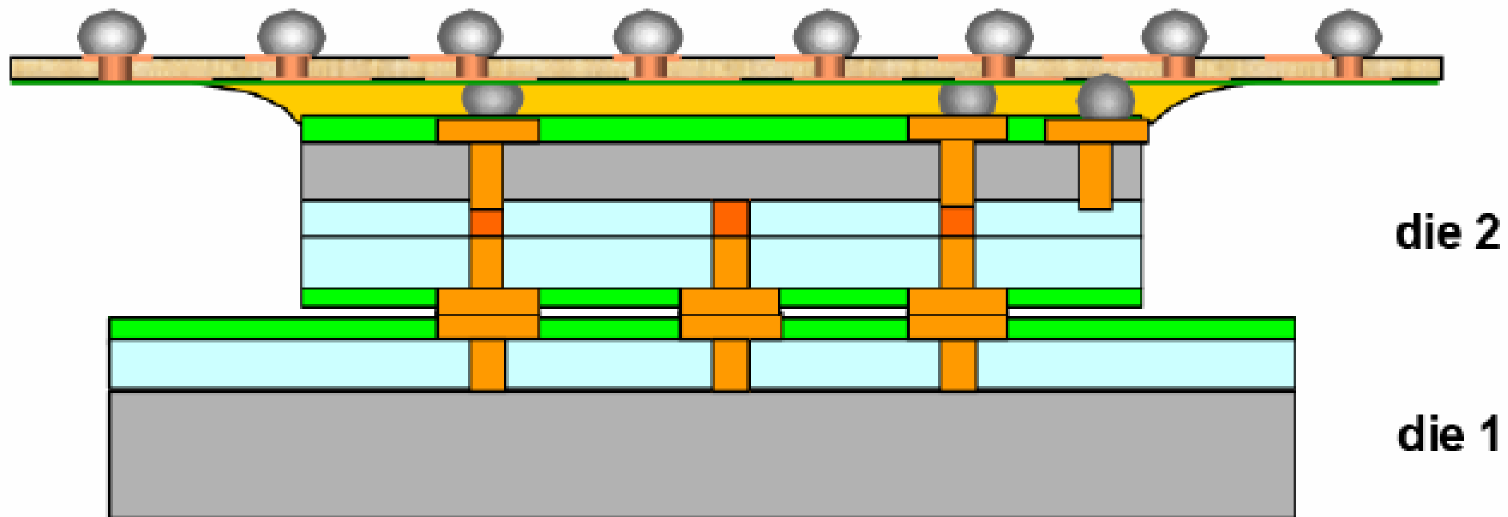
3D Stacking with TSV



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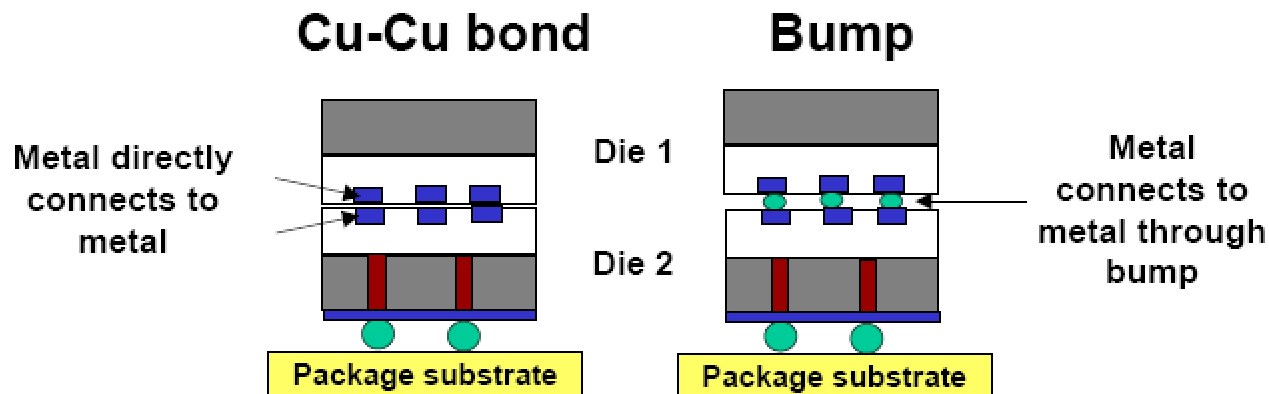
Die-to-die Connection

- Cu-Cu bond or Bump
  - Cu-Cu bond: Top-metal from each die touch directly to create connectivity
  - Bump: Top-metal from each die connected through bump as in standard bump process.



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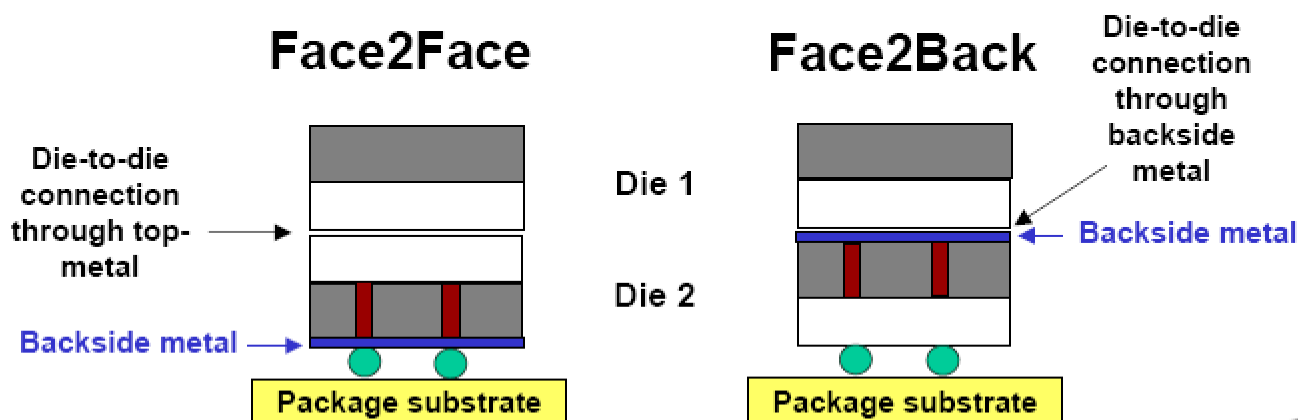
Stacking Schemes

- Face2Face or Face2Back
  - Face2Face: Top-metal of two dice connected to each other and has package bump on backside
  - Face2Back: Top-metal of first die connected to backside metal of second die and has package bump on front-side



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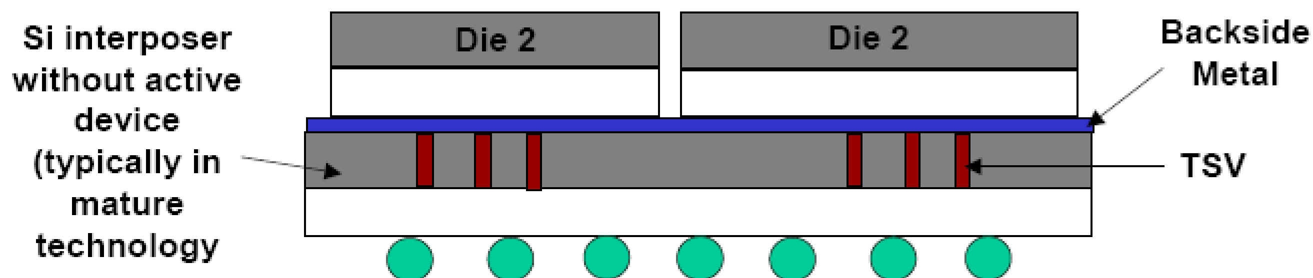
Silicon Interposer using TSV
- Alternative use of TSV

- TSV technology provides opportunities beyond 3D stacking
- TSV can be used to implement Si-Interposer that replaces package substrate in traditional SiP's
- Advantages in lower parasitics and denser routing



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3D IC Benefits

- Form-factor
  - Same as SoC without SoC complexity
- Speed
  - TSV RC in same order as chip metal
  - Die interconnect as opposed to off-chip interconnect
- Power
  - IO power reduced

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3D IC Design and Analysis Challenges

- Die-package co-design is a must
- 3D electromagnetic simulation necessarily beyond package and PCB

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System Level EM Simulation

- Complexity and size of the design requires large capacity and high efficiency
- Multiscale geometry usually leads to worse conditioning of the final matrix system
- Broadband solution requires the EM engine to work seamless from DC to multi-giga Hertz
- Whole system analysis requires the bi-directional link between EM model and circuit components

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Progress on FEM

- **Domain decomposition method**
  - Various forms
  - Frequency domain and time domain
  - Parallelization
- **Multi-grid method**
- **Layered finite element reduction recovery method**

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Progress on MoM

- **Improve electric field integral equation (EFIE) for better conditioning over broadband**
  - Calderon multiplicative preconditioner leverages the Calderon identity to obtain a well conditioned matrix
  - Augmented electric field integral equation (AEFIE) in a generalized saddle point form is a simple remedy for the low-frequency break down of EFIE
  - Current and charge integral equation (CCIE) constructs a sophisticated second kind integral equation to improve the conditioning
  - Equivalence principle algorithm (EPA) is an integral equation based domain decomposition method for multiscale structure

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Progress on MoM

- **Reduce dense matrix operation towards linear complexity**
  - Multilevel fast multipole algorithm (MLFMA) factorizes the Green's function based on the addition theorem
  - FFT based method utilizes the block Toeplitz structure of the impedance matrix of a regular grid
  - Fast QR method compresses the well-separated impedance matrix blocks
  - Adaptive cross approximation (ACA) is a rank-revealing LU decomposition without the need of computing all the matrix elements
  - H2 matrix creates block partitioning based on a cluster tree and approximates the integral operator kernel with polynomial interpolation

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Define Next Generation Fast 3D Solver

- Full package and PCB capacity
- DC to 10’s GHz fullwave accuracy
- Native multi-core and multi-processor
- Robust co-simulation with circuits
- Handle multi-scale geometry

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Co-Analysis

EM Source

- On-die device switching
- On-die substrate coupling
- IO simultaneous switching
- On-die core to IO coupling

EM Channel

- Package/PCB global power ground network
- Package/PCB power to signal coupling
- Signal return path discontinuity
- Radiation from traces, wires, vias and edges

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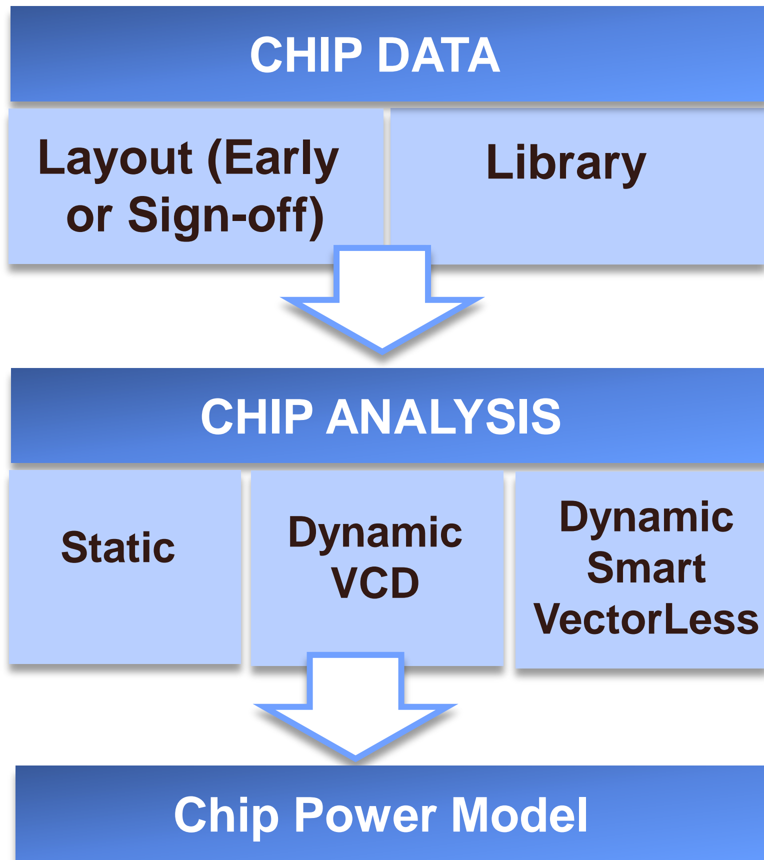
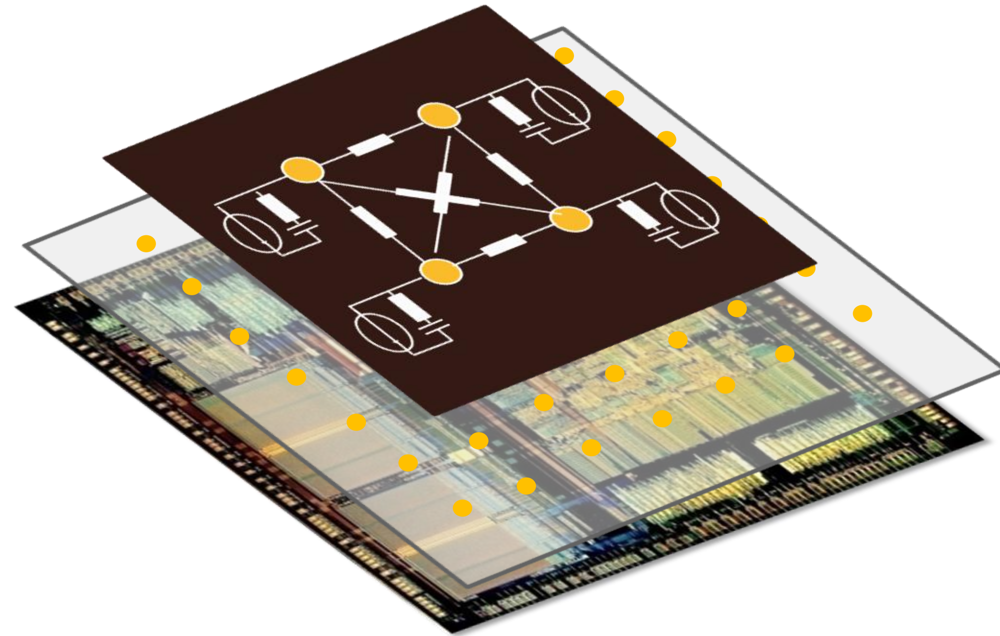
Chip Power Model

Power Delivery Network Analysis & Optimization





Modes

- Static (I_{avg}, R)
- Frequency domain (RLC)
- Time-domain (I(t), RLC)

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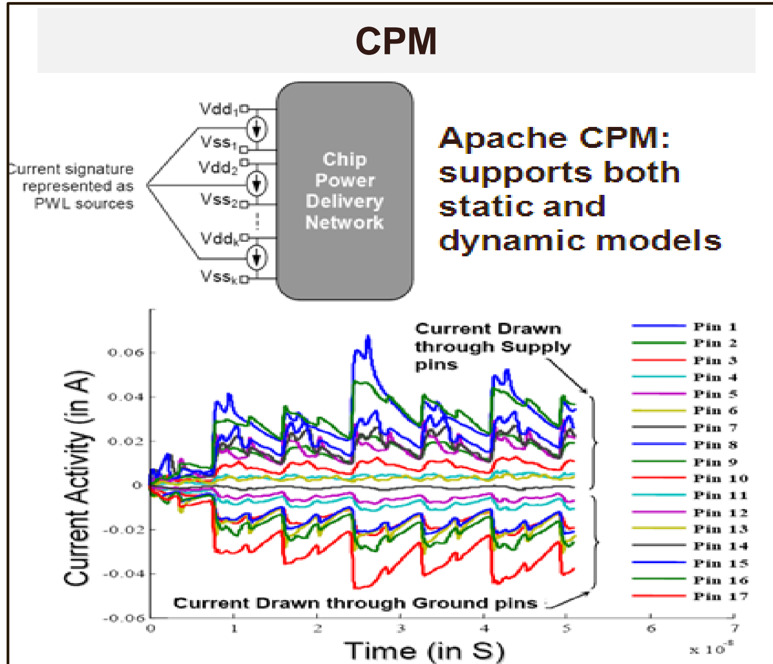
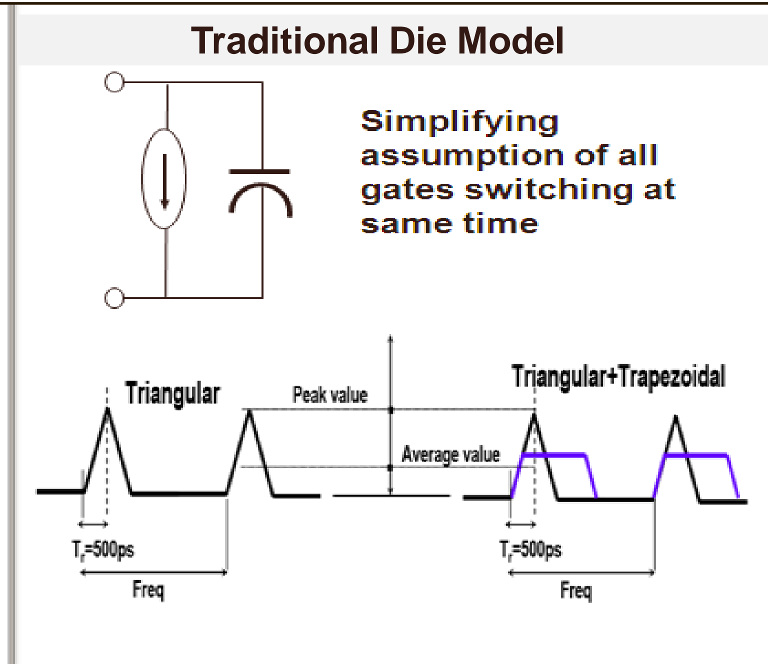
Chip Power Model

Power Delivery Network Analysis & Optimization

Switching Current





Die Parasitics

CPM includes all die parasitics

Power-grid RLC
Intrinsic De-cap
Intentional De-cap
Instance Load Capacitance
Well Capacitance

Estimated Cdie
Missing Rdie, Ldie

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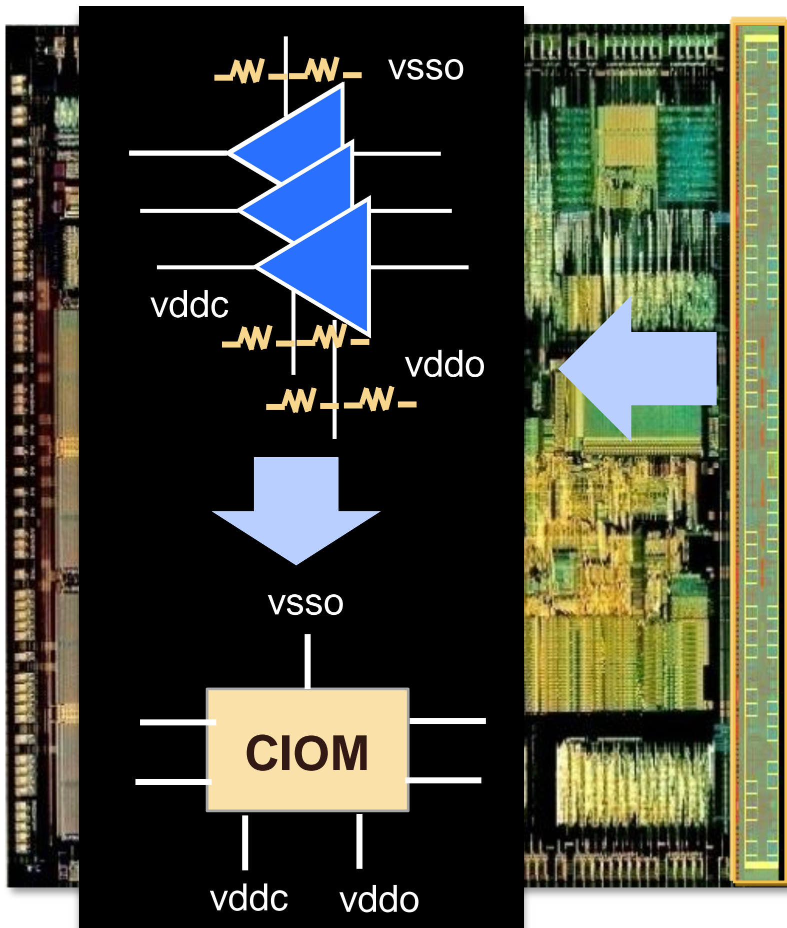
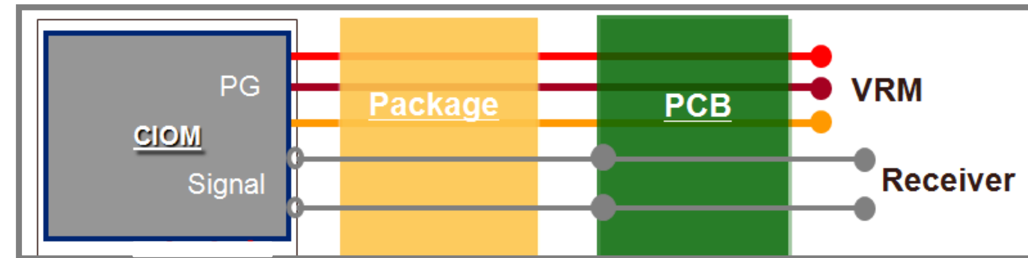
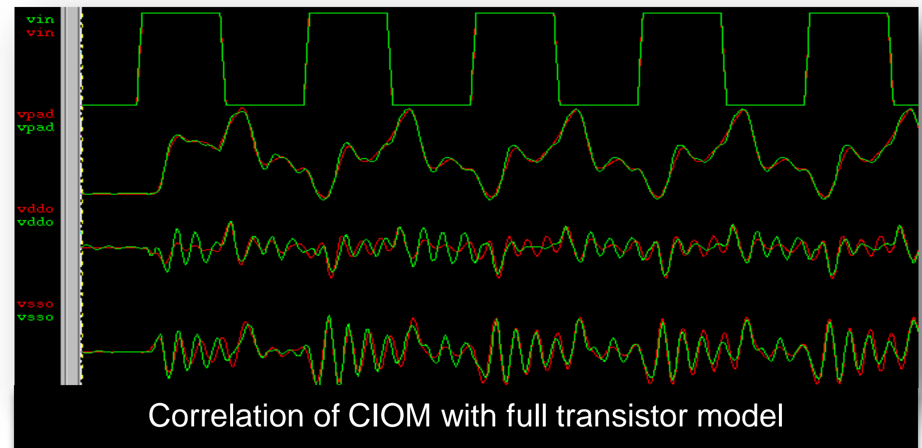
Chip IO Model – IO Behavioral Modeling
Signal Integrity Analysis & Optimization





Models Switching behavior & PG parasitics

Enables IP protection



Correlation of CIOM with full transistor model

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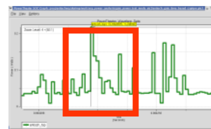
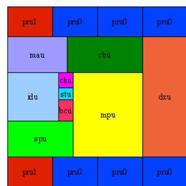
RTL Modeling for System EM Analysis

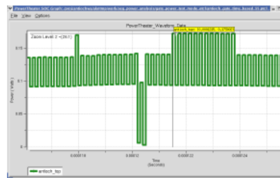
RTL design
and IP models

POWER THEATER

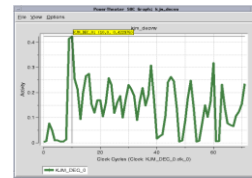




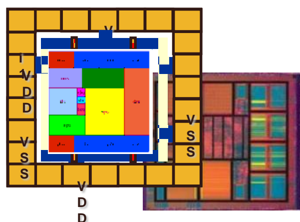
Block Average Power or Current



Cycle-average power vs. time

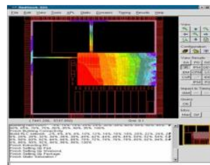


Cycle-average activity vs. time

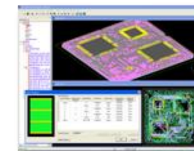


Power Grid + Floorplan

SoC Layout



Targeted vectorless DVD



On-die PDN and Pkg/PCB Signoff

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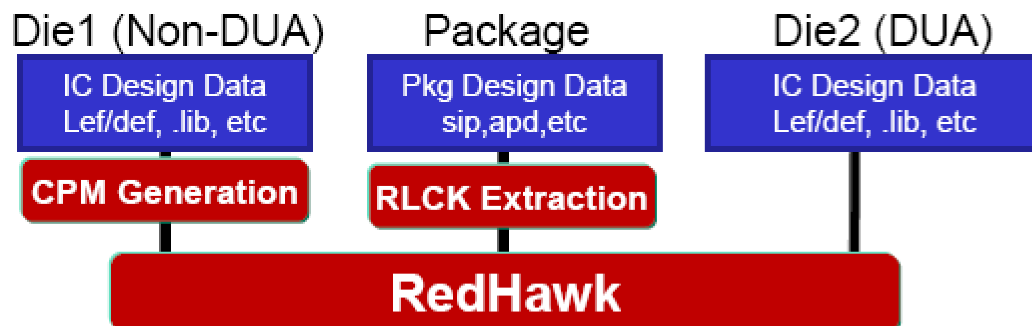
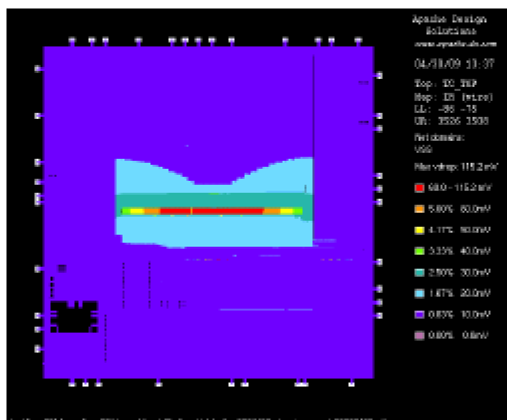
SiP IR Drop Example

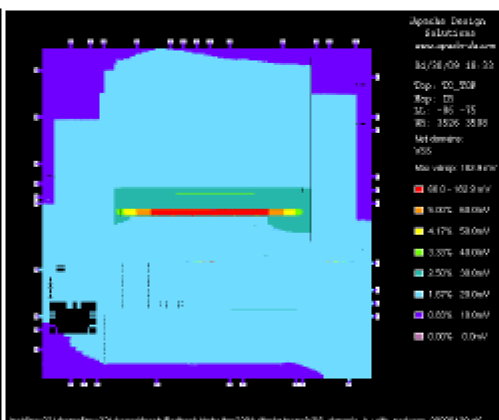




Logic DVD without Package

DVD Peak = 115.2 mV

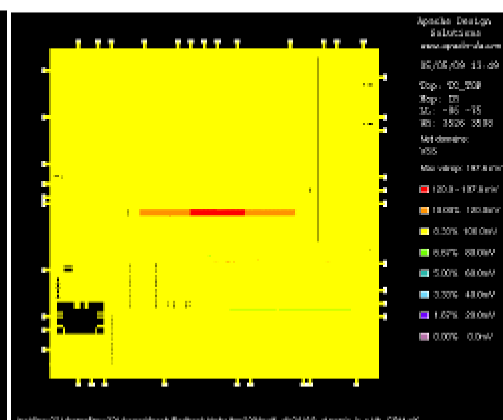
DVD Avg. = ~ 2 %



Logic DVD with Package

DVD Peak = 182.9 mV

DVD Avg. = ~ 2 - 3%



SRAM DVD with Package + ARM CPM

DVD Peak = 197.6 mV

DVD Avg. >= 8.3 %

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