IBM Technology Development

Thinking in 3D, Improving performance and modularity

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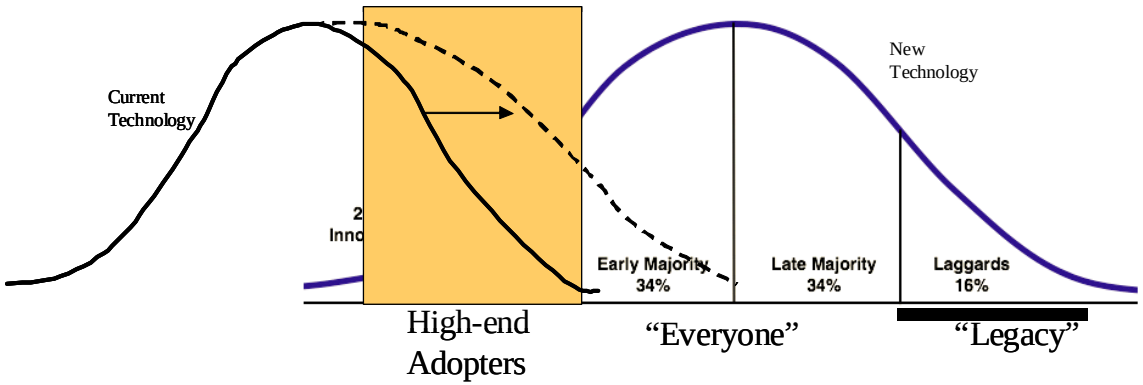
3D/TSV

- What is it? Why do we think it is interesting?
- Broader system level thought process required
- Thinking/executing in 3 dimensions
- Some Challenges for us

The evolution of thought concerning 3D application and usage

- **Although there is a fair amount of industry activity working to bring 3D (actually the via) to fruition... what is new about 3D anyway?**
  - **Concept of 3D not really new... wire-bonding, PAM, PoP, etc.**
  - **Via structure, size, shape, Lithography, and material improvements**
  - **EDA enablement / improvements (floor planning, timing, simulation, verification, test)**
  - **Interest in continuing along Moores' law course**

- **Wow factor needed, coupled with 2D thinking challenges 3D/TSV technology introduction.**
  - **A compelling reason to invest and take the risk is needed (ultimately no other way)**
  - *There is a difference between designing for 3D, and designing with 2D back-up.*
  - ***Challenges, values, general inertia of applying a new technology.***
    - **Limitations and considerations of power distribution, thermal, etc.**
    - **Necessitates a more comprehensive, system floor planning methodology**



Thru-Silicon Via technology

- So, In general, what is it ?
  - At it's base, a hole thru the semiconductor enabling connections on both sides of flip-chip devices
  - Some what different definition/process depending on your perspective and role within the industry
- Why is it interesting to the industry?
  - Tracking Moore's law, Integration, Performance, Cost, …
- What are the considerations to using this technology?
  - General shape and performance value or impact of this via capability
  - Typical new, risk / reward equations still apply
  - Application/system level view vs. floor planning impacts
  - Tools (EDA and Fab), Integration, definition, process

Potential top level values to an application

- **Performance**
  - Shorter nets,
  - Lower capacitance interconnect
- **Size / Density**
  - Moore's law
  - Smaller I/O blocks
  - Tighter integration
  - Less mass
- **Reduced power**
  - Lower capacitance and shorter nets
  - Less repower across chip
  - Less complex chip-chip I/O
- **Modularity/Reuse**
  - Mixing technologies
  - Cost

Basic I/O bandwidth performance - value of integration

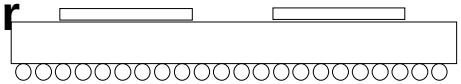
The “base”, path between two Single chip packages

Signal Path: Driver-Last Metal, ball, ~15mm package, BGA, 50mm card, BGA, ~15mm package, ball, Last Metal-Receiver

Traditional ESD devices required, driver and receiver often complex (pre-compensation, DFE, etc.)

Bus-width limited typically by package I/O count, Frequency typically limited by channel attenuation

A MCM/SiP Chip to Chip path on same carrier

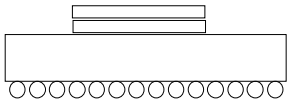


Signal Path: Driver-Last Metal, ball, ~15mm package, ball, Last Metal-Receiver

Traditional ESD devices usually still required, drivers and receivers typically less complex

Bus-width limited typically by chip I/O and ability to escape into and thru the package. Frequency less limited by channel

Stacked Devices, Chip to Chip Vertically



Signal Path: Driver-chip wire, TSV, chip wire-Receiver

ESD may be reduced, driver and receiver potentially much less complex

Bus-width limited only by TSV pitch/count (compared to the “base” above, virtually unlimited), bus frequency limited by circuits and impacts of thermal, noise, power distribution driven density.

3D/TSV additional usage considerations

- **Management of typically more items simultaneously**
  - Floor planning much more complex
  - Complexity more like system / product level than traditional 2D
    - Layer to layer interactions
    - Each layer to outside world

- **Utilization of 3D**
  - Mixing technologies
    - High value potential
      - Layer-layer interaction
      - Memory / Processor integration
  - Reusing IP
    - TSV impacts
    - Stacking multiples of the same layer
  - Signaling
    - Layer to layer, vs. off-stack or off-module
    - Driver selection / flexibility
    - Which layer do we drive off-stack or off-module from
  - Pre-planning/standardizing interconnects

3D/TSV additional usage considerations

- **Basics**
  - Thermal interaction layer-layer and at the module level
    - Hot spots
    - Where should the high power layer go?
  - Electrical
    - Planning for voltage requirements, now and future
    - Timing, clocking,
  - Structure and stack effect on electro-migration, current limitations…
- **Other**
  - Test
  - Debug
  - Etc.
- **Organizational effects**
  - Module/System integration visibility

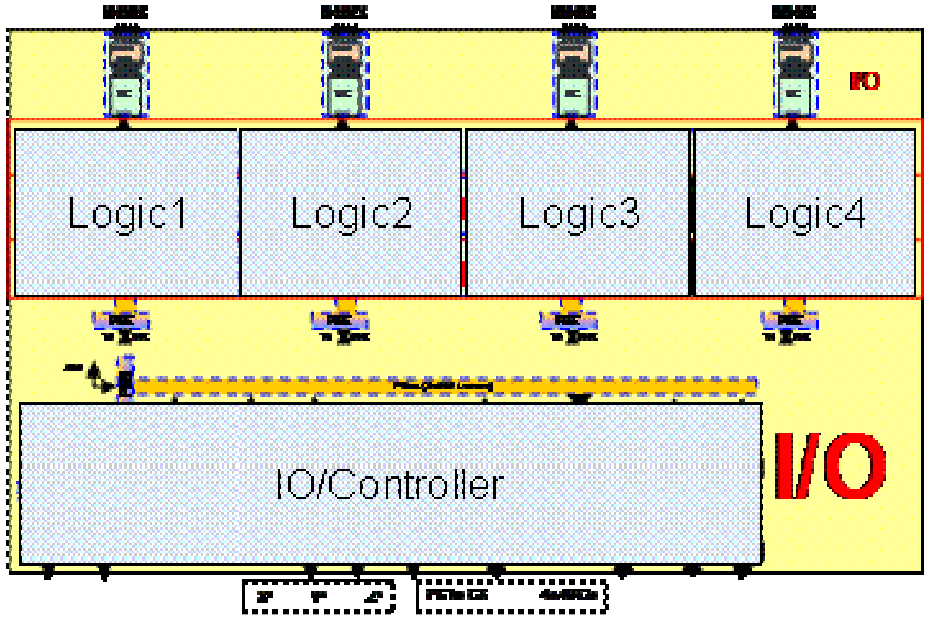
An example thought flow

Structure / stacking etc.

Baseline - How to extend a the range of a current product

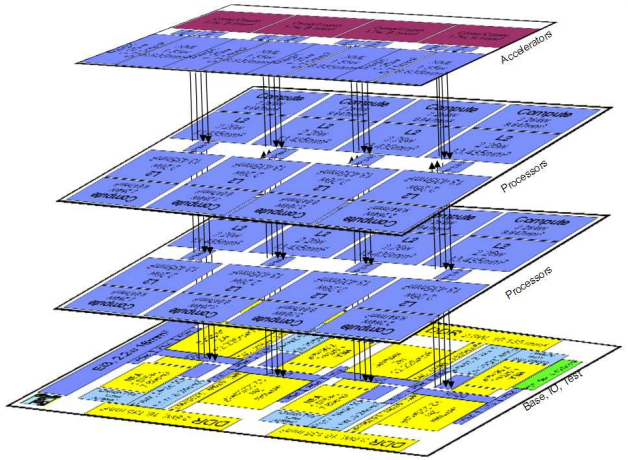
Extending design / increasing modularity/reuse

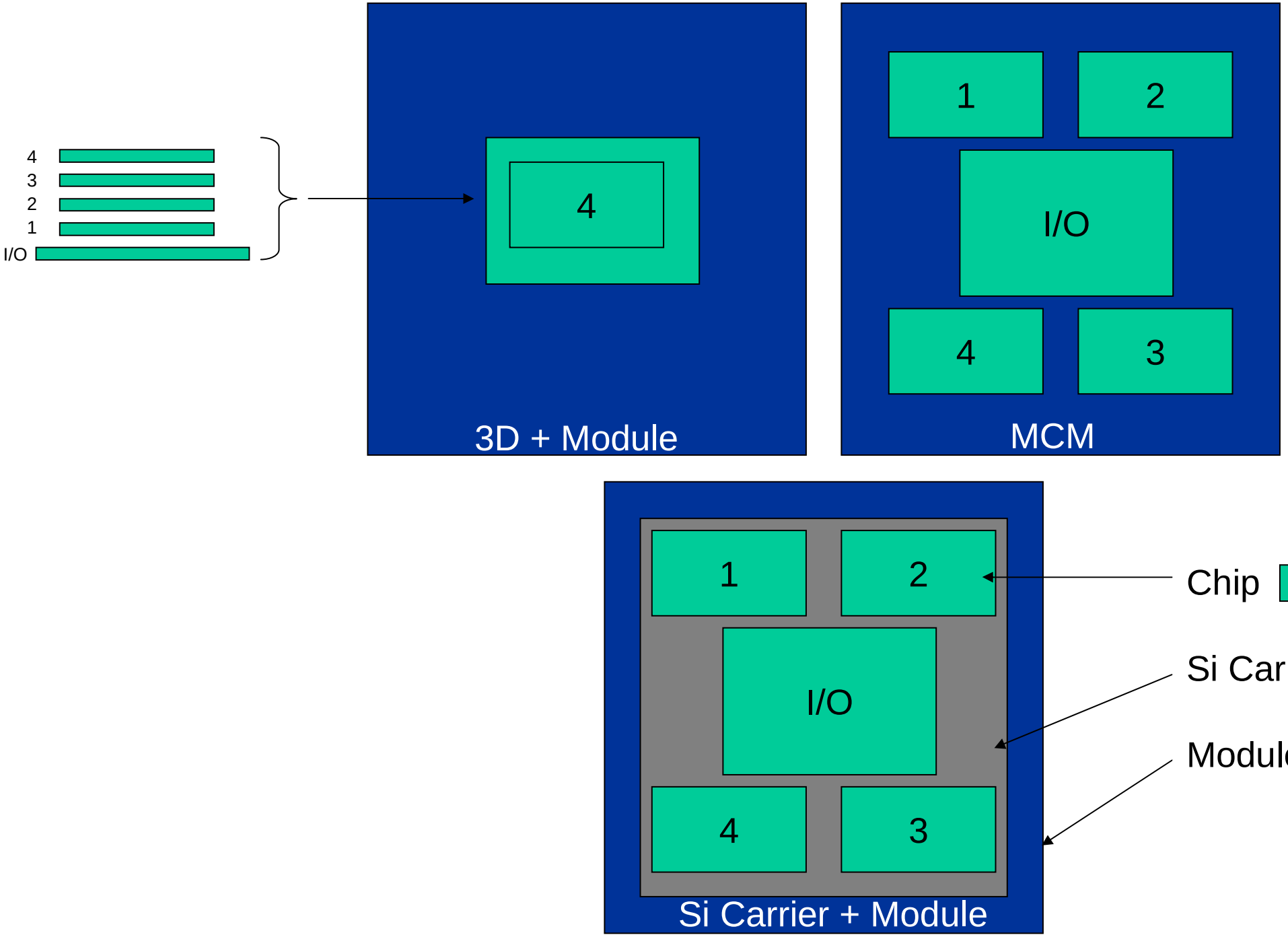
► **Creating a 4X capable product extension**



Essentially repeat 4 times the function of the original product

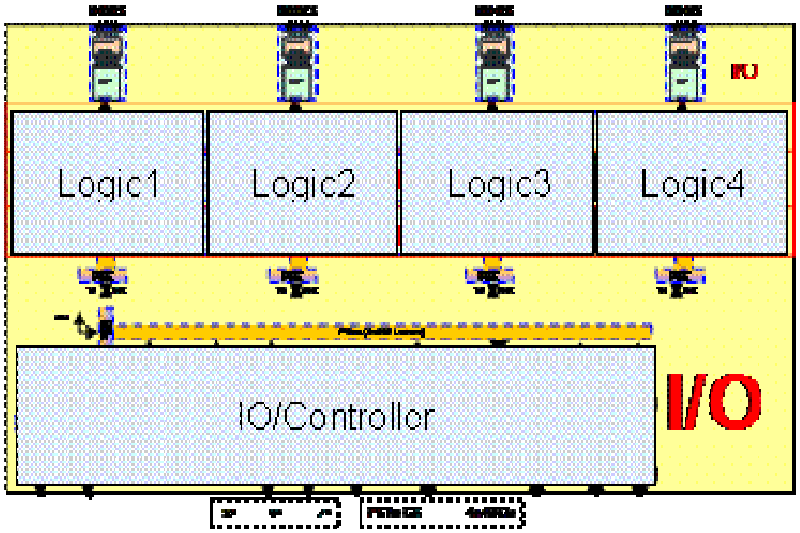
- Performance of Internal interconnect bus increased by changing the direction of the flow. I/O bandwidth value exploited



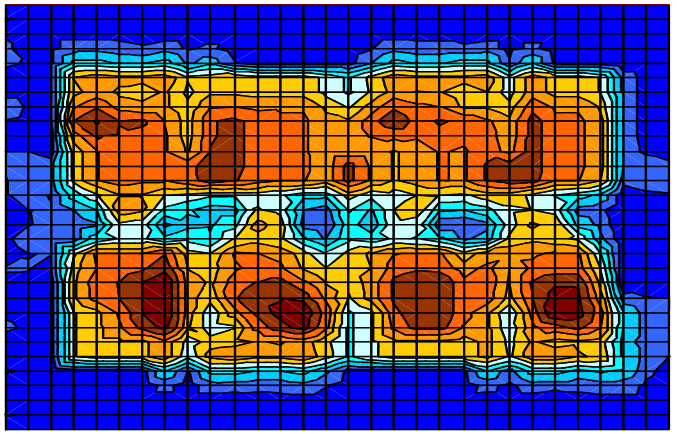

4
3
2
1
I/O
4
3D + Module
1
2
I/O
4
3
MCM
1
2
I/O
4
3
Si Carrier + Module
Chip
Si Carrier
Module

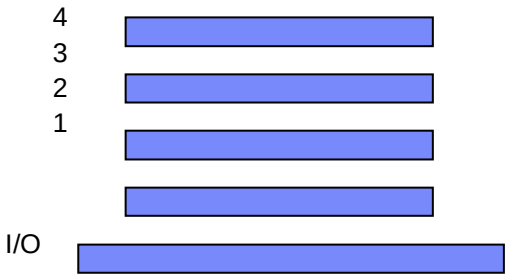
Extending design / increasing modularity/reuse

► Proposed 3D Configuration

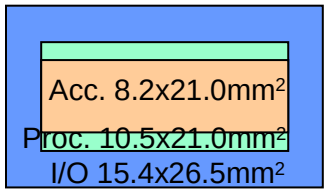


Aggregated power density

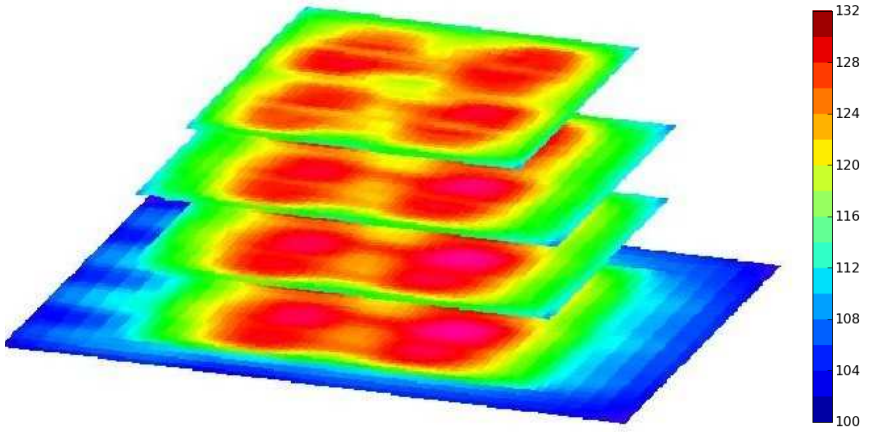




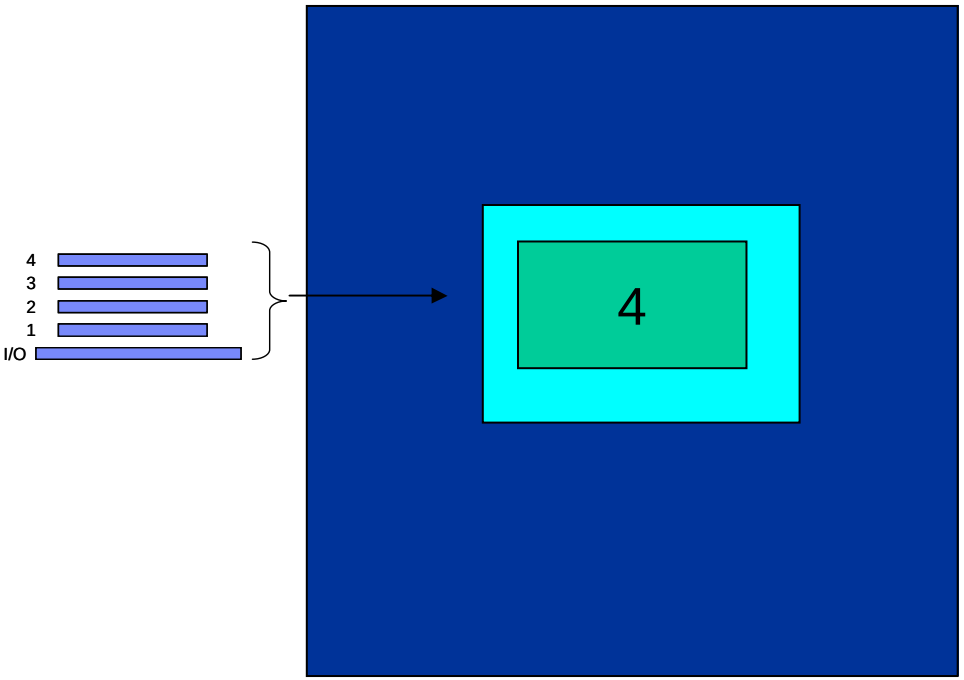
Top view

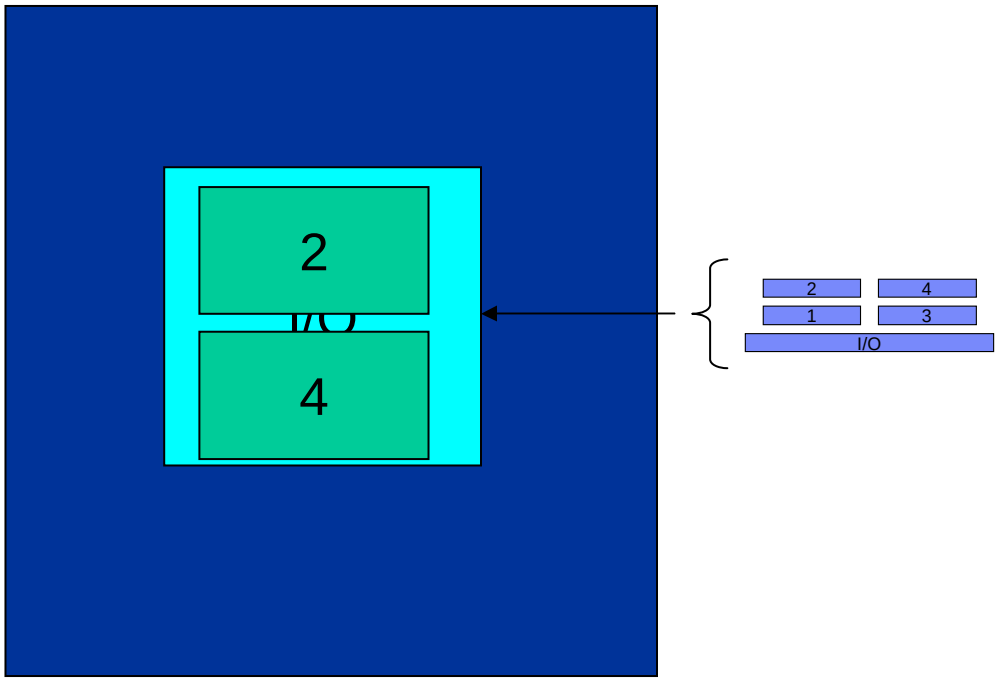


3D Thermal Map



Alternative 3D Stack Sequence





5 High Stack

“Paired” 3 High Stack

- add 2x2.5mm wings to I/O layer

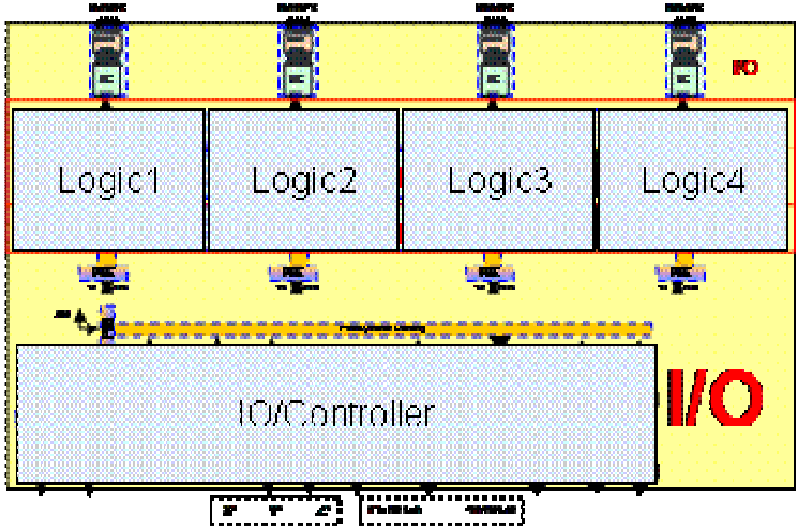
- - 14.5x21mm => 19.5x21mm
- - ~100mm2 area adder

- change aspect ratio of I/O layer + wings

- - 14.5x21mm => 17.5x17.5mm
- - still need to add ~ 50-65mm2

Extending design / increasing modularity/reuse

► Proposed 3D Configuration



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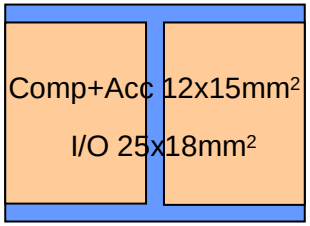

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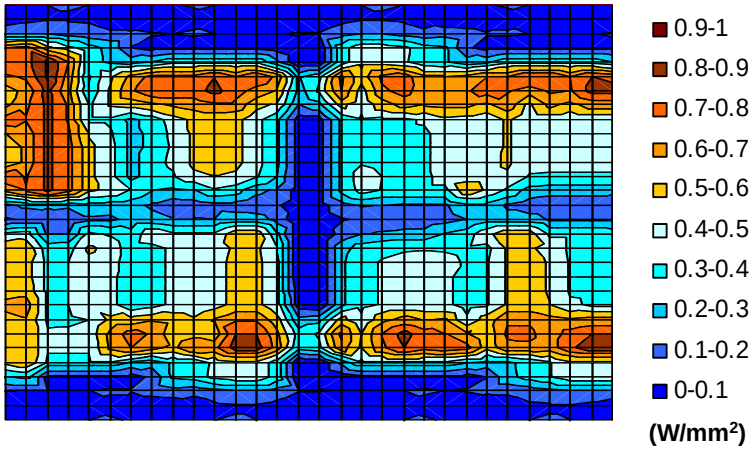

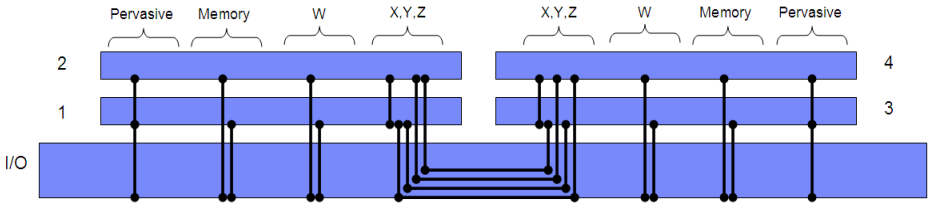

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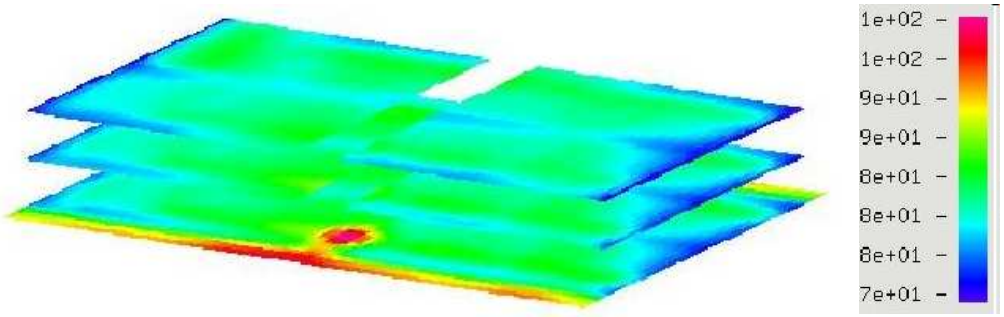

Challenge for us

- 3D technology optimization requires 3D thinking, and system level thought processes.
- Floor-planning tools/methodology must continue to evolve as the potential capability enabled by 3D/TSV drives increasing complexity.