Signal Integrity Design of TSV-Based 3D IC

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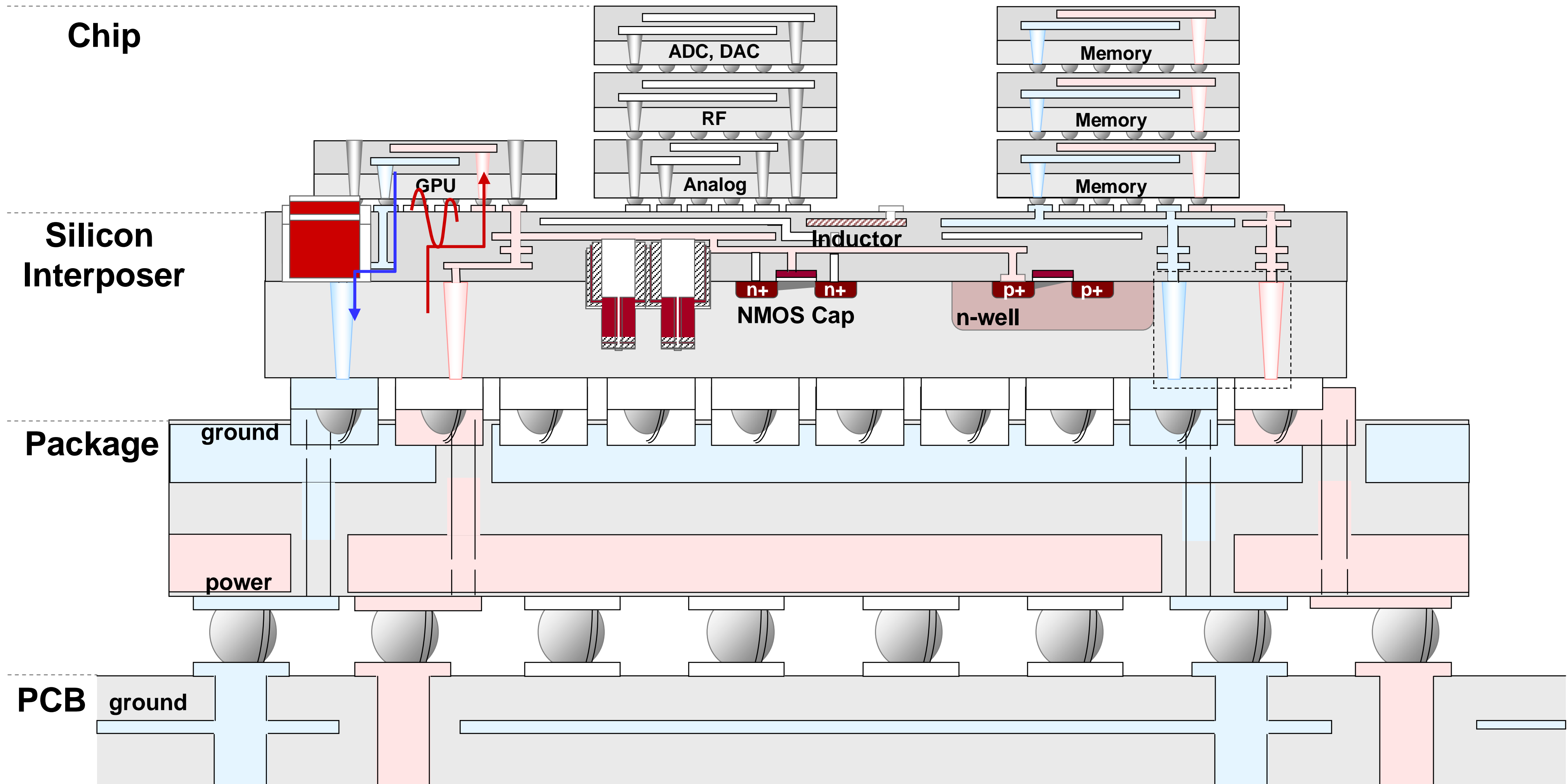
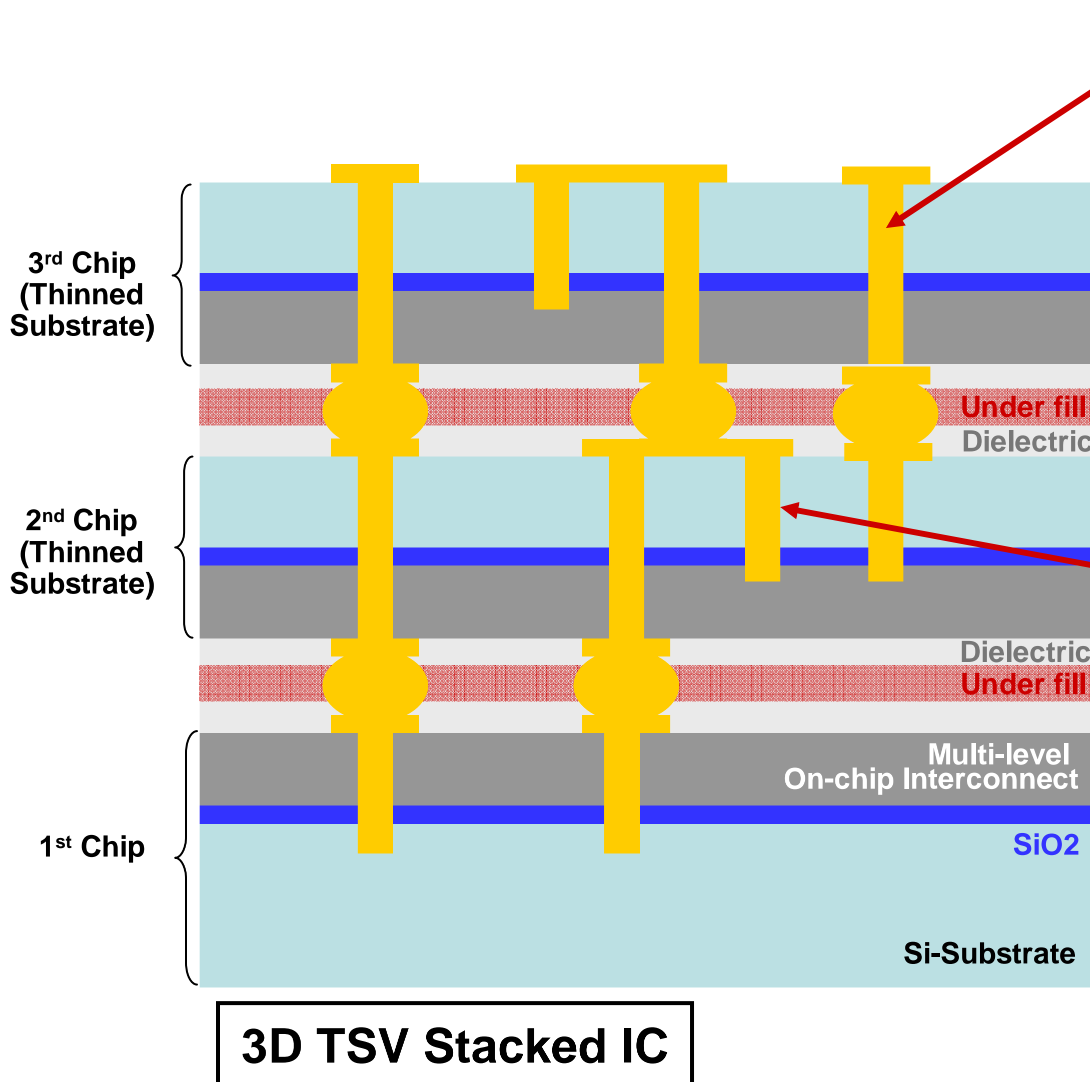
TSV Based 3D IC



Major Advantages of TSV-based 3D IC

- Large interconnection density
- Small for factor
- High performance: high-bandwidth, high I/O counts
- Low power
- Potentially low cost

Key Technology for 3D IC: TSV (Through Silicon Via)

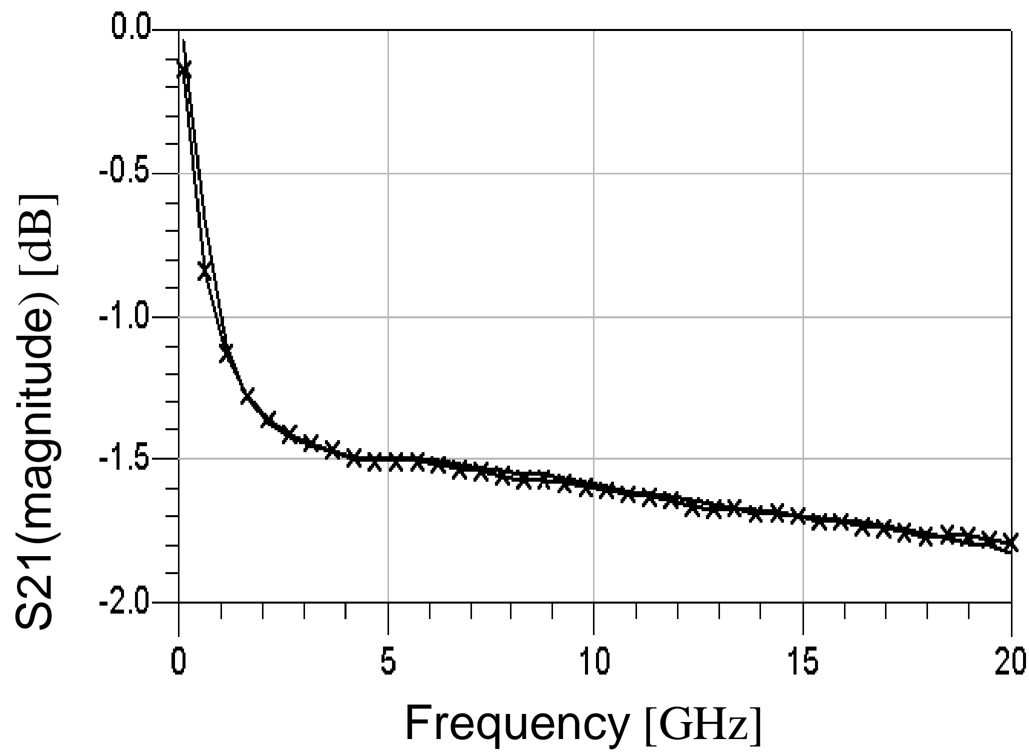


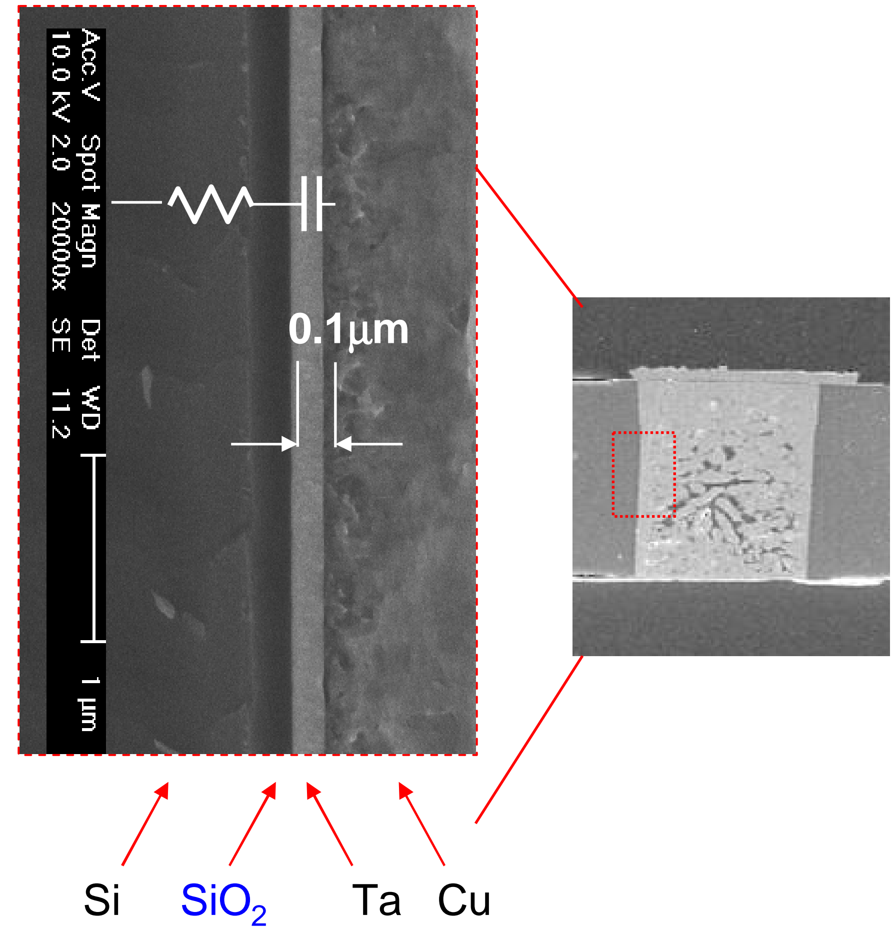
3D TSV Stacked IC

- Short Interconnection Length
  → Reduced Delays
  → Low Impedance for PDN
  → Low Power Consumption
  → Heat Dissipation Through Via

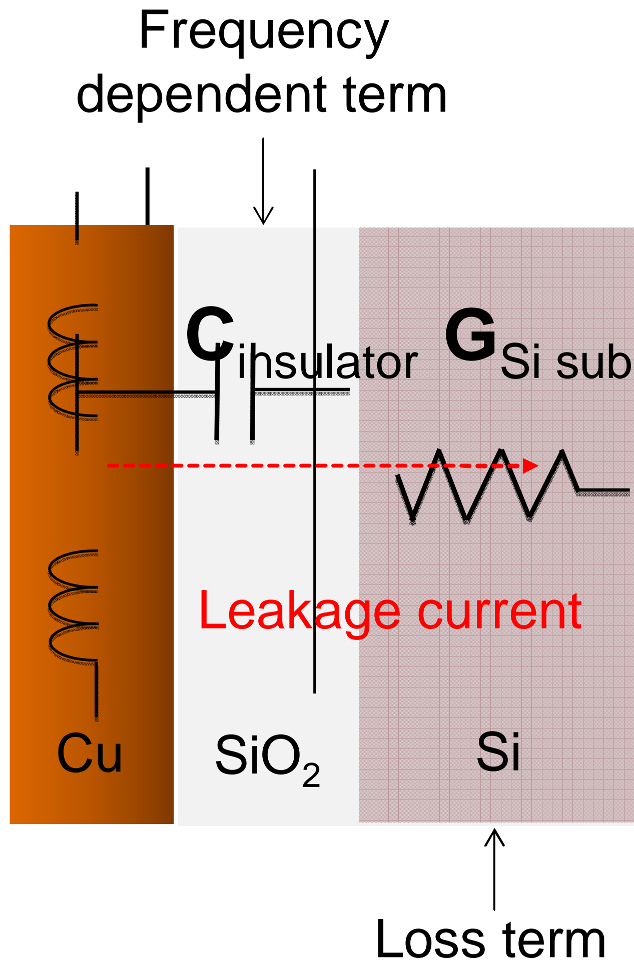
- Less Space for Interconnection
  → High Density Chip Wiring
  → Large Number of I/O
  → Small Area Package

High-frequency Channel Loss in TSV





Frequency-dependent Loss of Through Silicon Via



Insertion loss (dB)

0
-1
-2
-3
-4
-5
-6

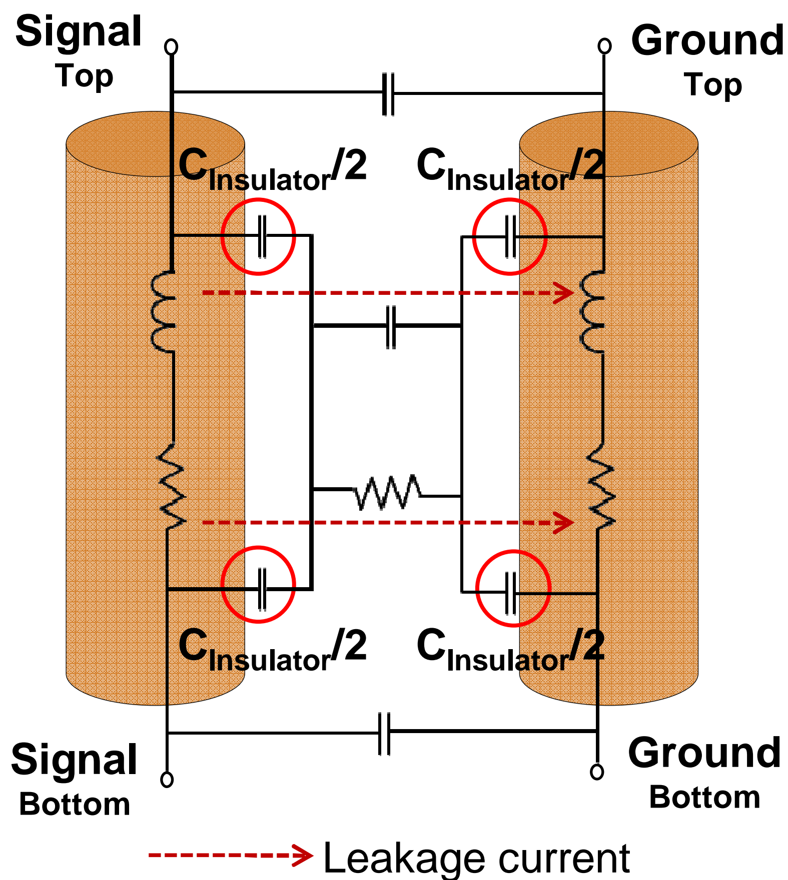
Capacitive region

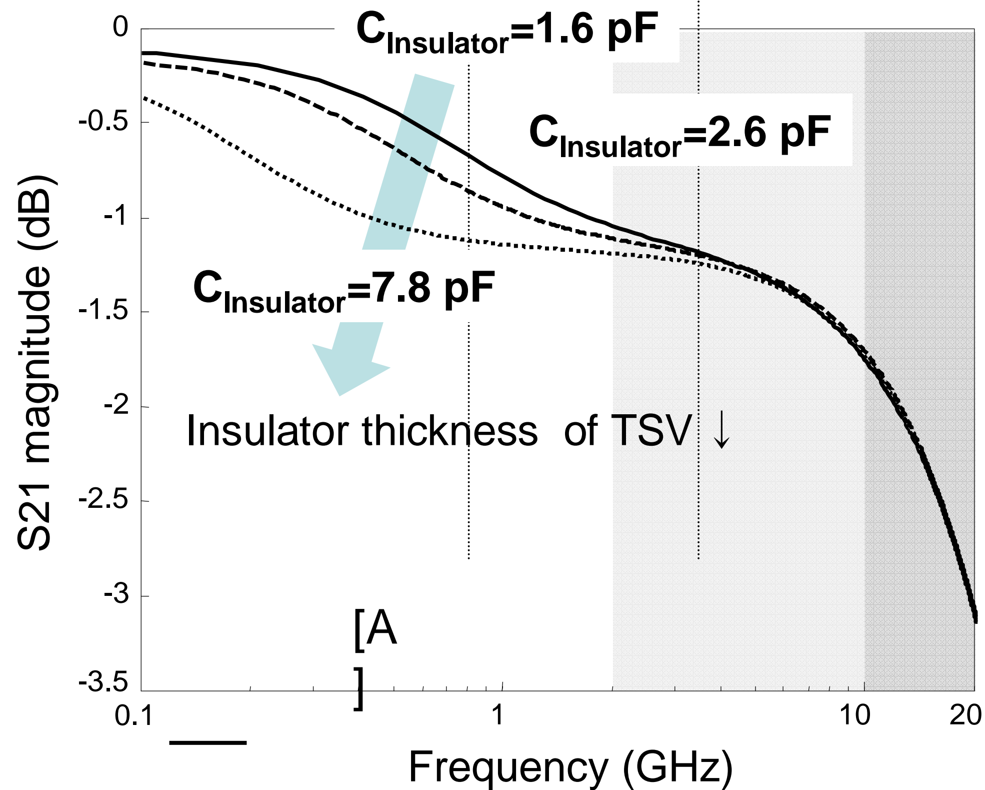
Resistive region

0.1 1 10 20

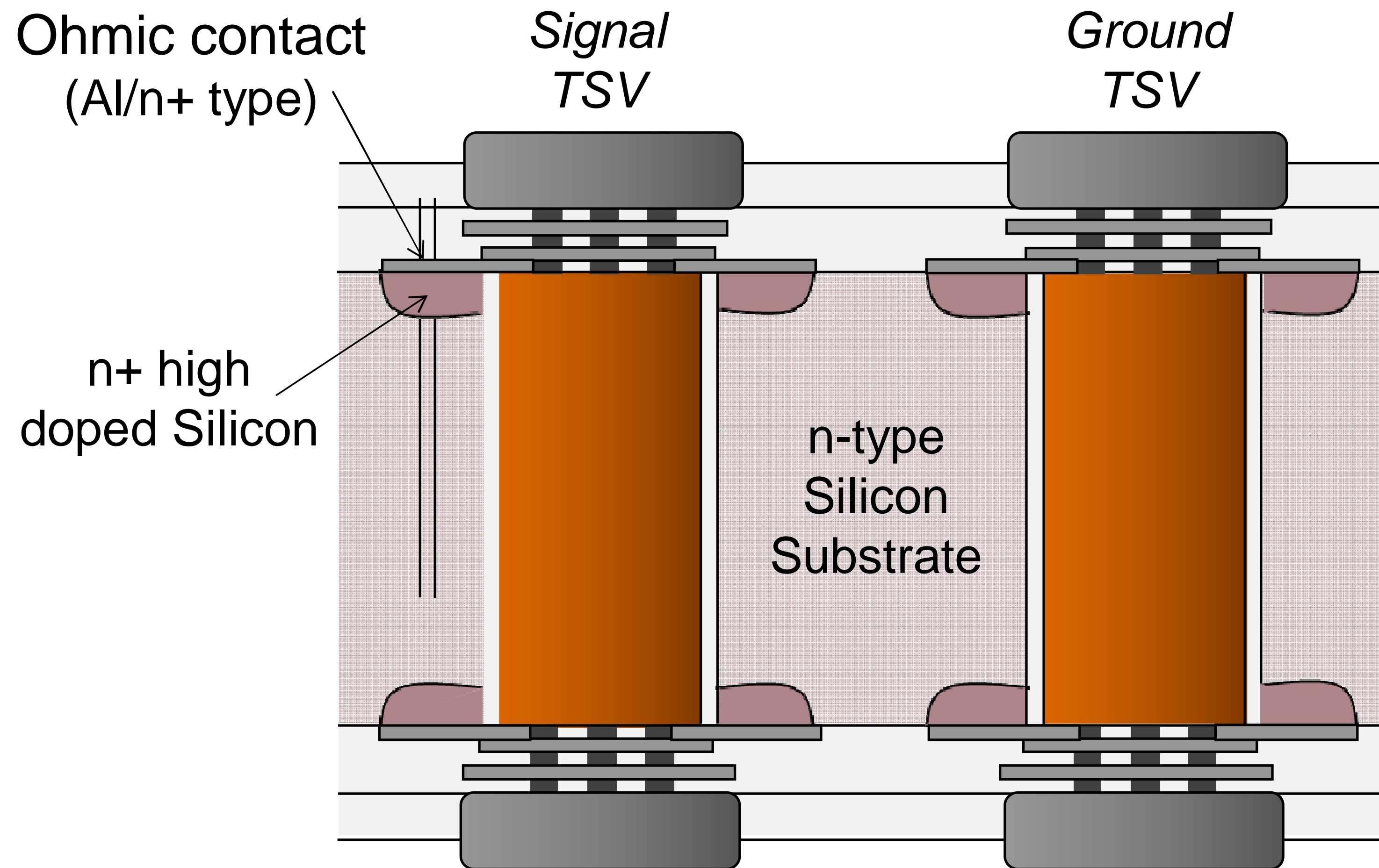
Frequency (GHz)

TSV Channel Loss with Various Insulator Thickness of TSV

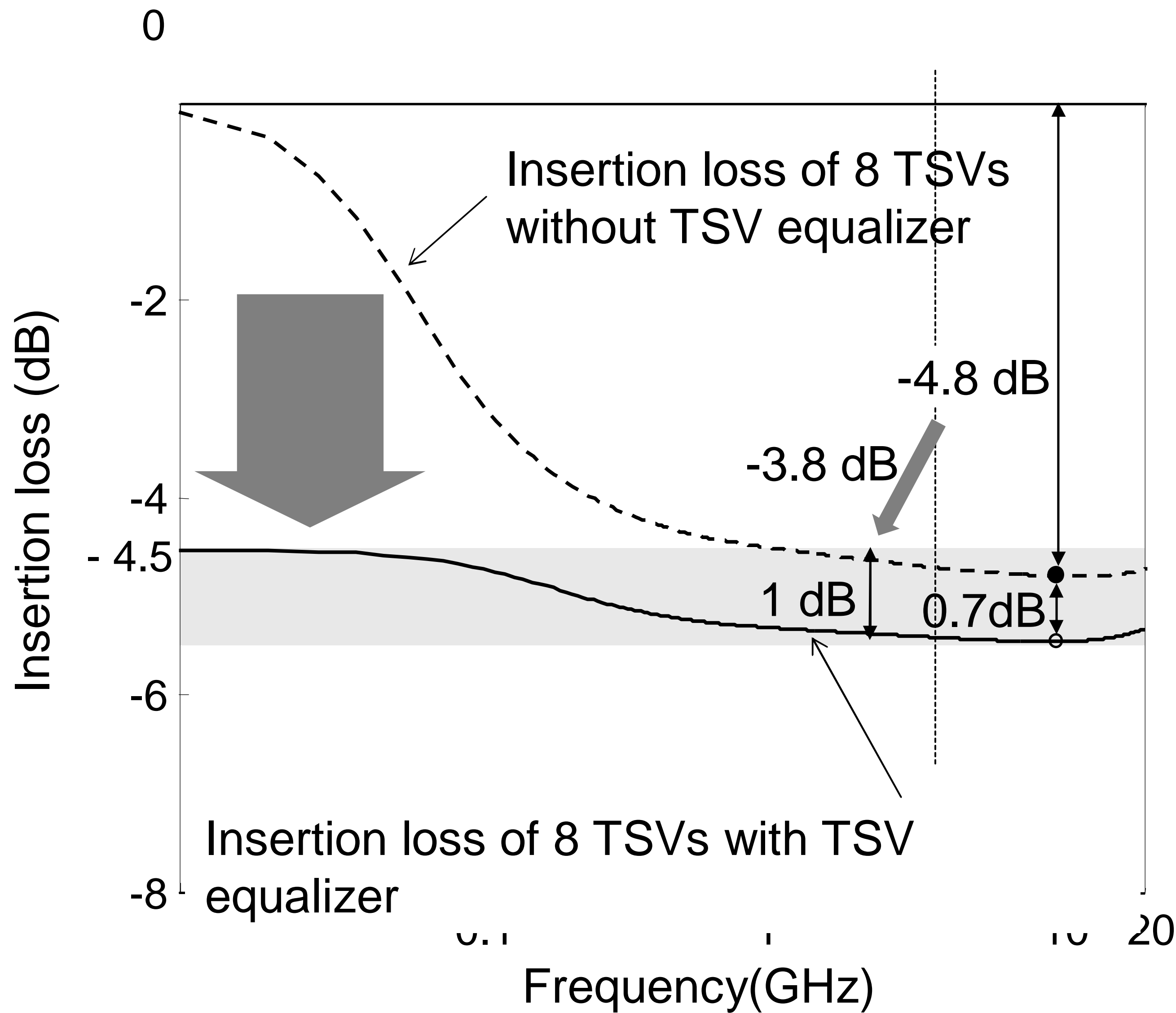




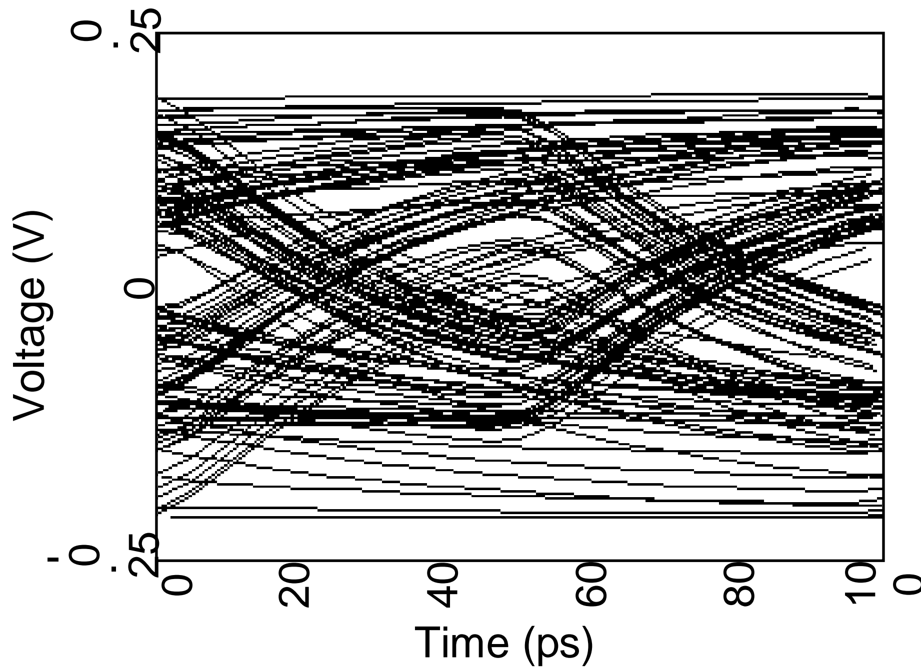
The Proposed TSV Equalizer using an Ohmic Contact

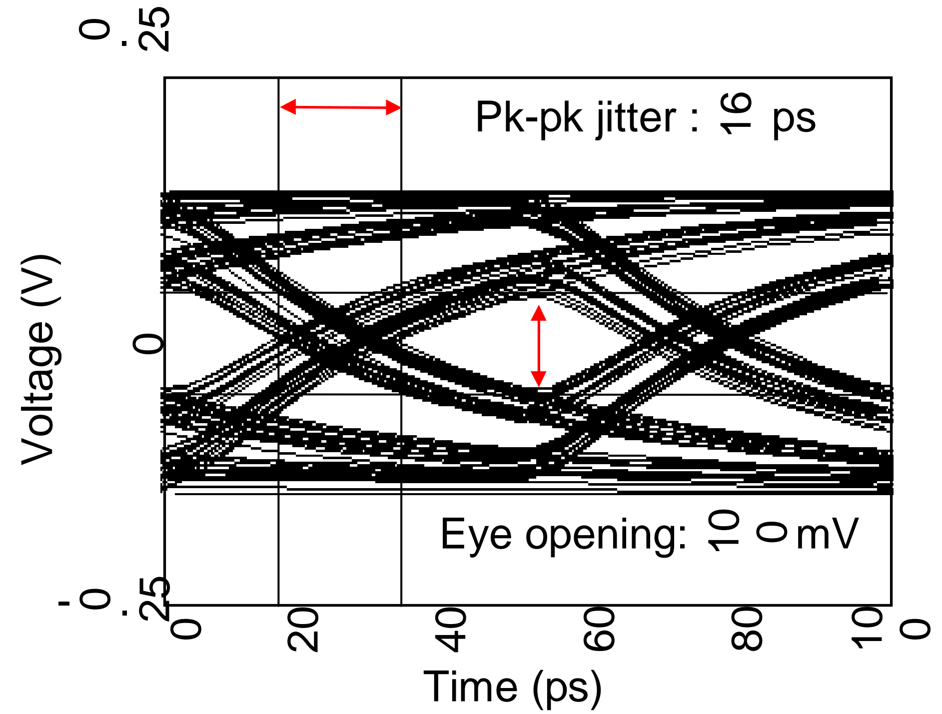


TSV Equalizer Performance



Eye opening by the TSV Equalizer

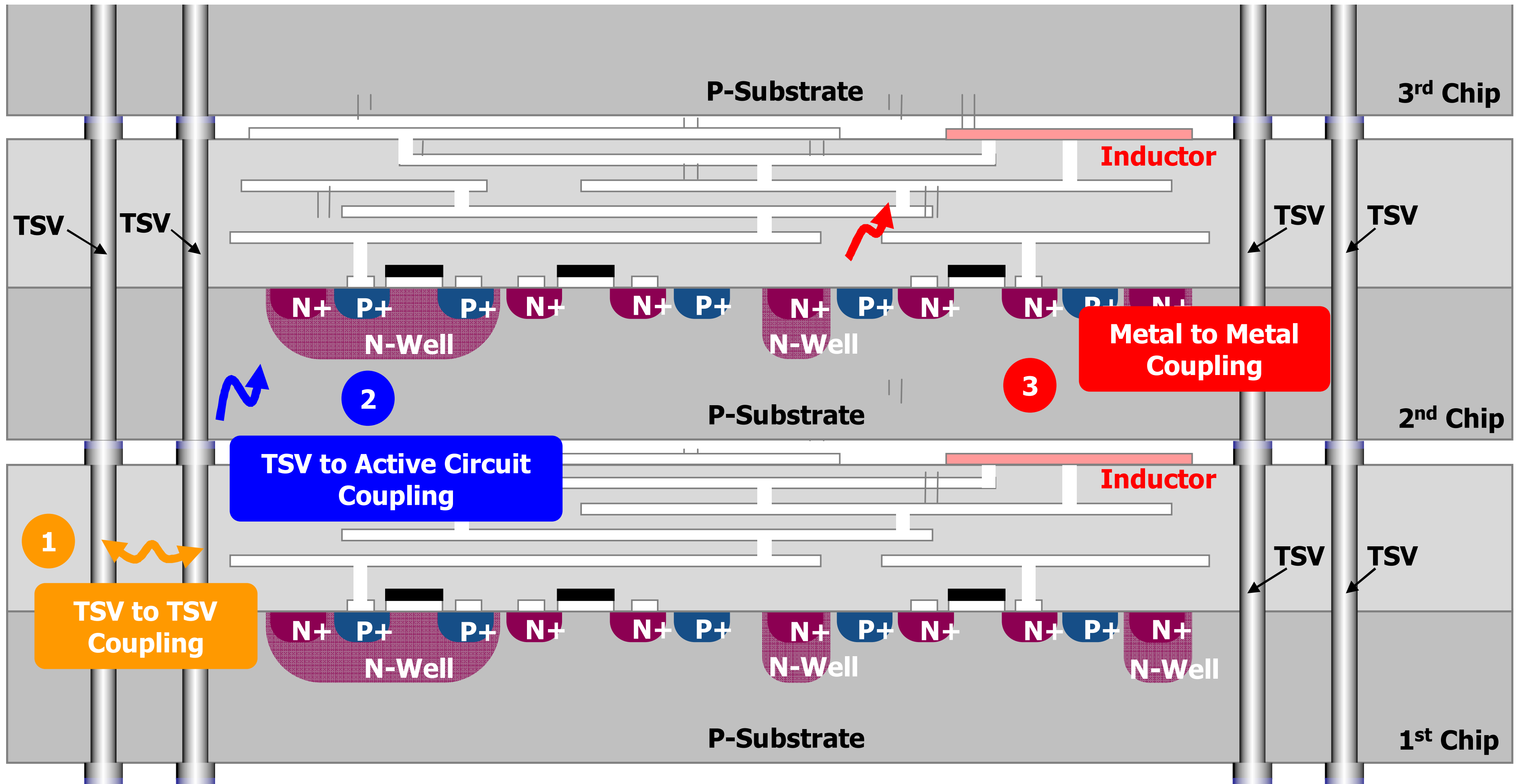




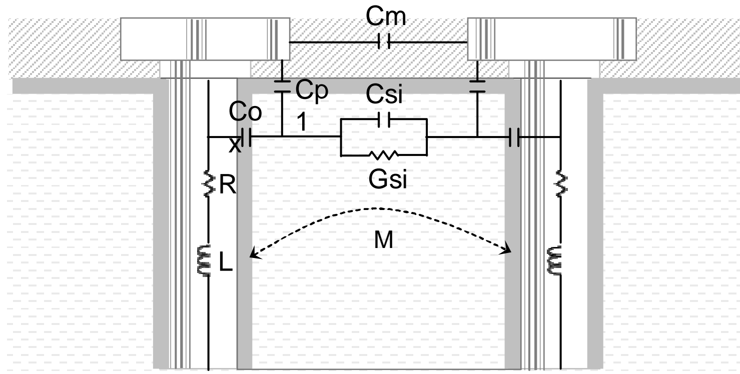
High speed channel loss by TSV

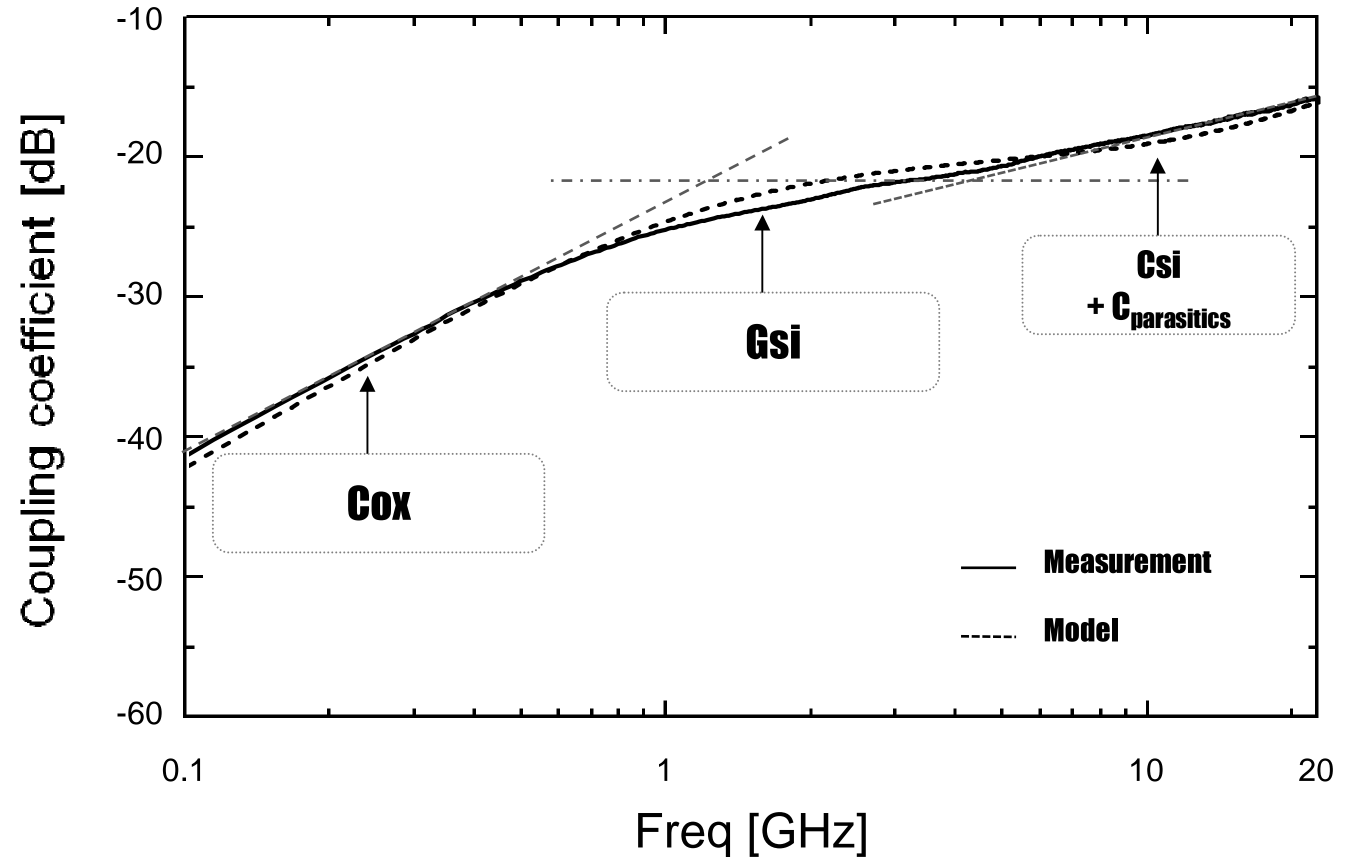
- High frequency loss
- Non uniform loss
- Loss increases as higher die stack and TSV numbers
- Passive and active equalization methods needed

Noise Coupling Paths in Stacked Dies using TSV

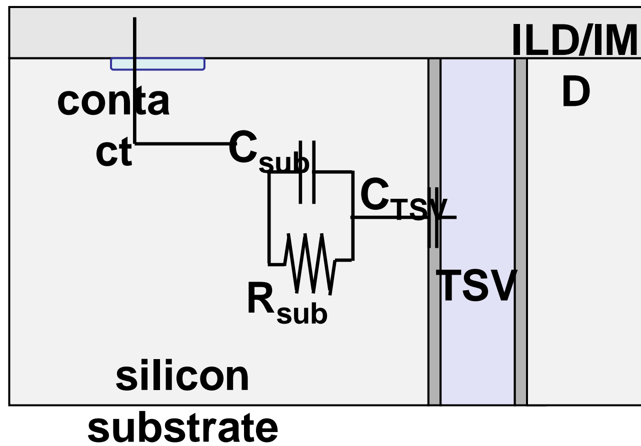


Coupling between TSVs

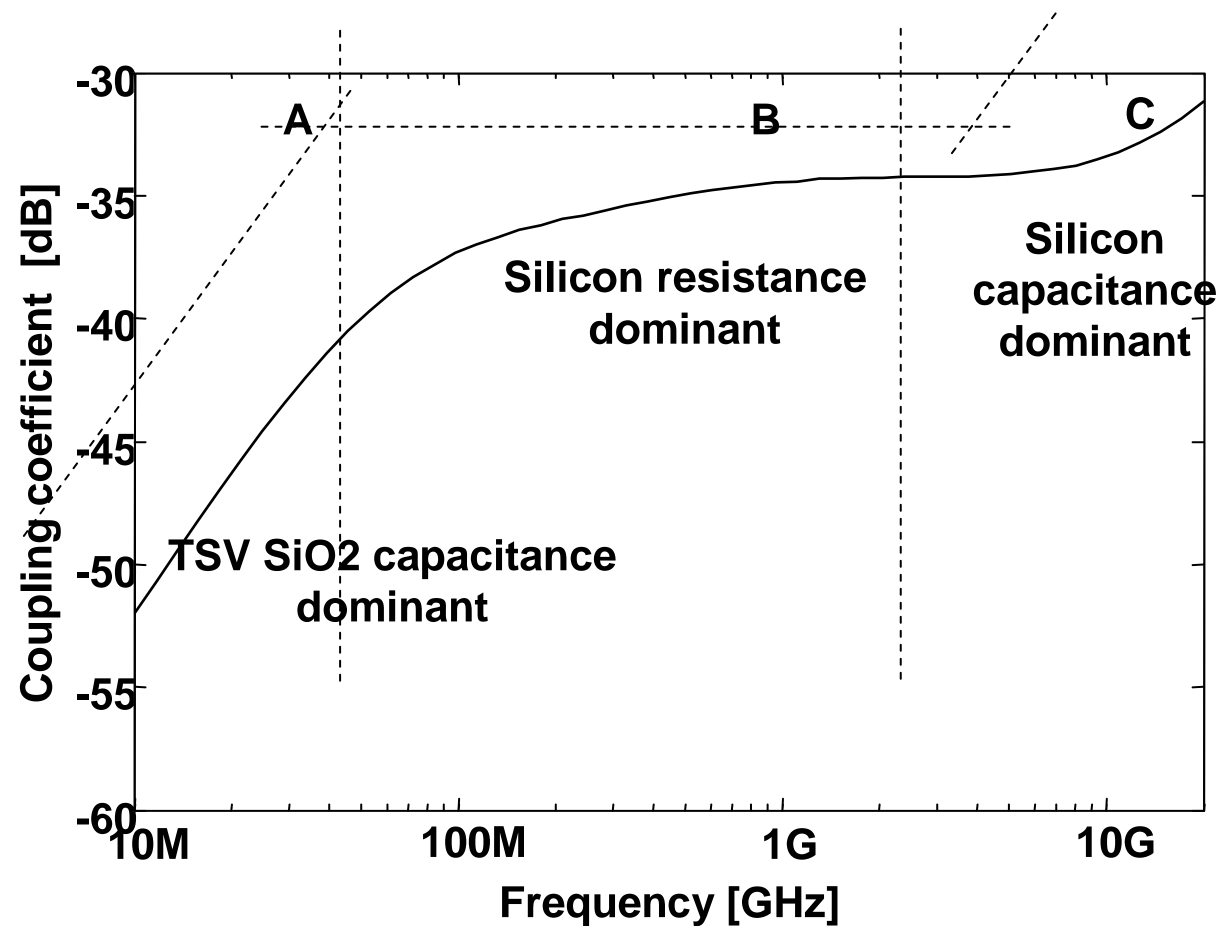




Noise Coupling from TSV to Active Circuits

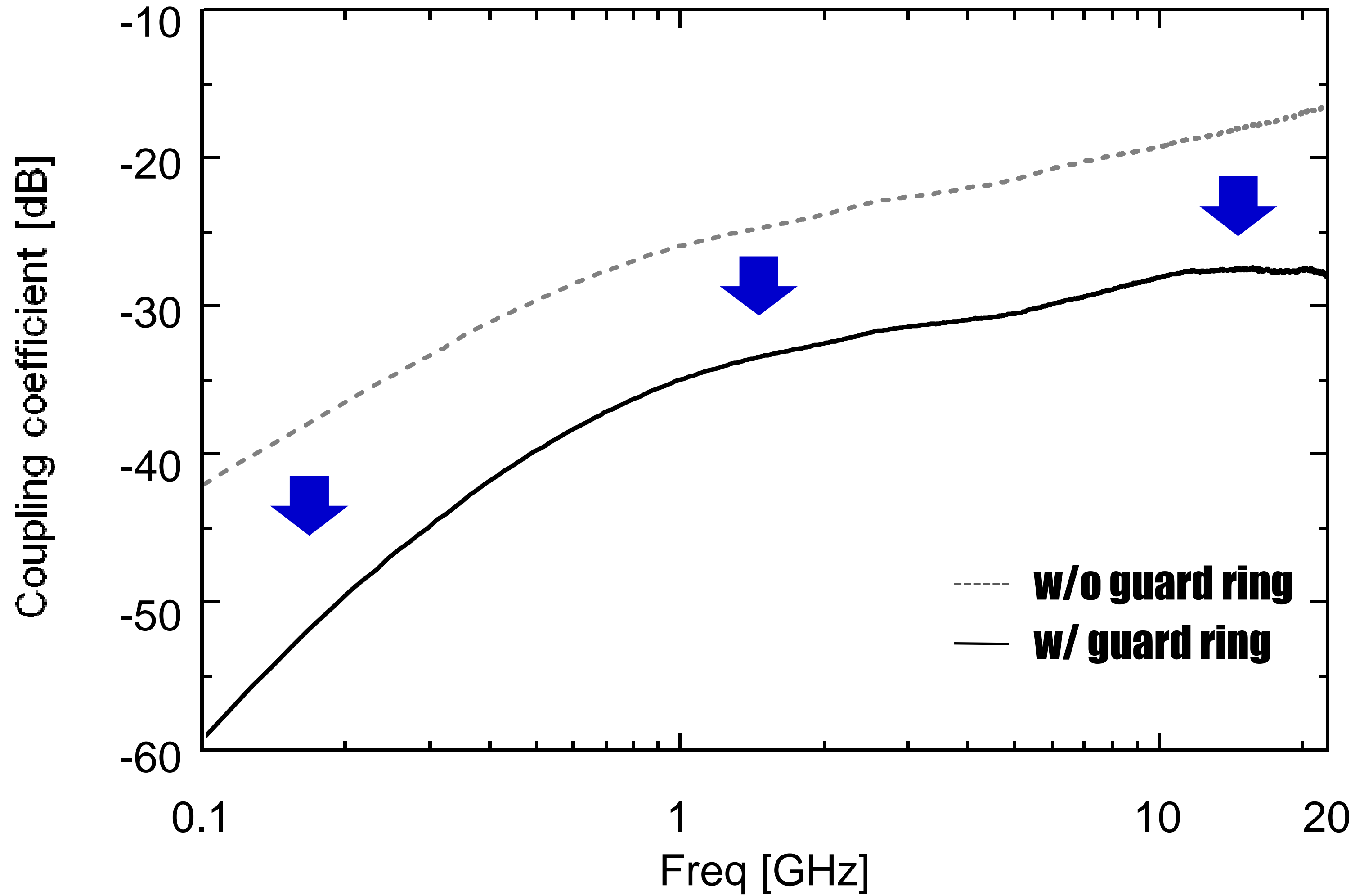


Distance between contact and TSV : 100 μm
Substrate height : 100 μm
TSV diameter : 30 μm
TSV SiO_2 thickness : 0.5 μm

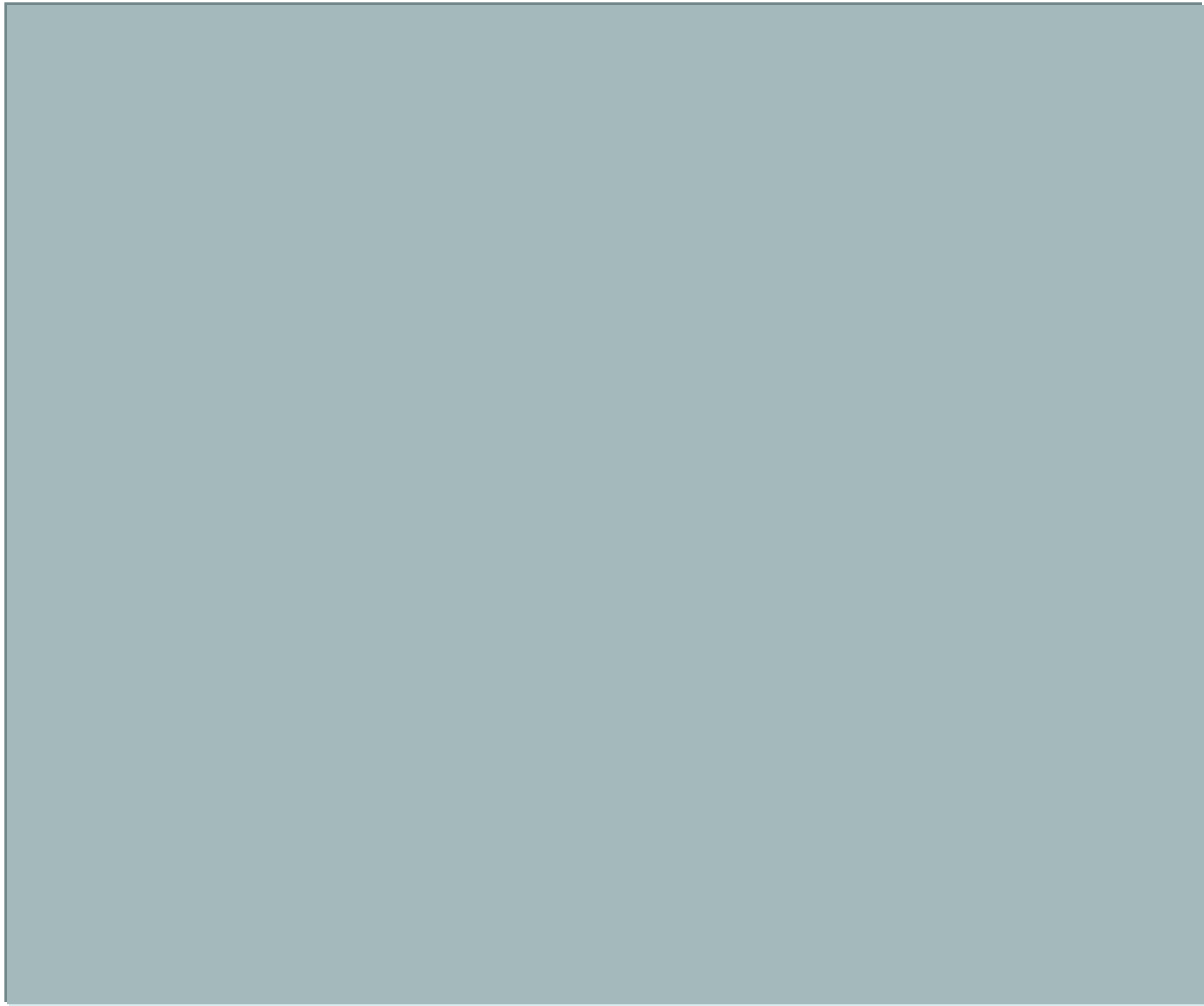


Shielding Methods for TSV Coupling

Shielding Effect Measurement: Guard Ring



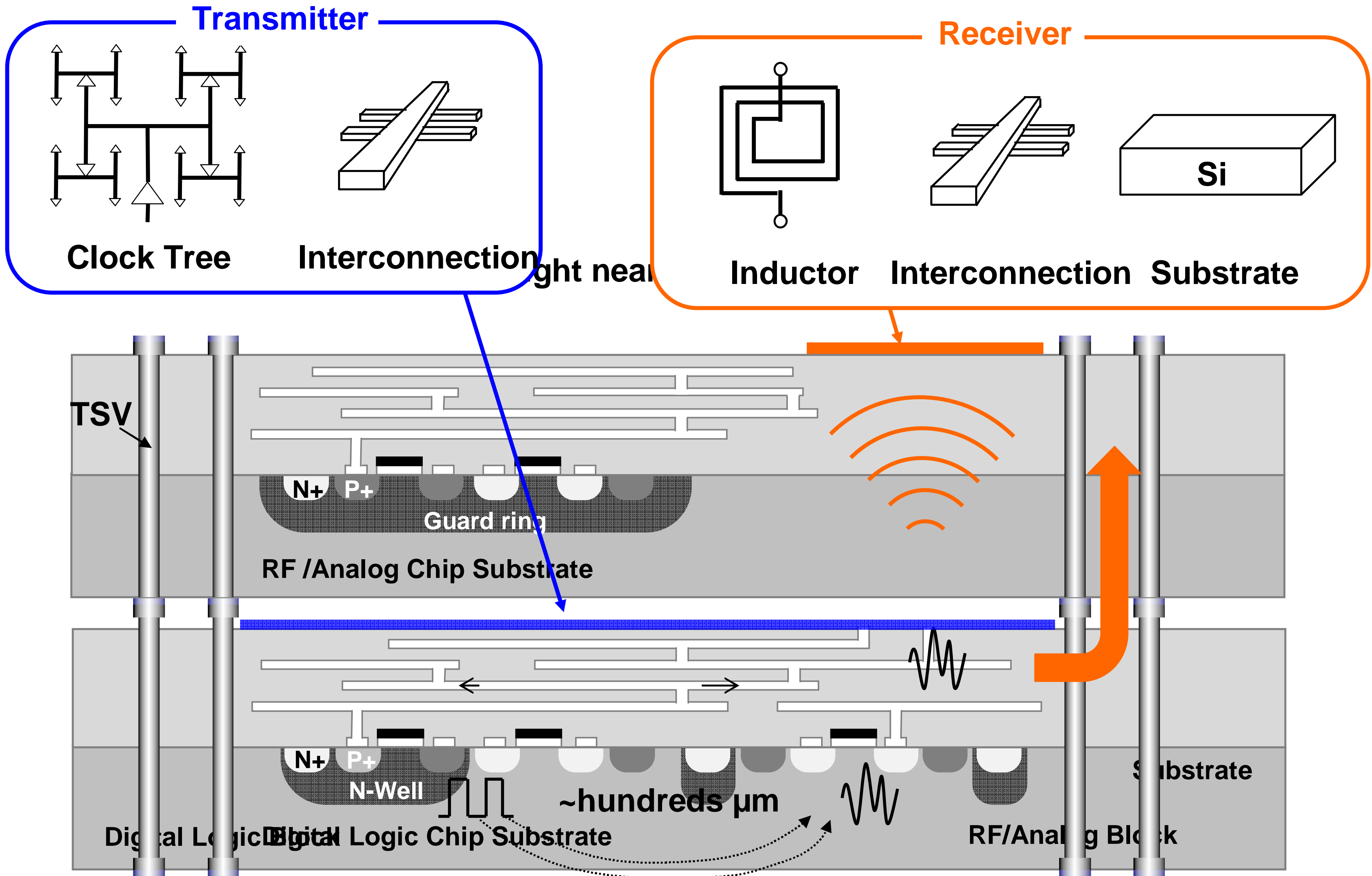
Shielding Methods for TSV Coupling



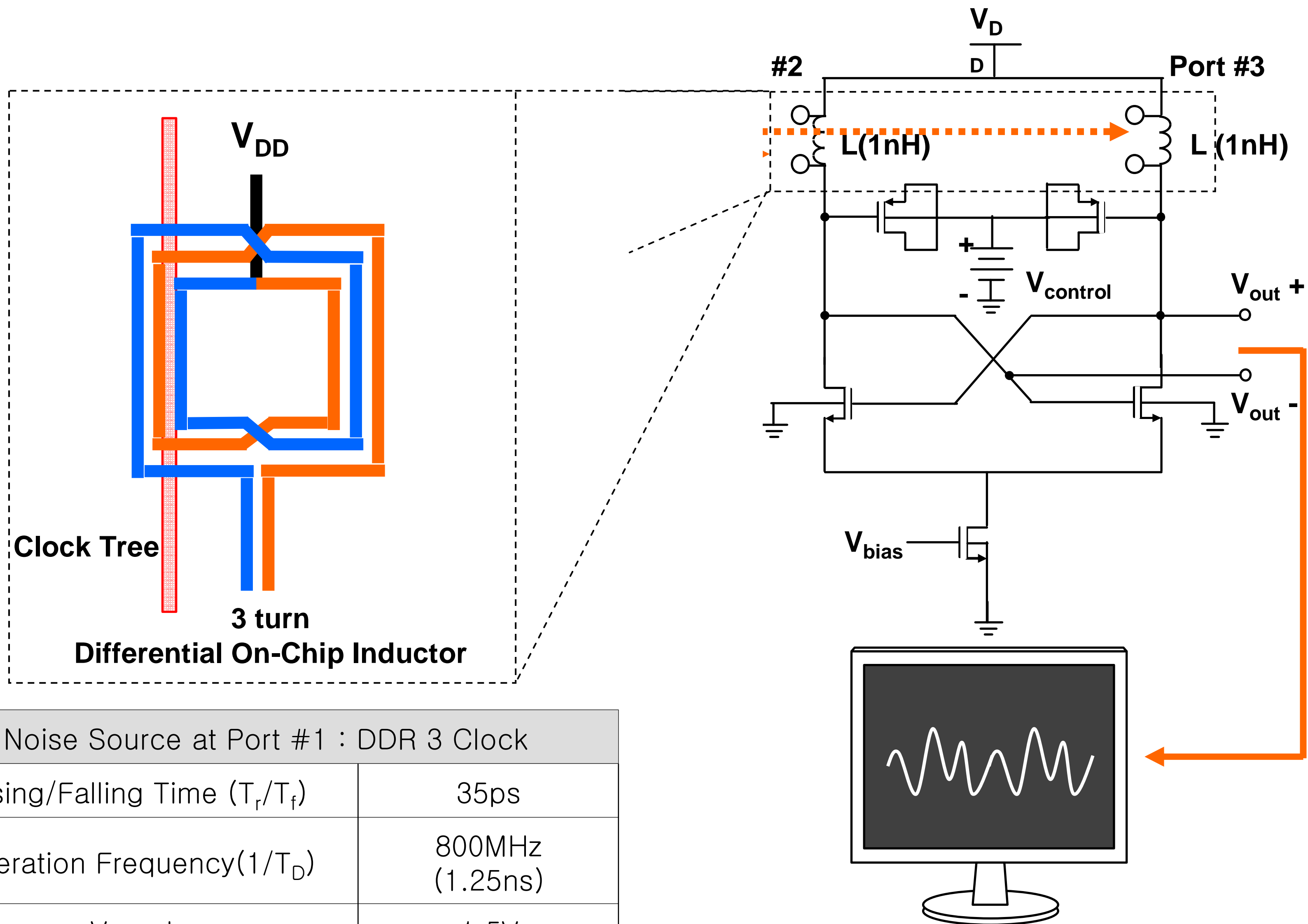
Crosstalk between TSV

- High frequency coupling
- Dependent on TVS designs: dimensions and materials
- Proper shielding methods are needed
- Shielding structures can be significant overhead of chip area
- Special I/O scheme may be needed to compensate or to avoid the crosstalk effects

Vertical Noise Coupling Issues in Mixed-Signal 3D-IC



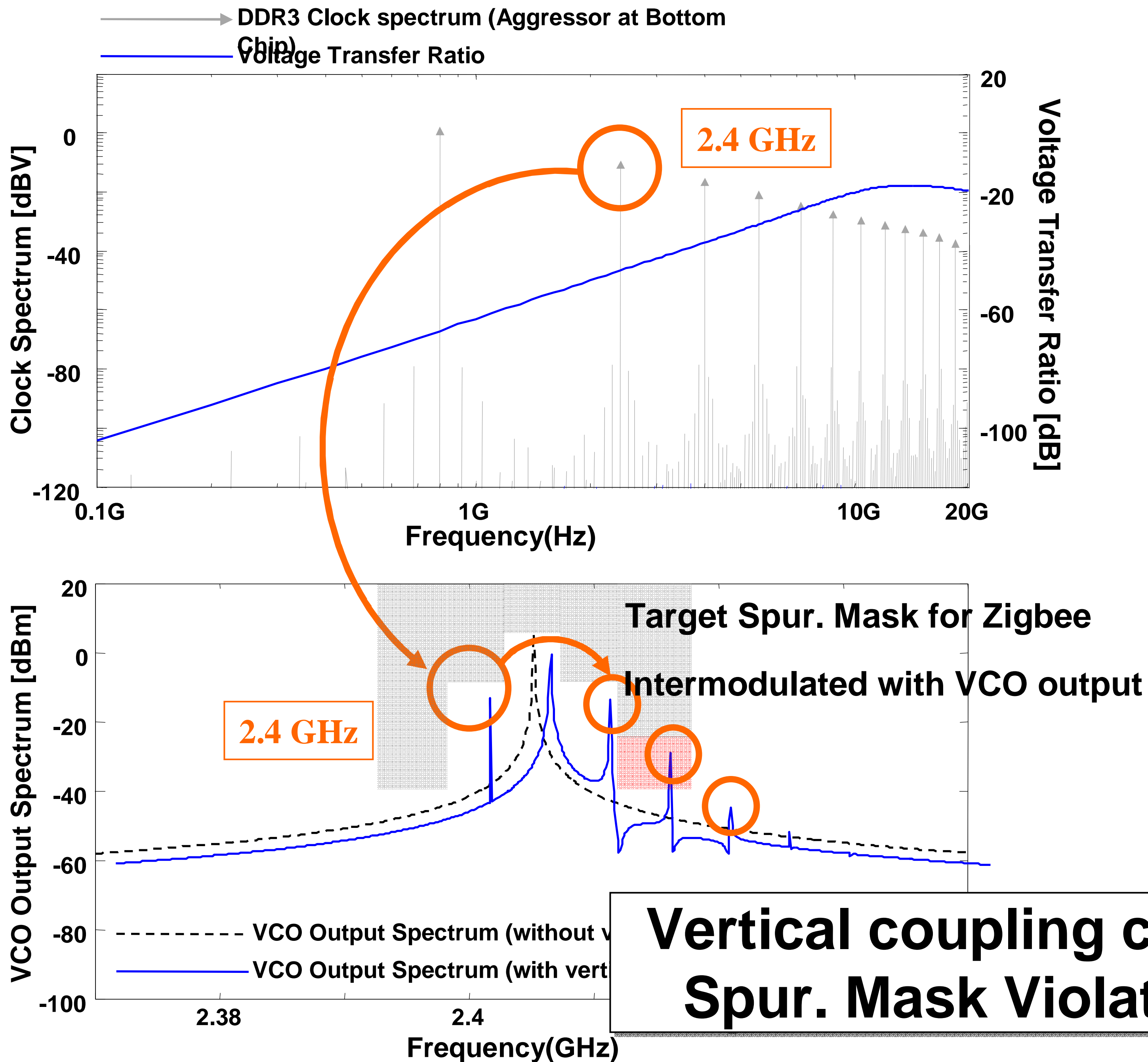
3D IC for 2.4GHz VCO in Zigbee module



Noise Source at Port #1 : DDR 3 Clock	
Rising/Falling Time (T_r/T_f)	35ps
Operation Frequency(1/T_D)	800MHz (1.25ns)
V peak	1.5V

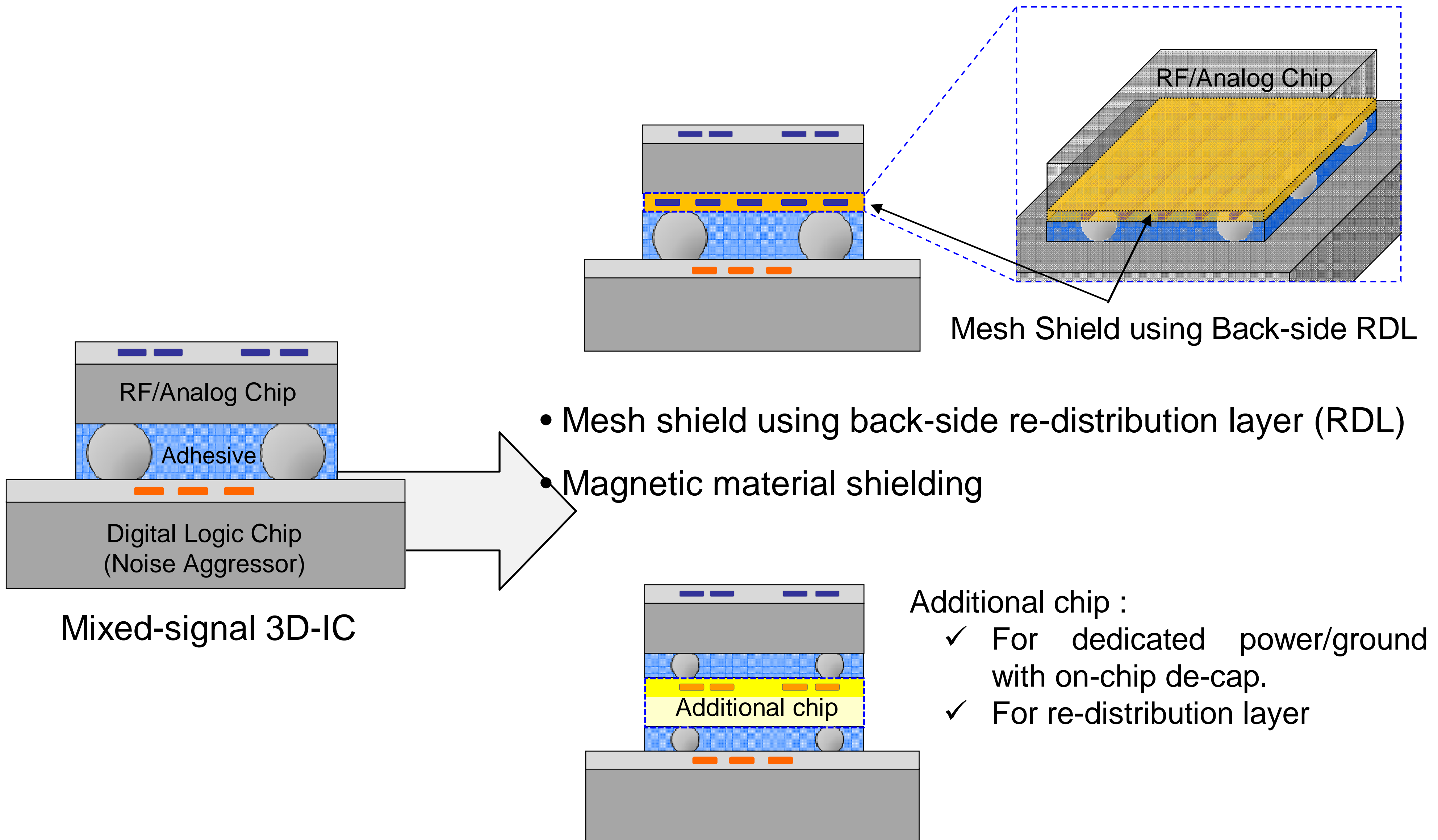
Spur. & Phase noise at VCO output

Impact of Vertical Coupling on VCO Output Spur.



Vertical coupling causes Spur. Mask Violation !

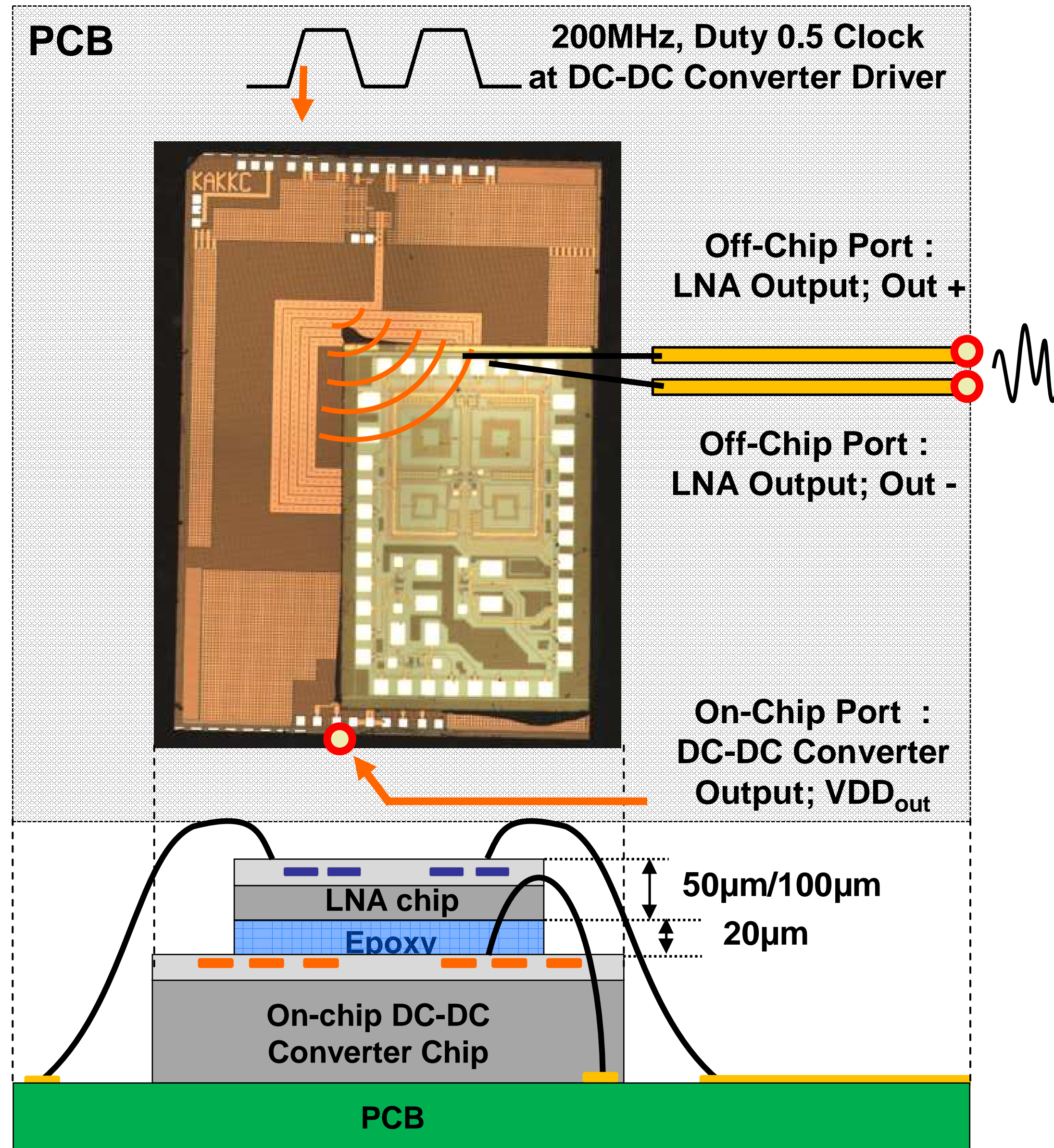
Solutions to Reduce Vertical Coupling in Mixed-Signal 3D-IC



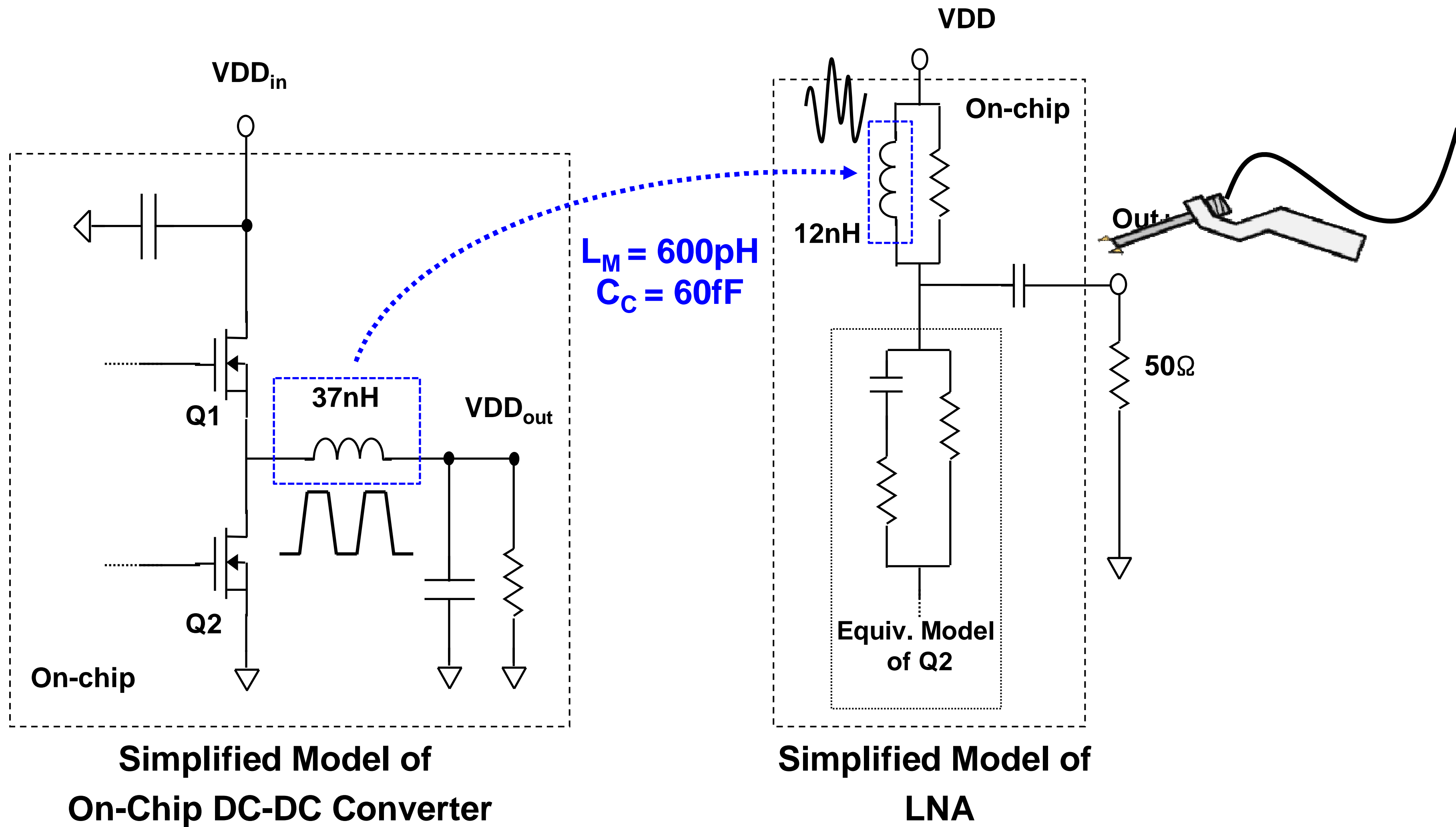
- Mesh shield using back-side re-distribution layer (RDL)
- Magnetic material shielding

- Dedicated chip for on-chip decoupling cap
- or re-distribution layer

Vertical Coupling from On-Chip DC-DC Converter to LNA



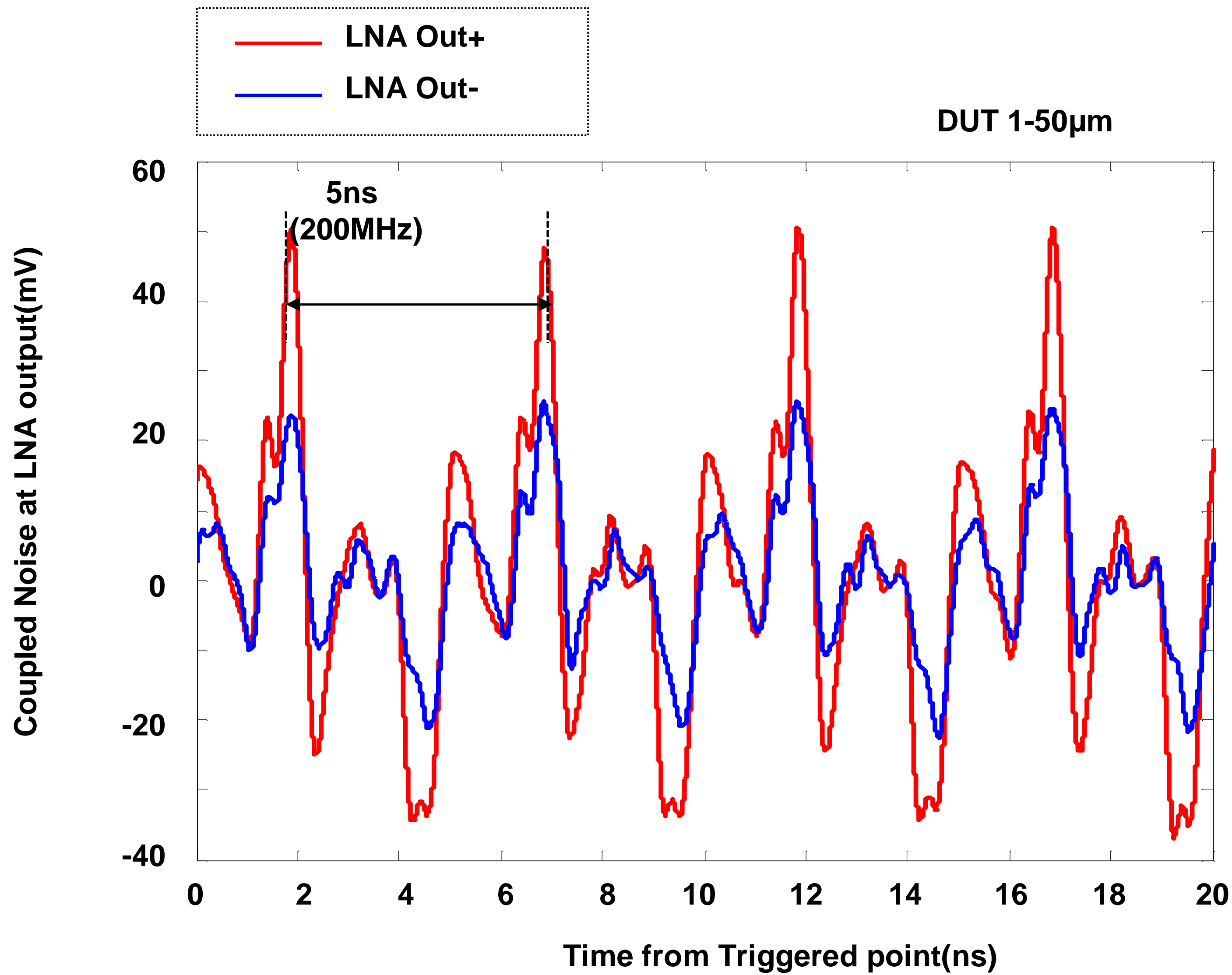
Inductive and Capacitive Coupling Model



Simplified Model of On-Chip DC-DC Converter

Simplified Model of LNA

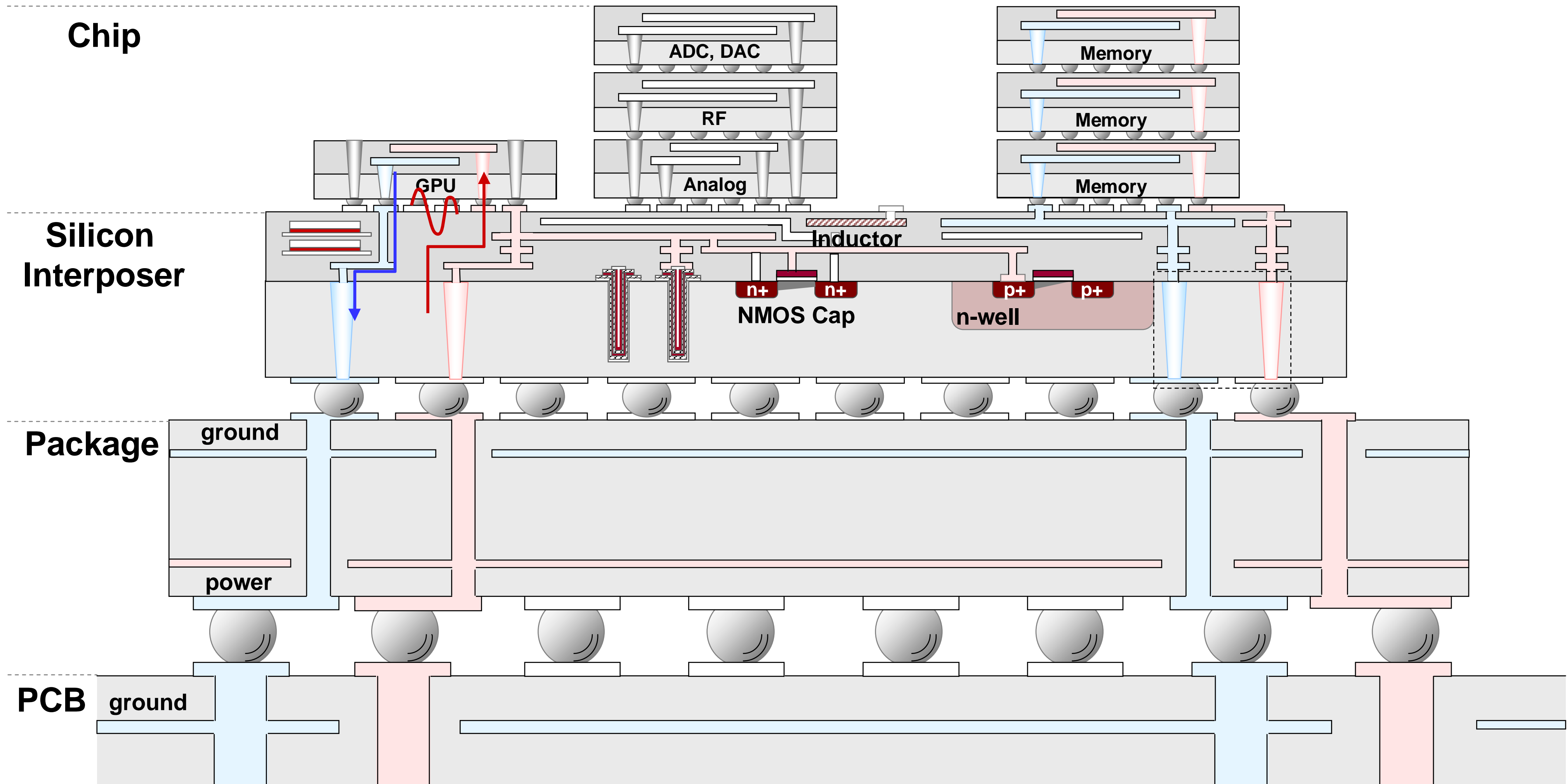
Measurement of Vertical Coupling



SSN Sensitive Circuits in IC

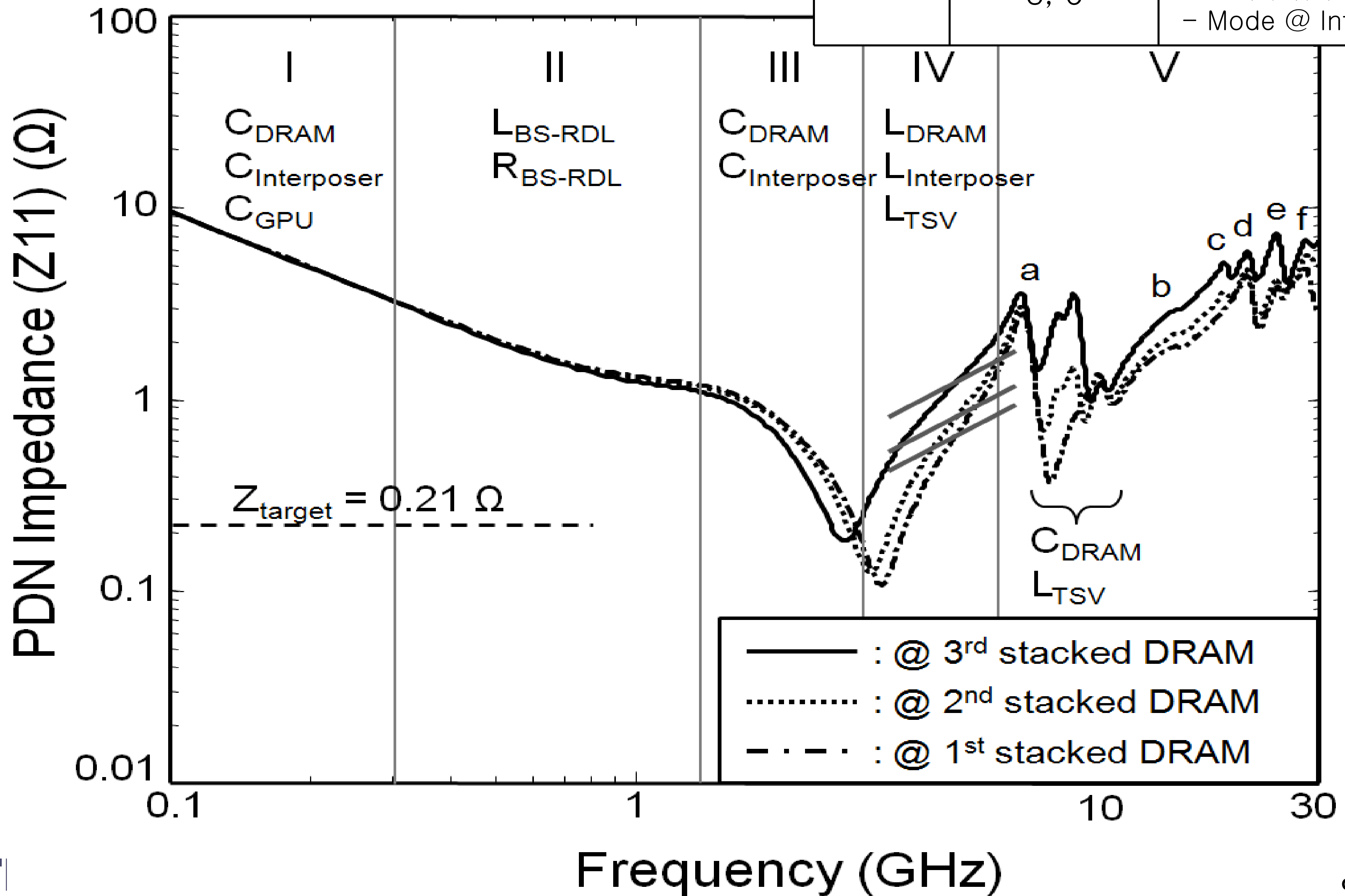
- VCO: Voltage Controlled Oscillator
- PLL: Phase Locked Loop
- ADC: Analog to Digital Converter
- DAC: Digital to Analog Converter
- LNA: Low Noise Amplifier
- RF Mixers

Hierarchical PDN in 3D IC

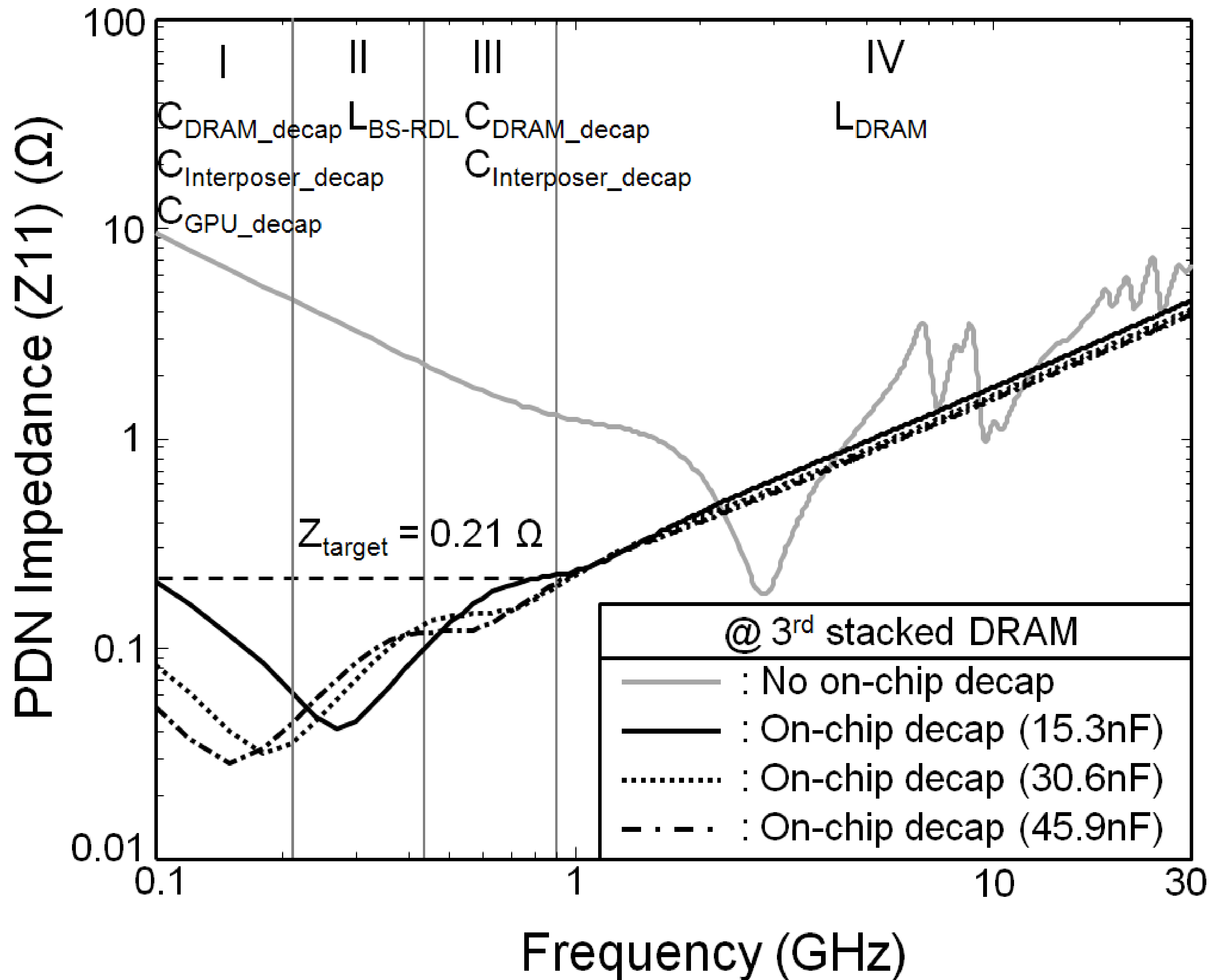


PDN Impedance Curves in 3D IC

Figure	*Peak (region V)*	*Mode number*
Fig. 3-(a)	a, b, d, f	(1,0), (2,0), (3,0), (4,0)/(0,1) - Mode @ DRAM
	c, e	(2,1), (3,1) - Mode @ Interposer



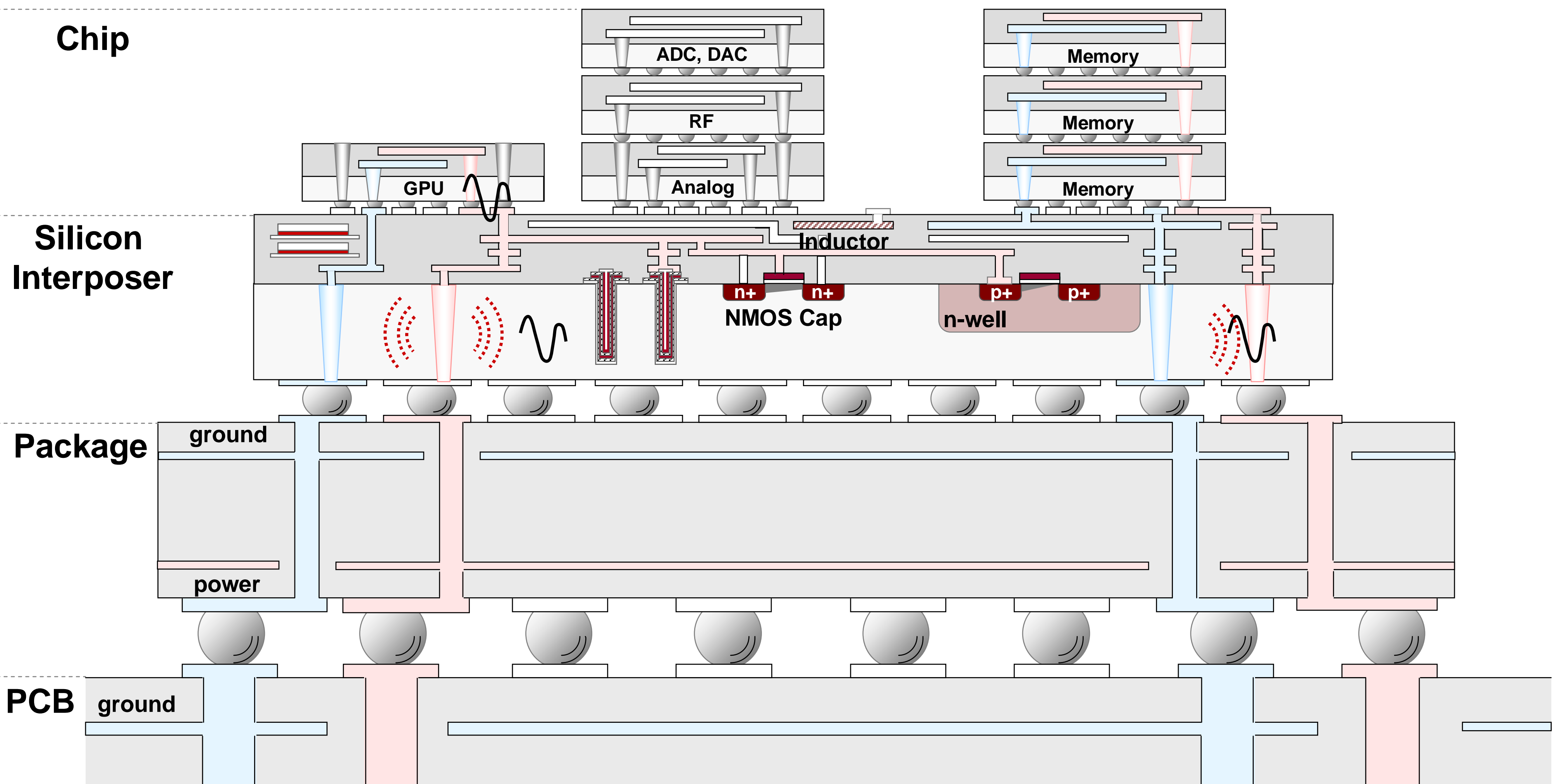
PDN Impedance of 3D IC with On-chip Decoupling Capacitors



Lowering PDN impedance in TSV based 3D IC

- On-chip and Off-chip decoupling capacitors
- Lower inductance TSV,
- Higher number of TSV
- Lower inductance of PDN interconnections in RDL, on-chip, and interposer
- Lower resistance of PDN interconnections in RDL, on-chip, and interposer

PDN Noise coupling pathes in3D IC

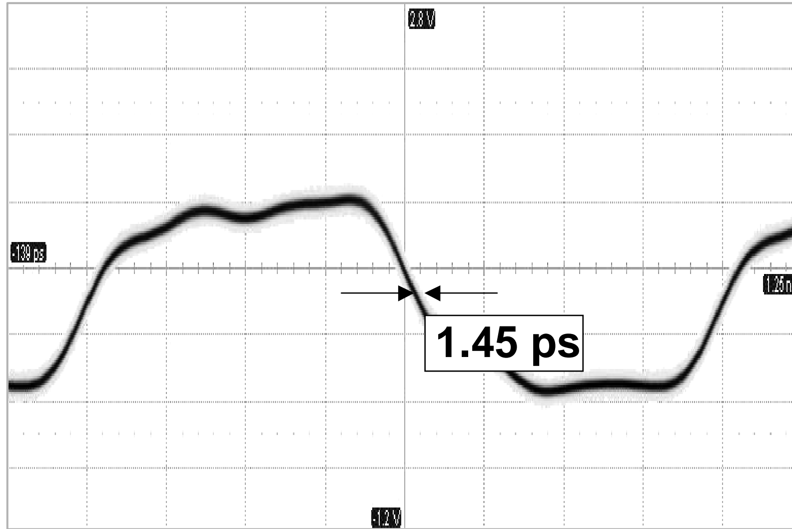


SSN Noise Coupling Paths

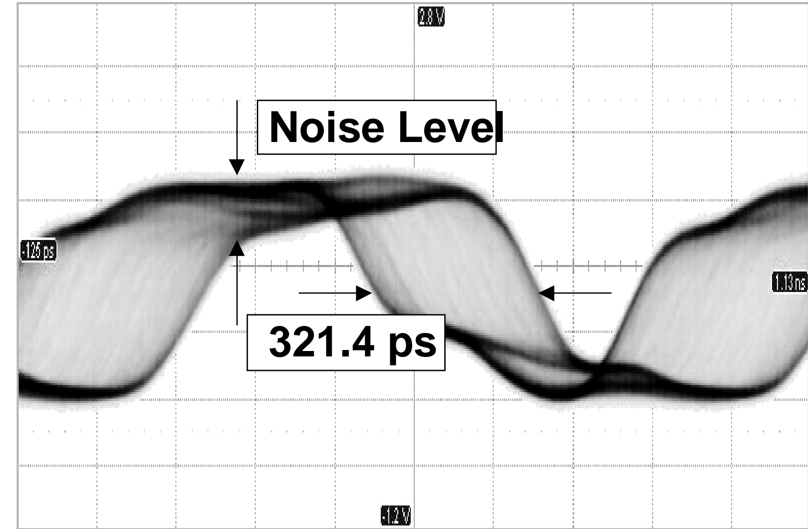
- On-chip and Off-chip PDN
- Si substrate
- Interposer substrate
- RDL patterns
- TSV
- Coupling

Clock Jitter Due to the SSN Coupling

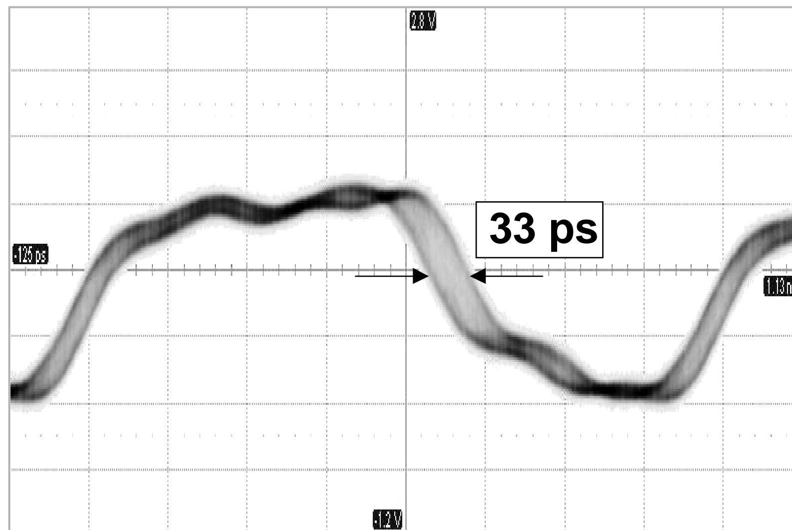
❖ w/o PDN Noise



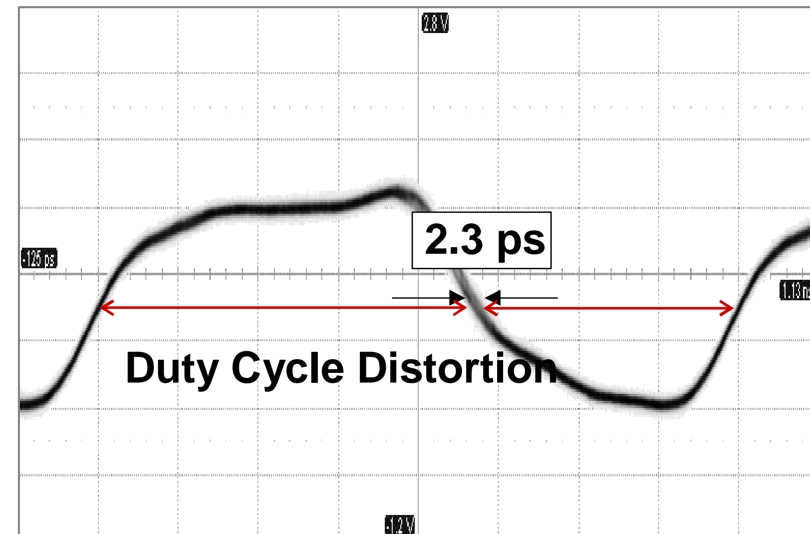
❖ 100MHz PDN Noise



❖ 800MHz PDN Noise



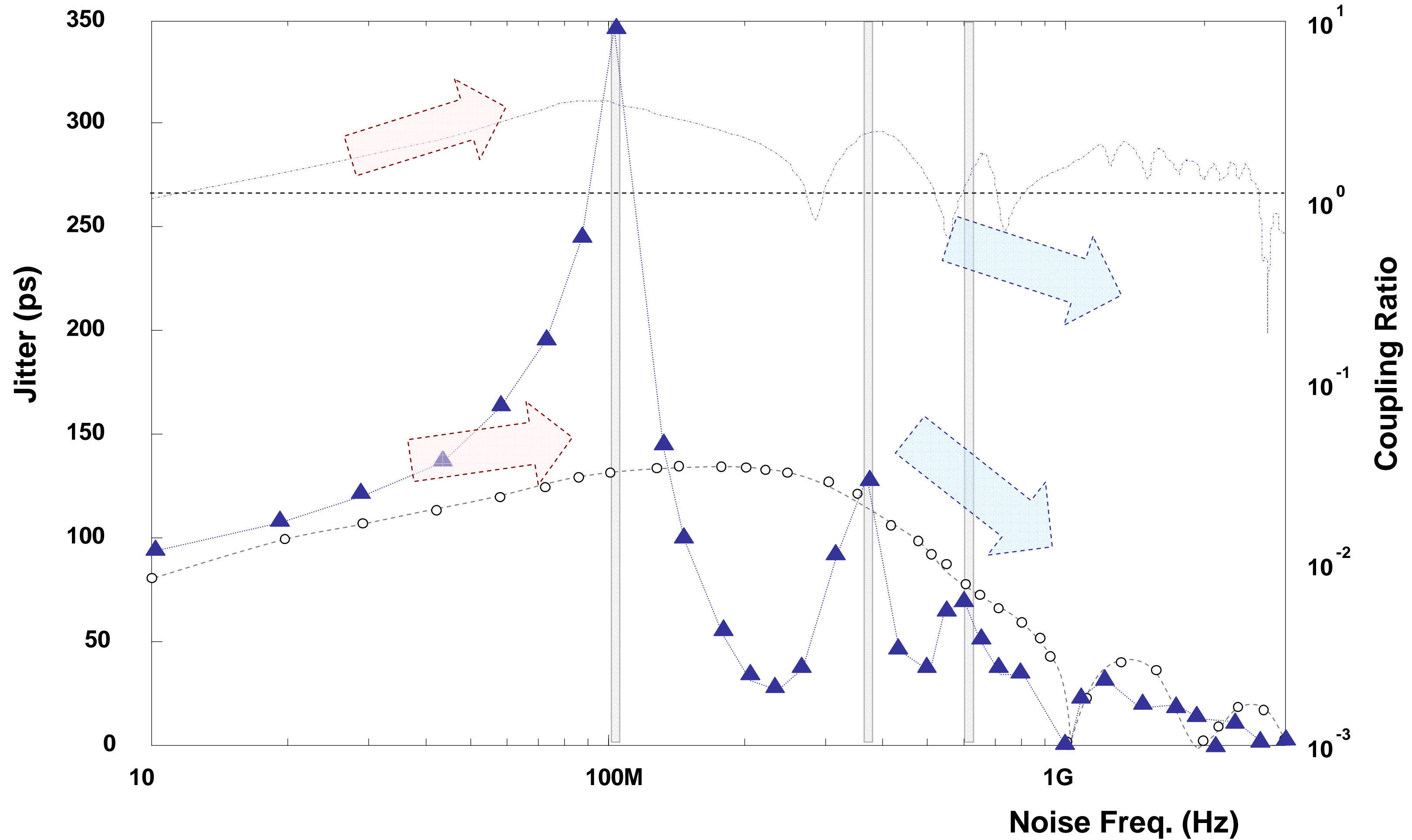
❖ 1GHz PDN Noise



Jitter w/o and w PDN Models

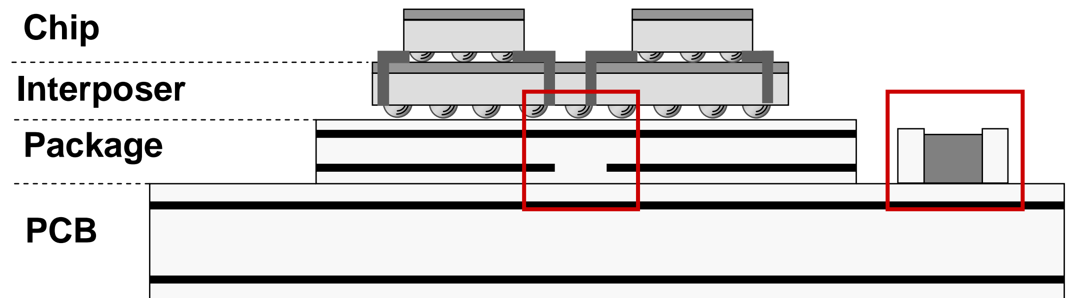
Noise level : 100 mV

Input Clock Frequency of DLL = 1 GHz

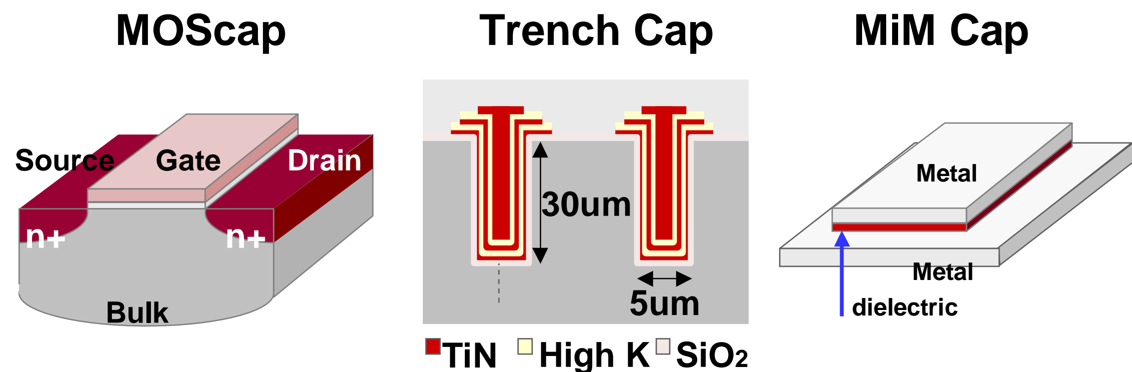


Noise Isolation Techniques Applicable to 3D ICs

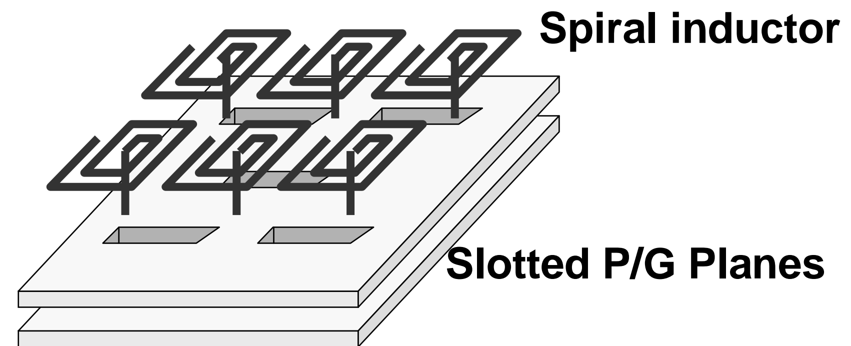
- At Low Frequency Region (< several hundred MHz)
  - Off-chip decap
  - Split P/G planes



- At Mid. Frequency Region (< several GHz)
  - On-chip decap
  - Embedded cap in interposer
  - Trench, MiM cap with a high K material

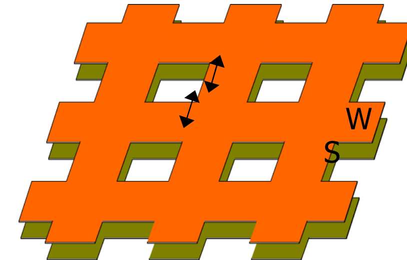


- At High Frequency Region (> tens GHz)
  - On-chip EBG in the interposer
  - Connected with TSVs
  - Design issues : High Q inductor and Low ESR



On-Interposer EBG Structure

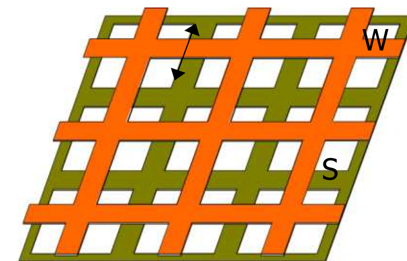
Capacitive P/G mesh



Width: 80um

Space: 120um

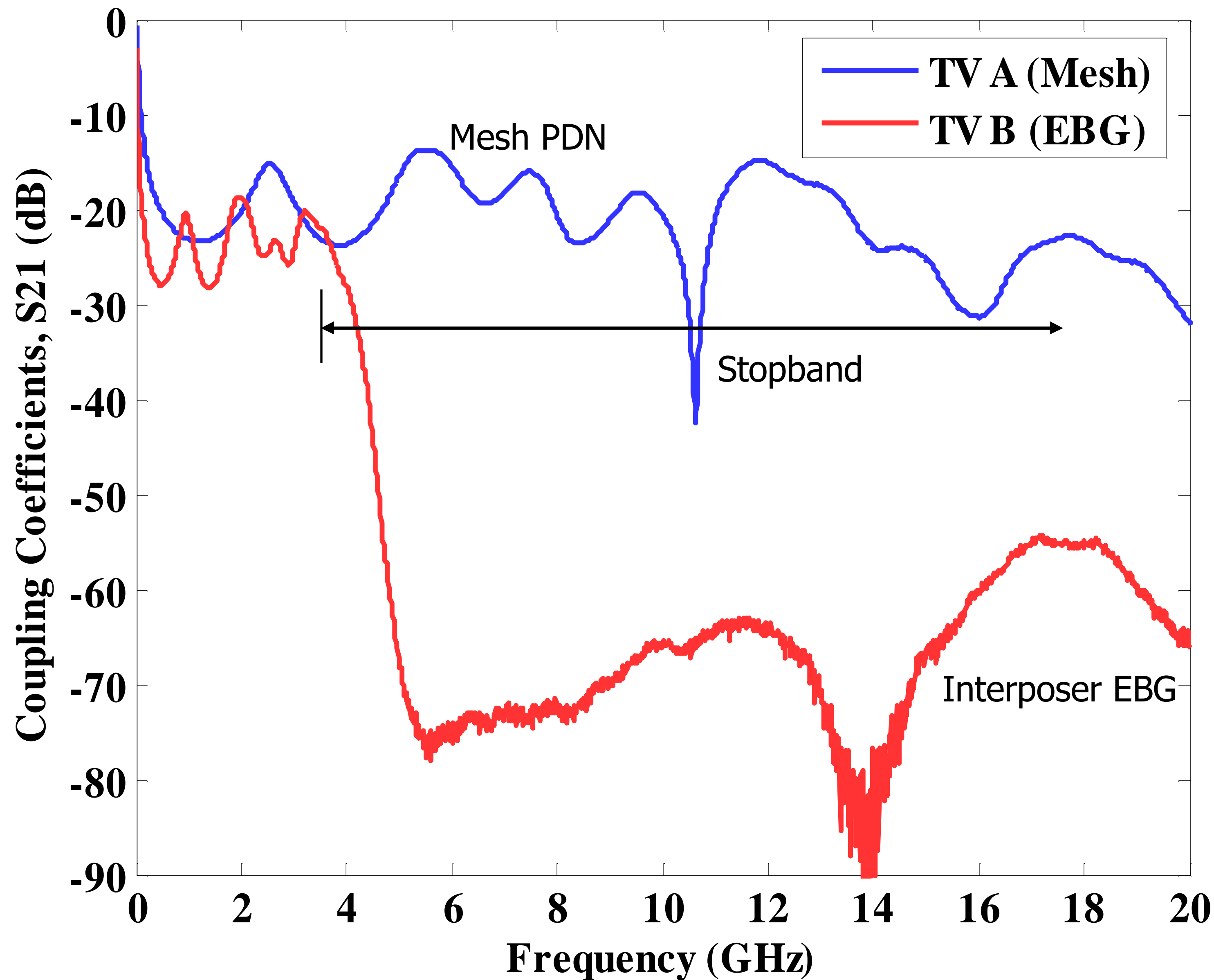
Inductive P/G mesh



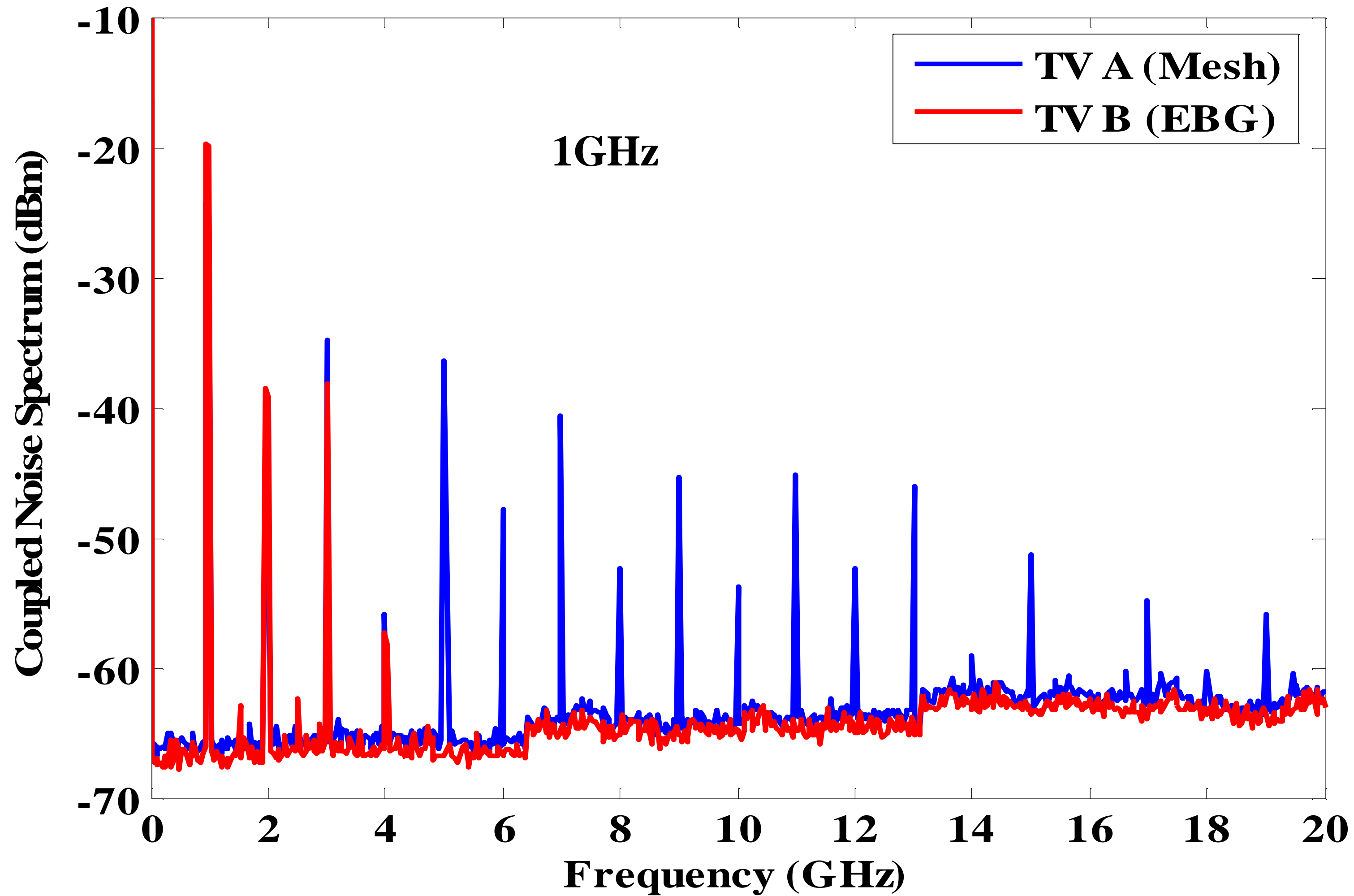
Width: 40um

Space: 360um

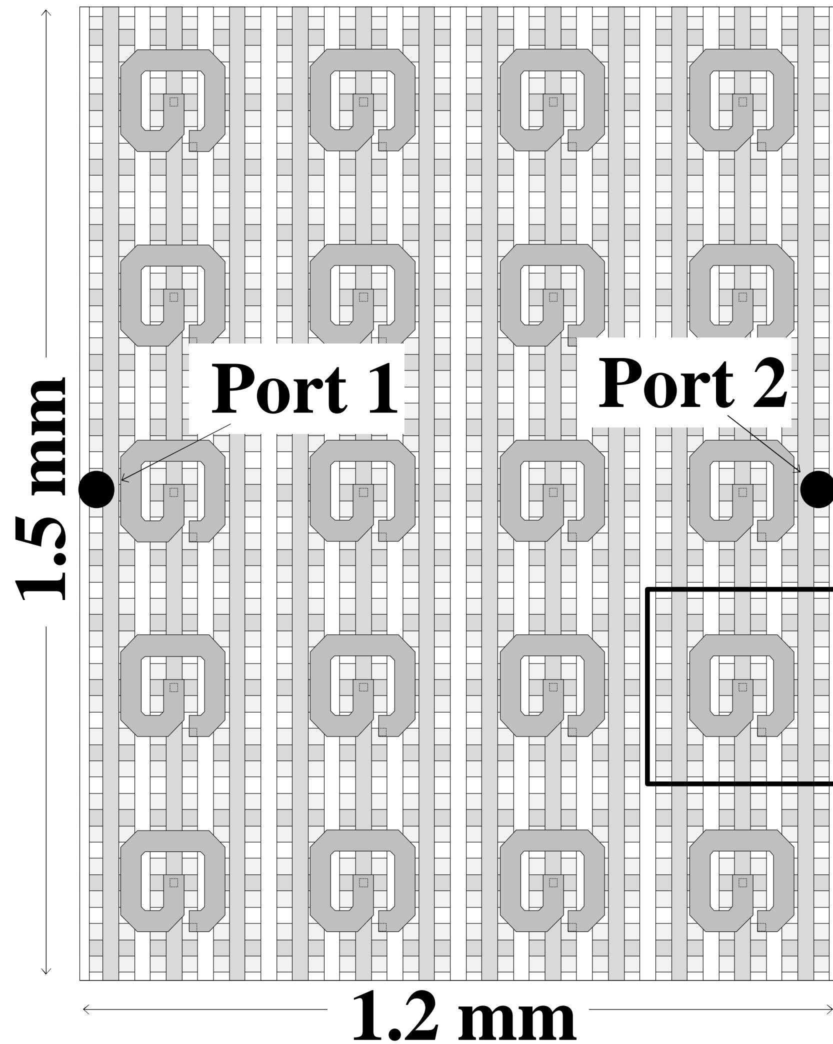
Measurement Results of On-interposer EBG

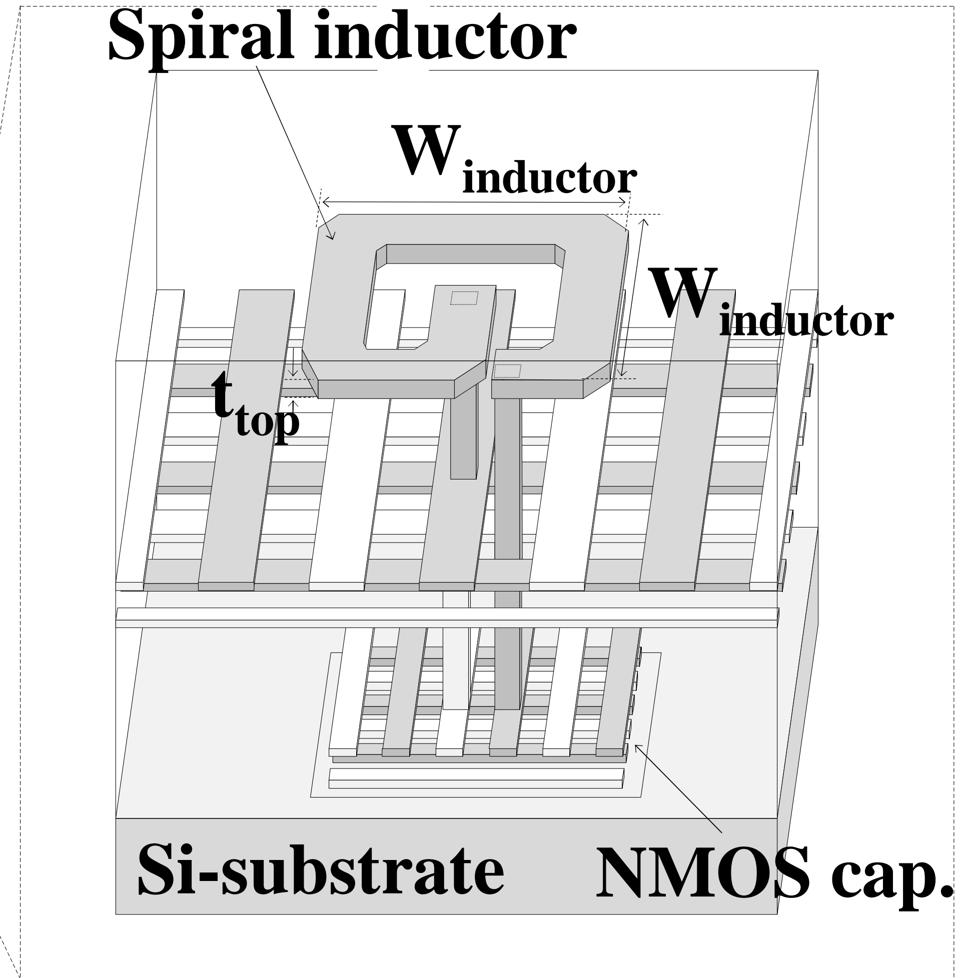


Measurement Results of On-interposer EBG

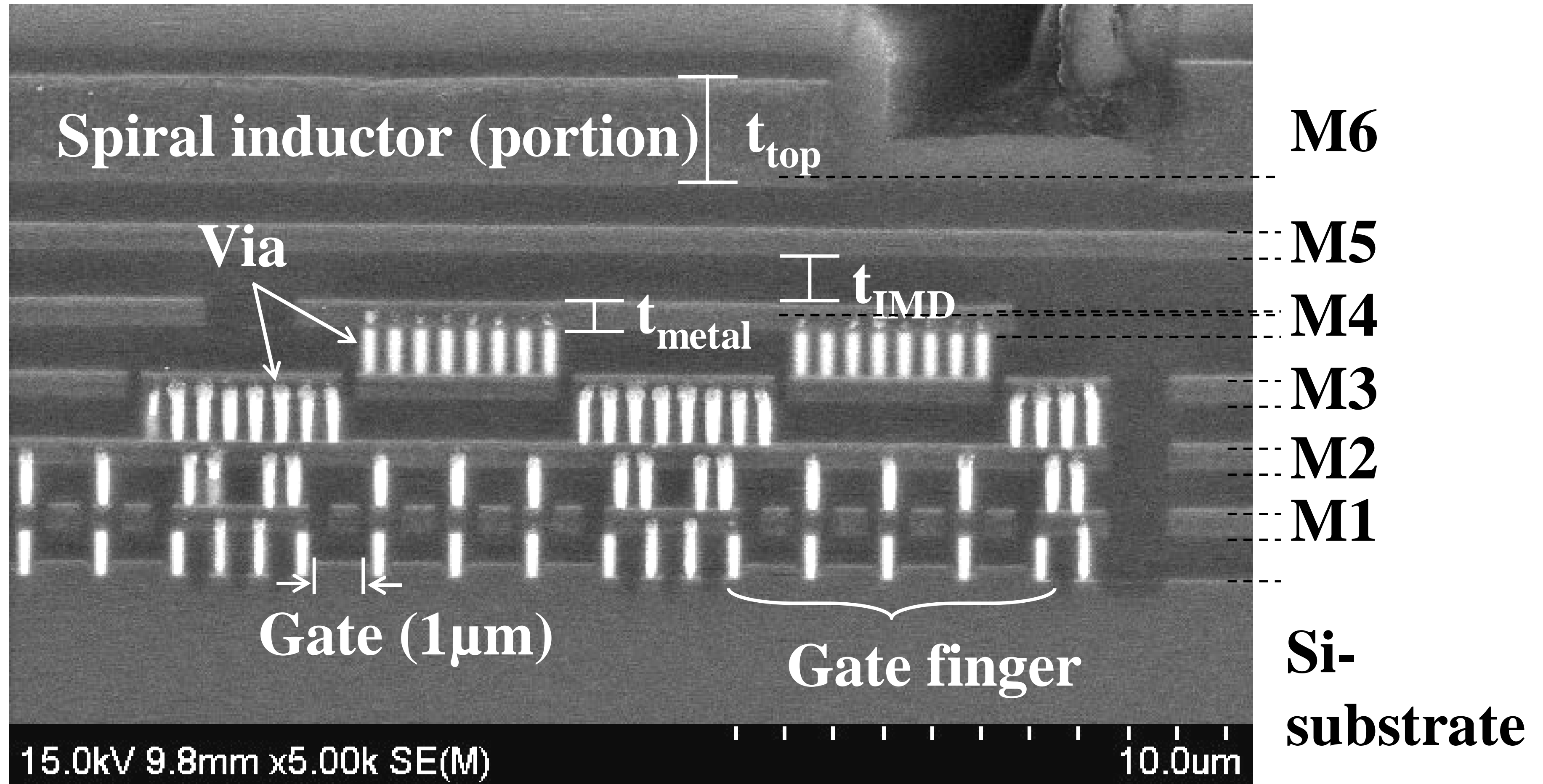


On-chip CMOS Active EBG



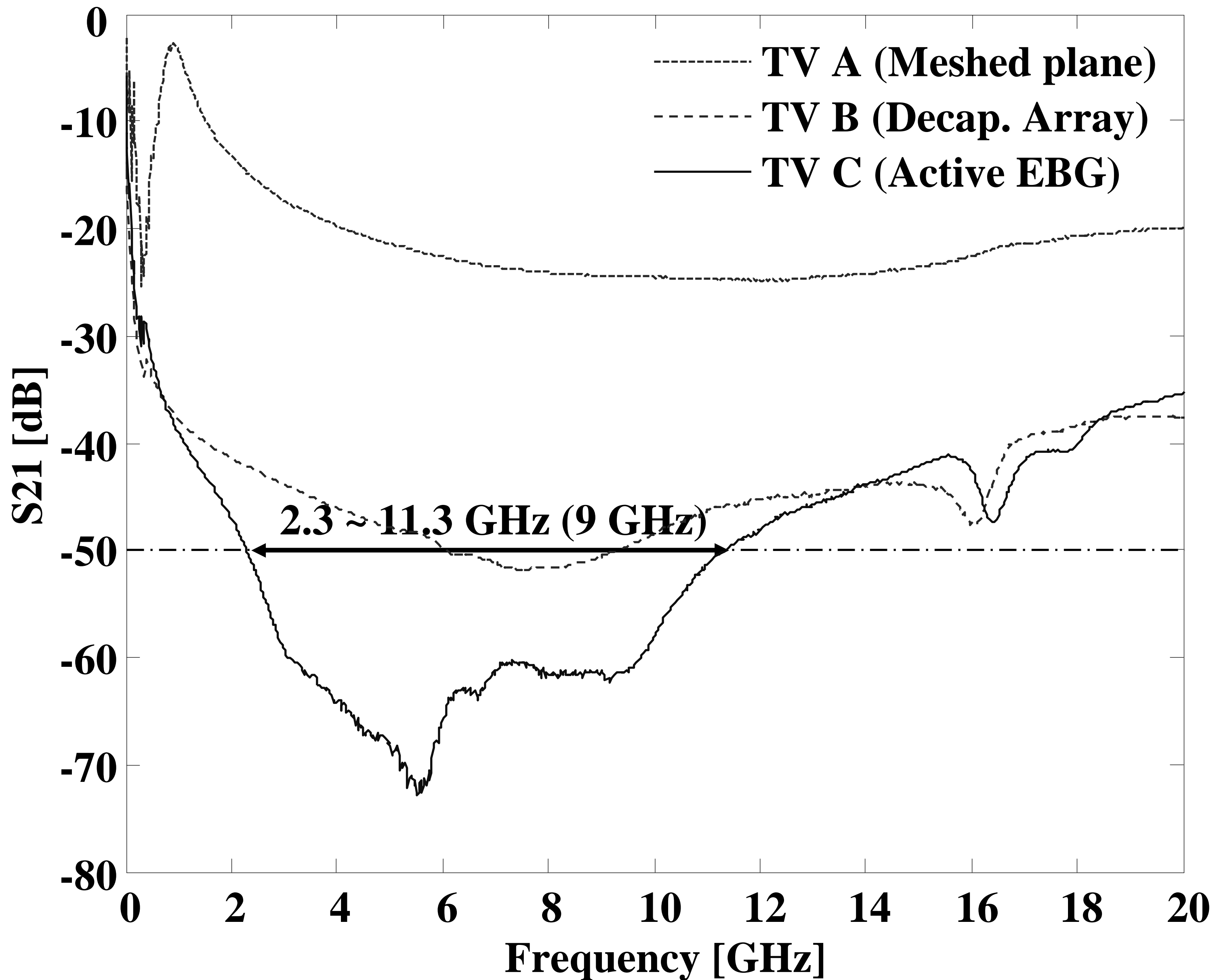


SEM Photograph of On-chip Active CMOS EBG

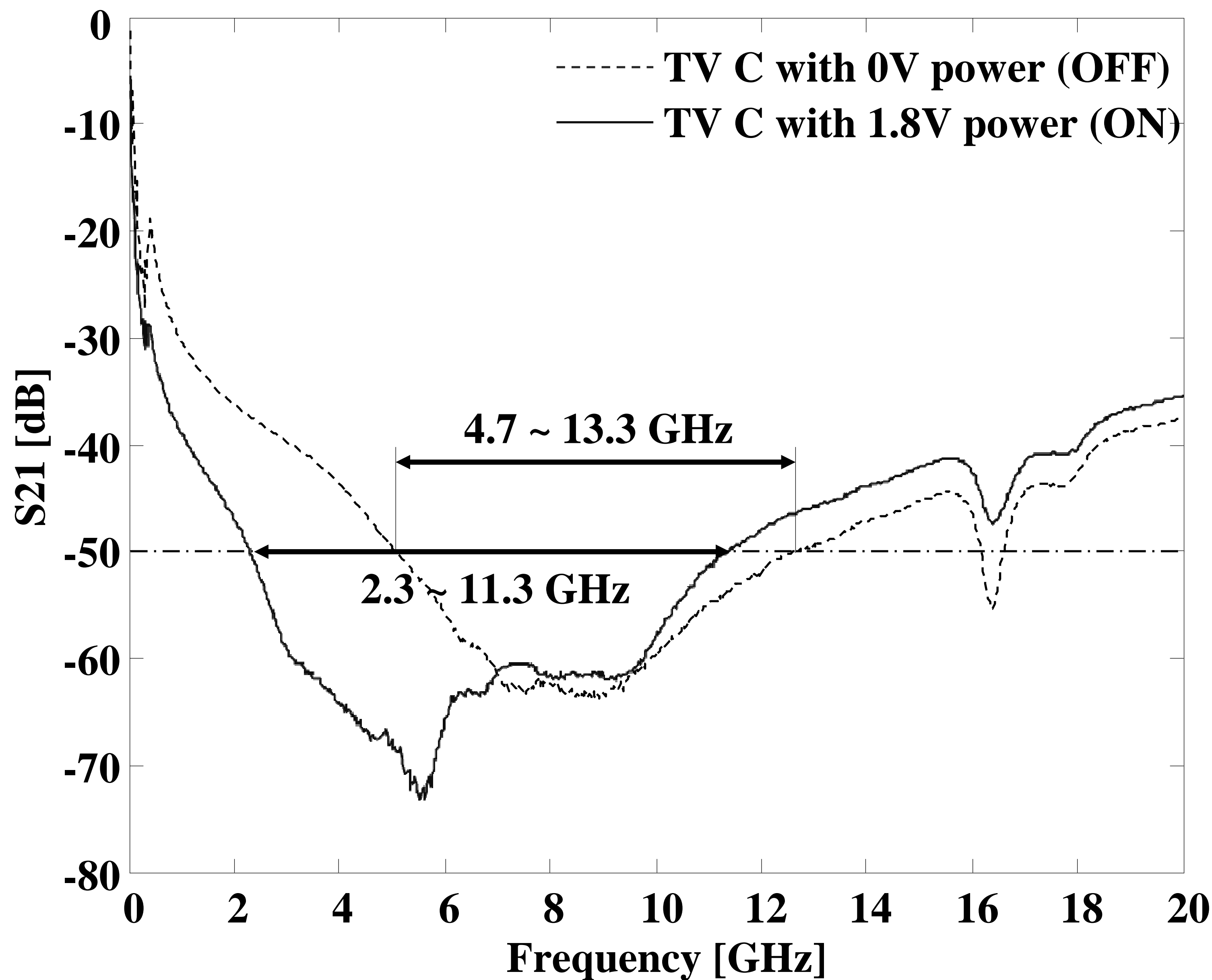


* MagnaChip 0.18μm standard CMOS Process

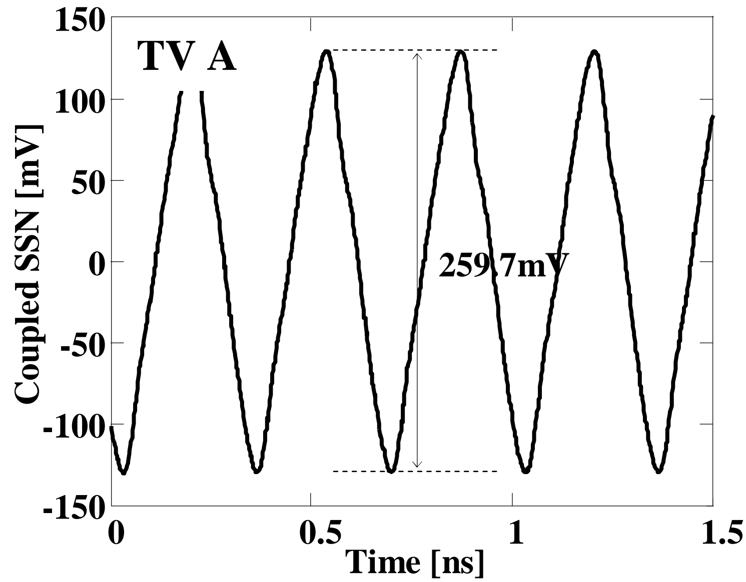
Measured S21 of On-chip Active CMOS EBG



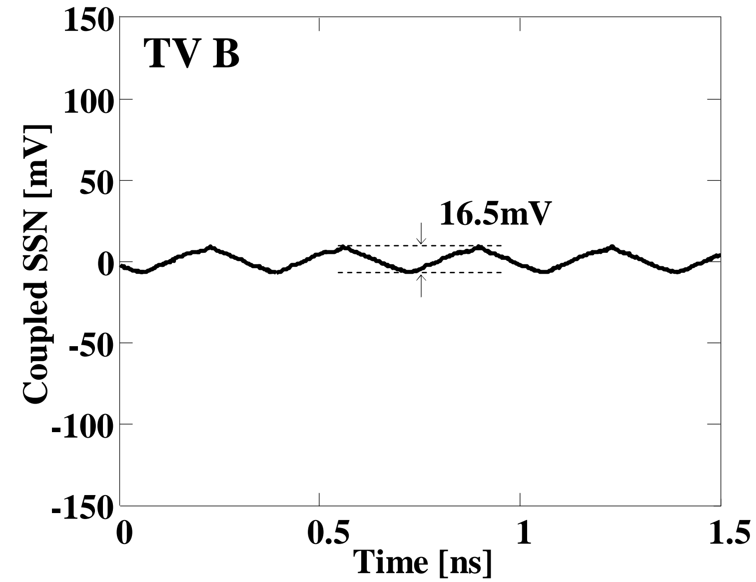
Tuning of On-chip Active CMOS EBG



Measured SSN Waveforms with a 3-GHz Clock Noise Input



(a)



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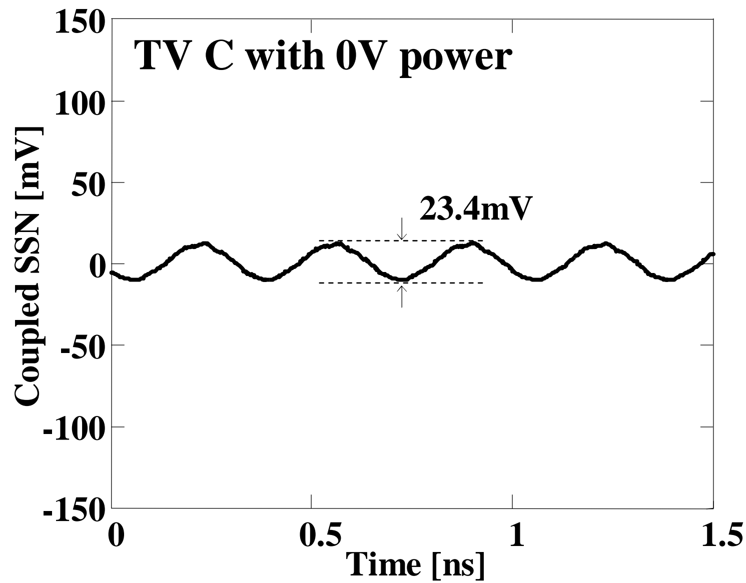
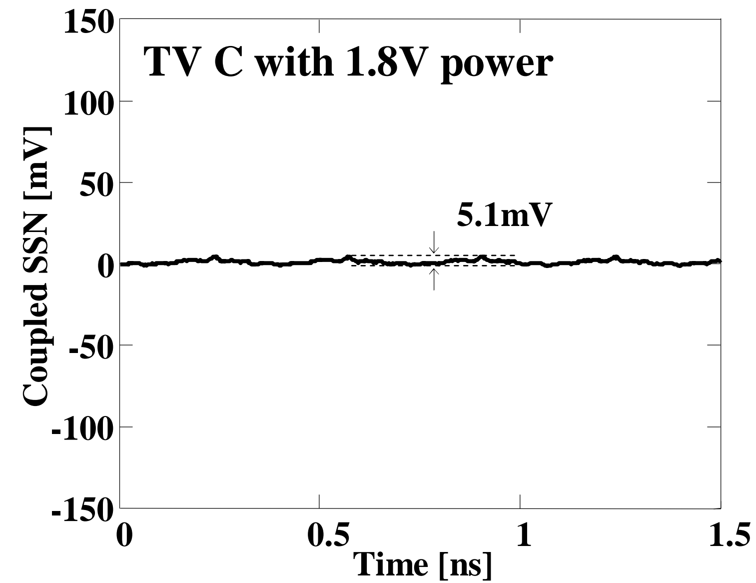


(c)



(d)

Summary

-TSV is the most critical interconnection structure in 3D IC.

- TSV can cause significant channel loss for high-speed signaling.

- Equalizer or specific I/O schemes are needed to support low power and high-speed data transmissions.

-Crosstalk and coupling between TSV and active circuit need to be considered when designing the TSV arrangement configurations.

-Vertical coupling should be considered in mixed mode 3D IC.

- Shielding structures are needed to reduce the TSV crosstalks and noise couplings.