



17th International Memory Workshop

May 18th – 21th 2025

Organizing Committee:

General Chair: Haitao Liu, *Micron*, USA

Publicity Chair: Antonio Arghini, *Imec*, Belgium

Technical Chair: Sangbum Kim, SNU, South Korea

Finance Chair: Prashant Majhi, *Intel*, USA

Scientific Committee:

Hao Meng, *CXMT*, China

Sumio Ikegawa, *Everspin*, USA

Fumie Kikushima, *Kioxia*, Japan

Teng-Hao(Elton) Yeh, *Macronix*, Taiwan

Yong Kyu Lee, *Samsung*, Korea

Seho Lee, *SK Hynix*, Korea

Henry Chin, *WDC*, USA

Zhiliang XIA, *YMTC*, China

Nanbo Gong, *IBM*, USA

Nhan Do, *Microchip*, USA

Michiel Van Duuren, *NXP*, Netherlands

Shibun Tsuda, *Renesas*, Japan

Jun Okuno, *SONY*, Japan

Mattia Boniardi, *ST Microelectronics*, Italy

Robert Glazewski, *Texas Instruments*, USA

Katherine Chiang, *TSMC*, Taiwan

Frederick Chen, *Winbond*, Taiwan

Xiao Gong, *National U of Singapore*, Singapore

Bin Gao, *Tsinghua Univ.*, China

Laurent Grenouillet, *CEA-Leti*, France

Stephan Menzel, *Forschungszentrum*, Germany

Xaixin Xu, *IME*, China

Ludovic Goux, *Imec*, Belgium

Arun Karamcheti, *Applied Materials*, USA

Takumi Mikawa, *Screen*, Japan

Motoyuki Sato, *Tel*, Japan

Advisory Committee:

Srivardhan Gowda, *Micron*, USA

Dirk Wouters, *RWTH Aachen*, Germany

Thomas Mikolajick, *NamLab&TU*, Germany

Summary of Events

Sunday, May 18th

Tutorial #1 – HBM

8:30AM – 11:30AM

Lunch (Provided)

11:30AM – 1:15PM

Tutorial #2 – Emerging Memory

1:15 PM – 4:15PM

Monday, May 19th

Opening remarks

8:30AM – 8:50AM

Session #1 – Keynotes

8:50AM – 10:20AM

Session #2 – DRAM

10:50AM – 12:05PM

Lunch (Provided)/Committee Luncheon

12:05PM – 2:05PM

Session #3 – NAND I

2:05PM – 3:45PM

Poster Session + Reception

5:30PM – 8:30PM

Tuesday, May 20th

Session #4 – In-Memory Computing

8:30AM – 10:10AM

Session #5 – NAND II

10:40AM – 12:20PM

Lunch (Provided)

12:20PM – 2:15PM

Session #6 – Emerging Memory

2:15PM – 3:55PM

Panel Discussion

4:20PM – 5:30PM

Banquet

7:00PM – 9:00PM

Wednesday, May 21st

Session #7 – NAND III

8:30AM – 10:10AM

Session #8 – Ferro

10:40AM – 11:55AM

Closing Remarks – Best papers awards

11:55AM – 12:15PM

Sunday, May 18th

Tutorial #1 8:30AM – 11:30AM Advanced DRAMs and HBM

Chair: Motoyuki Sato, *Tel*

Katherine Chiang, *TSMC*

08:30AM **Gaurav Thareja**, *Applied Materials*, "Materials, Processes and Systems Co-optimization for advanced HBMs"

09:20AM **Han Suk Ko**, *SK Hynix*, "HBM & Memory Opportunity/Challenge for AI"

10:10AM—10:40AM **Coffee Break**

10:40AM **Gummadi Ram**, *NVIDIA*, "(Tentative) HBM system"

11:30AM—1:15PM **Lunch (Provided)**

Tutorial #2: 1:15PM – 4:15PM Emerging Memory

Chair: Ludovic Goux, *Imec*

Stephan Menzel, *Forschungszentrum*

1:15PM **Kai Ni**, *University of Notre Dame*, "Rethinking Vertical NAND: How Ferroelectrics Can Potentially Change the Game"

2:05PM **Mattia Boniardi**, *ST*, "Embedded Phase Change Memory: From Device Physics to AI-oriented Applications"

2:55PM—3:25PM **Coffee Break**

3:25PM **Enrico Piccinini**, *Applied Materials*, "Simulation-driven material engineering for memory devices"

Monday, May 19th

Poster Session

6:00PM – 8:30PM

[P1] Teng-Hao Yeh, *Macronix International (MXIC)*, "Utilizing 2T SONOS Cell Characteristics for L2/Euclidean Distance Computing – From Unit Cell to Array Operations"

[P2] Anurag Swarnkar, *Imec*, "Design Technology Co-Optimization of 3D SRAM Macro in Nanosheet Technology for High-Bandwidth Applications"

[P3S] Elisa Vianello, *Univ. Grenoble Alpes*, "Dual-Mode 16kb Memory: Transforming a Ferroelectric Capacitor Bitcell into Resistive Filamentary Memory"

[P4] Po-Hao Tseng, *Macronix International*, "Monolithic 3D Macro Integrating CMOS with Ambipolar SONOS Tunnel FET for High Performance Edge-AI Computing Applications"

[P5] David Lehninger, *Fraunhofer IPMS*, "Al-Doped HZO: A BEOL compatible Ferroelectric Material for Automotive-Grade Memory"

[P6] Wooseok Choi, *IBM*, "Hardware Implementation of Ring Oscillator Networks Coupled by BEOL Integrated ReRAM for Associative Memory Tasks"

[P7] Enrico Piccinini, *Applied Materials*, "Simulation of Ge-rich PCM Device Material Evolution from Post-Deposition Anneal to Programming Operations"

[P8S] Junnosuke Furukawa, *University of Tokyo*, "Bayesian Neural Network Realization by Random Telegraph Noise in 40nm TaOX ReRAM CiM"

[P9S] Marcelo Correa Cueto, *Weebit Nano Ltd*, "Relaxation-Aware Programming in RRAM: Evaluating and Optimizing Write Termination"

[P10S] Mufeng Chen, *Purdue University*, "Analog Multilevel eDRAM-RRAM CIM for Zeroth-Order Fine-tuning of LLMs"

[P11S] Pufan Xu, *Tsinghua University*, "A Precision-Adaptive ECC Strategy with Computing Fusion Decoding for Near/In-Memory Computing"

[P12] Koji Sakui, *Unisant*, "Dynamic Flash Memory Operation Experimentally Validated with 65nm SOI Technology"

[P13S] Jihad Nacereddine Bouakaz, *KU Leuven*, "1kb IGZO TFT based Static Random Access Memory for IoT applications"

[P14] John Hoang, *Lam Research Corporation*, "Enabling Merged 3D NAND Memory Hole and Interlayer Dielectric (ILD) Contact Etches with Deposition and Etch Co-Optimization (DECO)"

[P15] Joshua Collins, *Lam Research Corporation*, "Deposition of ALD-Molybdenum for Flash Memory Wordline Metallization"

Monday May 19th

08:30AM Haitao Liu, **Opening Remarks**

Session #1 8:50AM – 10:20AM **Keynotes**

Chairs: Haitao Liu, *Micron*
Sangbum Kim, *Seoul National Univ.*

- 8:50AM [1.1] Krishnan Subramanian, *Micron*, NAND flash innovation in the AI Era" --**Invited**
- 9:20AM [1.2] Su Jin Ahn, *Samsung*, "Future Technology Outlook on DRAM/Flash Memories for More Moore and More Than Moore" --**Invited**
- 9:50AM [1.3] Dmitri Strukov, *UCSB*, "Controlling ReRAM's Switching Characteristics with Shadow Memory for Continual Learning" --**Invited**
- 10:20AM **Break**

Session #2 10:50AM – 12:05PM **DRAM**

- Chairs:** Motoyuki Sato, *Tel*
Frederick Chen, *Winbond*
- 10:50AM [2.1] Daisuke Matsubayashi, *imec*, Accurate off-current evaluation by parasitic capacitance extraction in capacitor-less DRAM cells"
- 11:15AM [2.2S] Po-Kai Hsu, *Georgia Institute of Technology*, "Monolithic 3D Stackable DRAM Design with BEOL-Compatible Oxide Channel Access Transistor"
- 11:40AM [2.3] Onur Mutlu, *ETH Zurich*, "Memory-Centric Computing: Solving Computing's Memory Problem" --**Invited**
- 12:05PM **Lunch (Provided) / Committee Luncheon**

Session #3 2:05PM – 3:45PM **NAND I**

- Chairs:** Fumie Kikushima, *Kioxia*
Henry Chin, *Sandisk*
- 2:05PM [3.1] Hiroshi Maejima, *Kioxia Corporation*, "Crossed Bit Line Architecture (CBL) in 3D Flash memory CMOS Directly Bonded to Array (CBA) Structure"
- 2:30PM [3.2] Chanyang Park, *Samsung Electronics*, "First Demonstration of Threshold Voltage Modeling in Multi-Hole V-NAND Flash Architecture with Noncircular Channel Hole Profiles"
- 2:55PM [3.3] Sana Rachidi, *Imec*, "Hole-Side Airgap Integration as Enabler for 3D NAND Flash Z-Pitch Scaling"
- 3:20PM [3.4] Masaaki Higuchi, *Micron*, "Modeling of the impact of elliptical shapes on main Read Window Budget mechanisms in 3D NAND"

Reception 5:30PM – 8:30PM

Sponsored by Applied Materials

Poster Session 6:00PM – 8:30PM

Chair: Arun Karamcheti, *Applied Materials*
Nanbo Gong, *IBM*

Tuesday May 20th

Session #4 8:30AM – 10:10AM **In-Memory Computing**

- Chairs:** Mattia Boniardi, *ST Microelectronics*
Takumi Mikawa, *Screen*
- 8:30AM [4.1] Steven Lemke, *SST*, "Reliability and Accuracy of a Qualified Split-Gate Flash In-Memory Compute Technology" --**Invited**
- 8:55AM [4.2S] Hechen Ji, *Beijing University of Posts and Telecommunications*, "High-parallel In-memory Data Sorting based on 40nm Analog RRAM Chip"
- 9:20AM [4.3S] Eknath Sarkar, *Georgia Institute of Technology*, "Analog In-Memory-Compute with Multi-bit Silicon Ferro FinFET Array for Improved Energy and Area Efficiency"
- 9:45AM [4.4] Sidney Tsai, *IBM*, "Analog AI Accelerators for Transformer-based Language Models: Hardware, Workload, and Power Performance" --**Invited**
- 10:10AM **Break**

Session #5 10:40AM – 12:20PM **NAND II**

- Chairs:** Antonio Arreghini, *Imec*
Fumie Kikushima, *Kioxia*
- 10:40AM [5.1] Kana Kudo, *Kioxia*, "Energy-Efficient In-Memory Computing using 3D Flash Memory with Sequential Multi-Block Activation and Current Control Cell (CC cell)"
- 11:05AM [5.2] Junyoung Lee, *Samsung Electronics*, "Development of Innovative Self-Aligned SSL Mold (SASM) Scheme with Remarkable Reduction of Chip Size"
- 11:30AM [5.3] Teng-Hao Yeh, *Macronix International (MXIC)*, "A Novel 3D Stacked Vertical-Channel High-Voltage Peripheral Transistor for Largely Scaled the WL Driver Circuit of 1000-layer 3D NAND Flash"
- 11:55AM [5.4] Albert Chen, *Sandisk Technologies, Inc.*, "On the Challenges of Open-Block Reads in 3D NAND"
- 12:20PM **Lunch (Provided)**

Session #6 2:15PM – 3:55PM **Emerging Memory**

- Chairs:** Michiel Van Duuren, *NXP*
Stephan Menzel, *Forschungszentrum Jülich*
- 2:15PM [6.1] John Sung, *MXIC*, "Enhancing 3D XPT/SOM Reliability: Strategies for Mitigating Spike Current and Improving Read Endurance" --**Invited**
- 2:40PM [6.2S] Song-hyeon Kuk, *KAIST*, "Proposal of Block Erase and Verify Schemes for Ferroelectric NAND: Overcoming Critical Challenges from Threshold Voltage Polarity"
- 3:05PM [6.3] Thi Van Anh Nguyen, *Tohoku Univ.*, "Low write power and Field-free sub-ns write speed SOT-MRAM cell with Design Technology of Canted SOT structure and Magnetic Anisotropy for NVM"
- 3:30PM [6.4] Syed M. Alam, *Everspin*, "STT-MRAM Antifuse Macro for Memory, SoC, and FPGA Chips" --**Invited**
- 3:55PM **Break**

Panel Discussion 4:20PM – 5:50PM

- Topic:** "Memories for AI (tentative)"
- Moderator:** Jian Chen, *Micron*
- Panellists:** Dr. Insoo Yoon, *SanDisk Corp*
Dr. Seho Lee, *SK Hynix*
Dr. Sidney Tsai, *IBM*
TBD, *Nvidia Corp*

Banquet 7:00PM – 9:00PM

Wednesday May 21st

Session #7 8:30AM – 10:10AM **NAND III**

- Chairs:** Yong Kyu Lee, *Samsung*
Prashant Majhi, *Intel*
- 8:30AM [7.1] Tae-Gon Lee, *Samsung Electronics Co.*, "On-Chip Capacitors with Wall-Type Structure in 9th Generation 3D VNAND Flash Memory"
- 8:55AM [7.2] Abhijith Prakash, *Sandisk Technologies, Inc.*, "Innovative V-NAND Flash Structure with Dual Trap Layer for Future Generations of Multi-Bit Device"
- 9:20AM [7.3] Jeongyoon Yeo, *Samsung Electronics*, "Innovative V-NAND Flash Structure with Dual Trap Layer for Future Generations of Multi-Bit Device"
- 9:45AM [7.4] Hao-Ling Tang, *Applied Materials*, "Demonstration of Conformal MoS₂ on High-Aspect-Ratio Structures up to 40:1 and Exploration of Manufacturability in a 300mm Fab for 3D NAND applications"
- 10:10AM **Break**

Session #8 10:40AM – 12:15PM **Ferro**

- Chair:** Prashant Majhi, *Intel*
Jun Okuno, *SONY*
- 10:40AM [8.1S] Mor Dahan, *Technion*, "Novel Ultrafast Non-Destructive Readout of FeRAM by Low-Voltage Transient Current"
- 11:05AM [8.2S] Lance Fernandes, *Georgia Tech*, "Comparative Study of Channel Materials for Ferroelectric NAND Applications"
- 11:30AM [8.3] Asif Khan, *Georgia Tech*, "Ferroelectrics for Vertical NAND Flash Applications" --**Invited**
- 11:55AM Haitao Liu, **Closing Remarks**
- 12:05PM Sangbum Kim, **Best Paper Award Announcement**

Premium Sponsor



Platinum Sponsor



Gold Sponsors



Silver Sponsors

