18th International Memory Workshop

May 10th – 13th 2026

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Jeffrey McNeil, *Micron,* USA
George Matamis, *Lamresearch,* USA

Advisory Committee:

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Thomas Mikolajick, *Namlab&TU,* Germany
Dirk Wouters, *RWTH Aachen*, Germany

Summary of Events

Sunday, May 10th

Tutorial #1 – Memory Enabled Systems	8:30AM – 11:30AM
Lunch (Provided)	11:30AM – 1:15PM
Tutorial #2 – Advanced Memories	1:15 PM – 4:15PM

Monday, May 11rh

Opening remarks	8:30AM – 8:45AM
Session #1 –Keynotes	8:45AM – 10:15AM
Session #2 – NAND 1	10:45AM – 12:25PM
Lunch (Provided)/Committee Luncheon	12:25PM – 2:30PM
Session #3 – DRAM I	2:10PM – 4:20PM
Poster Session + Reception	**4**:30PM – 8:00PM

Tuesday, May 12th

Session #4 – Adv/Emerging Memories I	8:30AM – 10:10AM
Session #5 – DRAM II	10:40AM – 12:20AM
Lunch (Provided)	12:20PM – 1:45PM
Session #6 – Memory Enabled Systems	1:45PM – 3:50PM
Panel Discussion	4:15PM – 6:00PM
Banquet	7:00PM – 9:00PM

Wednesday, May 13th

Session #7 – NAND II	8:30AM – 10:10AM
Session #8 – Adv/Emerging Memories II	10:35AM – 12:15AM
Closing Remarks – Best papers awards	12:15AM – 12:30PM

Sunday, May 10th

Tutorial #1 8:30AM – 11:30AM Memory Enabled Systems

Chairs: **Ludovic Goux**, *IMEC*
Jeffrey McNeil, *Micron*

08:30AM **Dwaipayan Biswas,** *IMEC*, "Cross-technology co-optimization for Memory density and bandwidth"
09:20AM **In-Soo Yoon,** *Sandisk*, "3DNAND Innovations: High Bandwidth Flash for AI Era"
10:10AM—10:40AM *Coffee Break*
10:40AM **Mudit Bhargawa**, *Intel*, "STCO for Compute Systems: What, Why, How"
11:30AM—1:15PM *Lunch (Provided)*

Tutorial #2: 1:15PM – 4:15PM Advanced Memories

Chairs: **Frederick Chen,** *Winbond*
Stephen Menzel, *Forschungszentrum*

1:15PM **Jianshi Tang**, *Tsinghua Univ*, "Memristor-based CiM for Neural Network Acceleration"
2:05PM **Uwe Schroder**, *NaMLab*, "Doped HfO 2 based ferroelectric devices Challenges and Developments"
2:55PM—3:25PM *Coffee Break*
3:25PM **Shimeng Yu**, *Georgia Tech*, "Monolithically Stackable 1T1C 3D DRAM"

Monday, May 11th

Poster Session **4:30PM – 8:00PM**

[P1S] Kyungsoo Park, *Hanyang Univ (MXIC)*, "Demonstration of 3D-Extendible, Logic-Compatible Sub-1.8 V Asymmetric Double-Gate FeFETs with Sub-3.5 nm Ultrathin HZO for Analog CIM"

[P2] Leitao Liu, *Samsung, "*Comprehensive Analysis of Floating-Body Effect and Data Retention in the Next Generation DRAM Cell"

[P3S] Youngjun Park, *SeoulTech*, "Architectural Design of Low-latency and High-bandwidth 3D NAND with Split-Stacked Row Decoder for LLM Inference"

[P4] Tianyue Fu**,** *Peking University,* "Ultra-fast FE Switching of 260 ps with Record-high 2Pr of 64 μC/cm2 and Switching Current of 3.2 × 105 A/cm2 in La-doped HfO2 with Recoverable Fatigue"

[P5S] Pramoda Vishnumurthy, *NaMLab*, "Achieving a Dielectric Constant of 60 in ZrxHf1-xO2: A Candidate for DRAM?"

[P6] Ankit Agarwal, *NTU*, "HZO-based Ferroelectric FinFETs Exhibiting Low Power, Long Retention, and High Endurance (>109 cycles) performance at Cryogenic Temperatures"

[P7] Chulmin Choi, *Samsung*, "Experimental Decomposition of Threshold Voltage Distribution in 176-Layer TLC Vertical NAND Flash Memory"

[P8S] Haoran Wang, *Peking University*, "In-memory Log-transformation and Multi-exponentiation with Analog RRAM Arrays for Efficient Data Processing"

[P9S] Jiseok Hong, *IMEC*, "Quantitative Analysis of On-Current Discrepancy Between Monocrystalline Si and IGZO Channels in Stacked 3D-DRAM Transistors"

[P10] Wei Wang, *IME*, "Comprehensive Parasitic Analysis and Scalability Optimization of IGZO GAA Nanosheet 3D DRAM"

[P11] Ashish Pal, *AMAT*, "Materials to Systems Co-Optimization (MSCO) Modeling Platform for DRAM PPA Projections from Novel Material and Process Innovations Targeting Next Generation DRAM Technology Nodes"

[P12S] Jaewon Ham, *SNU*, "Overcoming Erase Limitations of Amorphous Oxide Semiconductor Channels through Dual Source/Drain Structures for Flash Memory"

[P13] Tobin Kaufman-Osborn, *AMAT*, "Leveraging Cutting-Edge Oxidation Techniques to Enable Next Generation Memory Devices"

[P14S] Xiangchao Ma, *Tsinghua University*, "A 28nm 16Mb Embedded RRAM IP with Hybrid Array Structure for OTA Update Application"

[P15S] Cong Sun, *Tsinghua University*, "PIRS: A Thermodynamic Relaxation Suppression Scheme on 40nm MLC RRAM Macro for Edge AI Inference"

[P16] T. Kobayashi, *Floadia Corporation*, "Enhancing SONOS-type Flash Memory for Nonvolatile Analog Computing-in-Memory via Precise Multi-level Weight Control and Improved Retention"

[P17] Muhammad Masuduzzaman, *Sandisk, "*Logical Scaling Beyond 4 bit/cell: Opportunities and Challenges"

[P18S] Nicolò Giovannelli, *CEA-Leti*, "Evaluation of Sidewalls Properties in HZO-based 3D Ferroelectric Capacitors"

[P19S] Alexandre Baigol, *ETH Zürich, "*20 ps Non-Destructive Read and 1 ns Write Operations at <5 V in Ferroelectric HfO2/ZrO2 Non-Volatile Memories"

[P20S] Seah Min, *SeoulTech*, "A Gate-All-Around Back-Gated Junctionless 3D NAND Structure for Improved Switching Efficiency and Variability Suppression"

[P21] Jiacen Guo, *Sandisk*, "An Ultra-fast 3P0V Multi-Level Cell Programming Algorithm for Inference Context Memory Storage (ICMS)"

[P22] Wei Cao, *Sandisk*, "Mitigating String Current Deficit in Future-Generation 3D NAND through a Co-Design Strategy for Verify Level and Bitline Voltage"

[P23] Debashish Basu, *IMEC*, "Systematic Failure Mode Analysis and Yield Enhancement of STT MRAM Arrays via Interconnect Patterning and Process Optimization"

Monday May 11th

08:30AM **Sangbum Kim**, Opening Remarks

Session #1 8:45AM – 10:15AM Keynotes
Chairs: **Sangbum Kim,** *SNU*
Prashant Majhi, *Intel.*

8:45AM **[1.1] Nirmal Ramaswamy**, *Micron Technology*, "Memory Technology: Enabling the AI Revolution" ***--Invited***
9:15AM **[1.2] Chris Kang,** *Samsung,* "NAND Flash Memory: Boundless Battle against Capacity and Performance" ***--Invited***
9:45AM **[1.3] Robert Liu,** *CXMT,* "DRAM Evolution and Position in AI Era" **--Invited**

10:15AM *Break*

Session #2 10:45AM – 12:25PM NAND I
Chairs: **George Matamis,** *Lamresearch*
Henry Chin, *Sandisk*

10:45AM **[2.1] Jan Van Houdt,** *IMEC,* "Special Talk: 50 yr History of IMW" **--Invited**
11:10AM **[2.2] Hang-Ting Lue,** *Macronix*, "An Ideal Approach to 3D NAND Flash Design for Ultra-High IOPS SSDs"
11:35AM **[2.3] Takayuki Gyakushi,** *Sandisk*, "Novel Channel Backside Engineering for Highly Reliable QLC Operation in 3D Flash Memory"
12:00PM **[2.4] Daisuke Ikeno,** *Kioxia*, "Ultra-thin Molybdenum/Polysilicon Stacked Hybrid Floating Gate for Enhanced Program/Erase Efficiency in 3D Flash Memory"

12:25PM *Lunch (Provided) / Committee Luncheon*

Session #3 2:10PM – 4:20PM DRAM I
Chairs: **Seho Lee**, *SK Hynix*
Hao Meng, *CXMT*,

2:10PM **[3.1] Suman Datta,** *Georgia Tech,* "Gain-Cell DRAM Revisited " **--Invited**
2:35PM **[3.2] Ziheng Bai,** *BSAMT*, "Novel "S-Cut" Flows for Highly Uniform Multi-tier Integrated Oxide Semiconductor DRAM"

3:00PM *Break*

3:30PM **[3.3S] Sungwon Cho,** *Georgia Tech*, "Benchmarking Monolithic 1T1C 3D DRAM Cell Architectures"
3:55PM **[3.4] Moonyoung Jeong,** *Samsung*, "Design Considerations for High Performance Vertical Channel DRAM Cell Array Transistor"

Reception 4:30PM – 8:00PM
Sponsored by Applied Materials

Poster Session 4:30PM – 8:00PM
Chair: Arun Karamcheti, *Applied Materials*

Tuesday May 12th

Session #4 8:30AM – 10:10AM Advanced and Emerging Memories I
Chairs: **Mattia Boniardi**, *ST Microelectronics*
Michiel Van Duuren, *NXP*

8:30AM **[4.1] Daniele Ielmini,** *Politechnico di Milano*, "Scaling of nonvolatile memory (NVM) technologies for storage and computing in edge AI" **--Invited**
8:55AM [4.2] **Andrea Ghetti,** *Micron Technology*, "A comprehensive metric for 'spike' related effects in Single Chalcogenide Xpoint Memory"
9:20AM **[4.3] Taras Ravsher,** *IMEC*, "Balancing Memory Window and Write Speed in MFSM Capacitors for Non-Destructive Read-Out FeRAM"
9:45AM **[4.4S] Rivka-Galya Nir-Harwood,** *Technion*, "Picosecond Probing of Selector-Only Memory Revealing a Memory Window in the Time-Domain"

10:10AM *Break*

Session #5 10:40AM – 12:20PM DRAM II
Chairs: **Motoyuki Sato**, *TEL*
Laurent Grenouillet, *CEA-Leti*

10:40AM **[5.1] David Fried,** *Lamresearch*, "Accelerating DRAM Manufacturing Yield using AI/ML and Physics-Based Process Models" **--Invited**
11:05AM **[5.2S] Xuanming Zhang,** *IME*, "First Demonstration of Vertical Bit-line 1T1C 3D DRAM Based-on Stacked Dual-gate IGZO FETs"
11:30AM **[5.3] Eren Canga,** *IMEC*, "Advancements in Gate Length Scaling and Process Optimization for 3D DRAM Selector Transistors"
11:55AM **[5.4] Hang-Ting Lue,** *Macronix*, "A Novel 3D AND-Type 1T1C DRAM Architecture with Local Bitline Transistor (BLT) for Stacked 3D DRAM"

12:20AM *Lunch (Provided)*

Session #6 1:45PM – 3:50PM Memory Enabled Systems
Chairs: **Katherine Chiang**, *TSMC*
Nanbo Gong, *IBM*

1:45PM **[6.1] Stephen Morein,** *SaiMemory*, "Challenges and Innovations in High-Bandwidth DRAM: The Case for Z Angle Memory" **--Invited**
2:10PM **[6.2] Takashi Maeda,** *Kioxia*, "STCO Evaluation of High Bandwidth Storage for Cost-Efficient LLM Training"
2:35PM **[6.3] Rishabh Kishore,** *IMEC*, "3D Charge Coupled Device for High-Density and Cost-Efficient Buffer Memory"
3:00PM **[6.4S] Zhaoqiang Bai,** *BSAMT*, "DRAM Operations under Cryogenic Temperatures: From Device Physics to DIMM Behavior"
3:25PM **[6.5] Hyungrock Oh,** *IMEC*, "Design Architecture Trade-offs for Hybrid Bonded Array-Periphery VBL 3D-DRAM"

3:50PM *Break*

Panel Discussion 4:15PM – 6:00PM
Topic: **"Beyond the Wall: Architecting for Memory Specialization"**
Moderators: Suman Datta, *Georgia Tech,*, **Prashant Majhi,** *Intel*
Panellists: TBA

Banquet 7:00PM – 9:00PM

Wednesday May 13th

Session #7 8:30AM – 10:10AM NAND II
Chairs: **Fumie Kikushima**, *Kioxia*
Jun Okuno, *SONY*

8:30AM **[7.1] Mahendra Pakala,** *AMAT*, "Enabling Memory Inflections for the AI Era through Materials Engineering" **--Invited**
8:55AM **[7.2] Takashi Kashimura,** *Sandisk*, "Novel Control Gate Contact enabling HARC merging in 3D Flash memory"
9:20AM **[7.3] Laurent Breuil,** *IMEC*, "Investigation of Erase Mechanism in Gate Side Injection Devices and its Optimization With an Oxide Semiconductor Channel"
9:45AM **[7.4] Jiahui Yuan,** *Sandisk*, "Improving 3D NAND Read Performance Through Spatial Analysis of Hot-Carrier Injection Along the Memory Channel"

10:10AM *Break*

Session #8 10:35AM – 12:30PM Advanced and Emerging Memories II
Chairs: **Nhan Do,** *Microchip*
Takumi Mikawa, *Screen*

10:35AM **[8.1] Takumi Moriyama,** *Sandisk*, "Array Scale Evaluations of High-k Inside Memory Hole (HIM) Structure for Advanced Z-scaling of 3D Flash Memory"
11:00AM **[8.2] Kana Kudo,** *Kioxia*, "Multi-level In-Memory Computing with 3D Flash Memory using Activation-Time-Modulated Sequential Multi-Block Access"
11:25AM **[8.3] Arvind Sharma,** *IMEC*, "Analysis and Mitigation for Row Hammer in IGZO based eDRAM at Advanced FinFET Node"
11:50AM **[8.4] Athanasios Vasilopoulos,** *IBM*, "Analog In-Memory Computing for Large Language Model Inference: Opportunities and Challenges" **--Invited**

12:15AM **Sangbum Kim**, Closing Remarks
12:25PM **Prashant Majhi**, Best Paper Award Announcement

12:30AM *Lunch (Provided)*