



16th International Memory Workshop

May 12th – 15th 2024

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Summary of Events

Sunday, May 12th

Tutorial #1 – Advanced Memory 8:30AM – 11:30AM

Lunch (Provided) 11:30AM – 1:15PM

Tutorial #2 – Neuromorphic Computing 1:15 PM – 4:15PM

Monday, May 13th

Opening remarks 8:30AM – 8:50AM

Session #1 –Keynotes 8:50AM – 10:20AM

Session #2 – NAND I 10:50AM – 12:05PM

Lunch (Provided)/Committee Luncheon 12:05PM – 2:05PM

Session #3 – Ferro/OTS/STT 2:05PM – 3:45PM

Poster Session + Reception 5:30PM – 8:30PM

Tuesday, May 14th

Session #4 – DRAM 8:30AM – 10:10AM

Session #5 – NAND II 10:40AM – 12:20PM

Lunch (Provided) 12:20PM – 2:15PM

Session #6 – Embedded/RRAM 2:15PM – 3:55PM

Panel Discussion 4:20PM – 5:50PM

Banquet 7:00PM – 9:00PM

Wednesday, May 15th

Session #7 – Ferro 8:30AM – 10:10AM

Session #8 – 3D Processing 10:40AM – 11:30AM

Closing Remarks – Best papers awards 11:30AM – 11:50AM

Sunday, May 12th

Tutorial #1 8:30AM – 11:30AM Advanced Memory

Chair: Fred Chen, *Winbond*

08:30AM **Cheol Seong Hwang**, *Seoul National Univ*, “Dynamic Random Access Memory”

09:20AM **Siva Ramesh**, *IMEC*, “Advanced channel crystallization techniques to improve current conduction in 3-D NAND”

10:10AM—10:40AM **Coffee Break**

10:40AM **Di Geng** (o/b/o **Ling Li**), *IME/China*, “IGZO 2T0C DRAM”

11:30AM—1:15PM **Lunch (Provided)**

Tutorial #2: 1:15PM – 4:15PM Neuromorphic computing

Chair: Stephan Menzel, *Forschungszentrum Juelich*

1:15PM **Masatoshi Ishii**, *IBM/Japan*, “AI hardware accelerators with analog memory: Towards energy-efficient compute”

2:05PM **Ken Takeuchi**, *Univ. of Tokyo*, “Non-volatile Memory-based Analog CiM for Edge AI Applications”

2:55PM—3:25PM **Coffee Break**

3:25PM **Giuseppe Piccolboni**, *Weebit Nano*, “A Complete No-Brainer: ReRAM for Neuromorphic Computing”

Monday, May 13th

Poster Session

6:00PM – 8:30PM

[P1] Karansingh Thakor, *Indian Institute of Technology Bombay*, “Comprehensive physics-based modeling of post-cycling long-term data retention in 176L 3-D NAND Flash Memories”

[P2] Naoko Misawa, *The University of Tokyo*, “Embedded Transformer Hetero-CiM: SRAM CiM for 4b Read/Write-MAC Self-attention and MLC ReRAM CiM for 6b Read-MAC Linear&FC Layers”

[P3] Won-Tae Koo, *SK Hynix*, “Modeling and Demonstration for Multi-level Weight Conductance in Computational FeFET Memory Cell”

[P4] Hitomi Tanaka, *Kioxia*, “Overcome the End of Life of 3D Flash Memory by Recovery Annealing, Aiming for Carbon Neutrality in Semiconductor Manufacturing”

[P5] Yu Li, *Fudan University*, “High-efficient and Comprehensive Modeling of MFIM Ferroelectric Tunnel Junctions for Non-volatile/Volatile Applications”

[P6S] Dasom Lee, *UC Berkeley*, “SiGe/Si Heterojunction Drain Transistor for Faster 3D NAND Flash Memory Erase”

[P7] Hongxi Liu, *Truth Memory Corporation*, “Process optimization and cryogenic evaluation of spin-orbit torque magnetic random-access memory”

[P8] Jijun Kim, *SK Hynix*, “Realistic Noise-aware Training as a Component of the Holistic ACiM Development Platform”

[P9] Wei-Chih Chien, *Macronix*, “A Novel Program-verify Free and Low Drift Multi-level Operation on Cross-point OTS-PCM for In-Memory Computing Application”

[P10S] Thomas Bauvent, *Univ. Grenoble Alpes*, “Optimizing RRAM Performance: A Comparative Analysis of Forming Strategies”

[P11S] Daniel Schon, *Forschungszentrum Jülich*, “Understanding the Thermal Aspects in Dense RRAM Memory Arrays”

[P12S] Yuan He, *Tsinghua University*, “A 3.75Mb Embedded RRAM IP on 40nm High-Voltage CMOS Technology”

[P13S] Jun Yu, *Huazhong UST*, “High Operation Speed(10ns/100ns) and Low Read Current (sub-1 μ A) 2D Floating Gate Transistor”

[P14S] Saifei Dai, *IME/China*, “Role of Nitrogen in Suppressing Interfacial States Generation and Improving Endurance in Ferroelectric Field Effect Transistors”

[P15S] Yuanbiao Li, *University of Sci & Tech, China*, “CMOS-Compatible Low-T Processing Methods for HZO-based DRAM capacitors by E-field Cycling”

Monday May 13th08:30AM **Antonio Arreghini, Opening Remarks****Session #1 8:50AM – 10:20AM** **Keynotes****Chairs:** **Antonio Arreghini, IMEC**
Haitao Liu, Micron8:50AM **[1.1] Kwi Wook Kim, SK Hynix**, "Present and Future, Challenges of High Bandwidth Memory". --**Invited**9:20AM **[1.2] Daewon Ha, Samsung**, "Exploring Innovative IGZO-based DRAM Cell Architectures and Key Technologies for Sub-10nm Node" --**Invited**9:50AM **[1.3] Ryota Katsumata, Kioxia**, "Flash memory revolution: journey from 2D to 3D, migrating to modular memory fabrication". --**Invited**10:20AM **Break****Session #2 10:50AM – 12:05PM** **NAND I****Chairs:** **Bruce Hsu, Macronix**
Yong Kyu Lee, Samsung10:50AM **[2.1] Sana Rachidi, IMEC**, "Pure-Metal Replacement Gate for Reliable 30 nm Pitch Scaled 3D NAND Flash"11:15AM **[2.2] Noboru Shibata, Kioxia**, "Novel Multi-Level Coding and Architecture Enabling Fast Random Access for Flash Memory"11:40AM **[2.3] Po-Hao Tseng, Macronix**, "3D-NAND based Filtering Cube with High Resolution 2D Query and Tunable Feature Length for Computational SSD"12:05PM **Lunch (Provided) / Committee Luncheon****Session #3 2:05PM – 3:45PM** **Ferro/OTS/STT****Chairs:** **Nhan Do, Microchip**
Martin Lueker-Boden, Western Digital2:05PM **[3.1] Shimeng Yu, Georgia Tech**, "Engineering nVcap From FEOL to BEOL with Ferroelectric Small-signal Non-destructive Read" --**Invited**2:30PM **[3.2] Alex Grun, Macronix**, "AsSeGeS and GeN Heterostructures for Superior OTS Performance"2:55PM **[3.3S] Taras Ravsher, KU Leuven/IMEC**, "Novel Cross-Point Architecture utilizing Distributed Diode Selector for Read Margin Amplification"3:20PM **[3.4] Valerio Pica, IMEC**, "A novel test and analysis scheme to elucidate tail bit characteristics in STT-MRAM arrays"3:45PM **Break****Reception 6:00PM – 8:00PM**

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Poster Session 5:30PM – 8:30PM**Chair:** Gill Lee, Applied Materials**Tuesday May 14th****Session #4 8:30AM – 10:10AM** **DRAM****Chairs:** **Seho Lee, SK Hynix****Hao Meng, CXMT**8:30AM **[4.1] Andy Hsu, NEO semiconductor**, "3D X-DRAM: A novel 3D NAND-like DRAM cell and TCAD simulations" -- **Invited**.8:55AM **[4.2] Pratik Vyas, Applied Materials**, "Gate-All-Around SRAM: Performance Investigation and Optimization Towards Vcc_min Scaling"9:20AM **[4.3] Hiroko Inoue, SEL**, "Heterogeneous OS-FETs Comprising Planar FET and Vertical Channel FETs Monolithically Stacked on Si CMOS, Enabling 1-Mbit 3D DRAM" --**Invited**.9:45AM **[4.4] Hang-Ting Lue, Macronix**, "Multi-Gate Access Transistor to Minimize GIDL Leakage Current for Scaling 2-tier Stacked 4F2 DRAM Below Equivalent 10nm Node".10:10AM **Break****Session #5 10:40AM – 12:20PM** **NAND II****Chairs:** **Tomoya Sanuki, Kioxia****Bin Gao, Tsinghua University**10:40AM **[5.1] Mahendra Pakala, Applied Materials**, "Demonstration of High-Growth-Rate Epitaxially Grown Si Channel on 3D NAND vehicle with Memory Functionality"11:05AM **[5.2] Xi-wei Lin, Synopsys**, "Device and Process Simulations for Memory Technology Exploration and Development" -- **Invited**11:30AM **[5.3] Laurent Breuil, IMEC**, "Gate Side Injection Operating Mode for 3D NAND Flash Memories".11:55AM **[5.4] Lance Fernandes, Georgia Tech**, "Design Framework for Ferroelectric Gate Stack Engineering of Vertical NAND Structures for Efficient TLC & QLC"12:20PM **Lunch (Provided)****Session #6 2:15PM – 3:30PM** **Embedded/RRAM****Chairs:** **Shibun Tsuda, Renesas****Katherine Chiang, TSMC**2:15PM **[6.1] Sven Beyer, Global Foundries**, "Charge trapping challenges of CMOS embedded complementary FeFETs" -- **Invited**2:40PM **[6.2] YoungJae Kwon, SK Hynix**, "Improvement of MAC Accuracy using Oxygen Diffusion Barriers in Resistive Synaptic Cell Arrays"3:05PM **[6.3] Bastien Beltrando, Applied Materials**, "Self-rectifying non-volatile tunneling synapse: multiscale modeling augmented development".3:30PM **[6.4] Ralf Richter, Global Foundries**, "Performance and Reliability of Technology Qualified 34 Mb Split-Gate eFLASH Macro in 28 nm HKMG"3:55PM **Break****Panel Discussion 4:20PM – 5:50PM**

Topic: "Advanced channel materials for memory application"

Moderator: **Jian Chen, Stanford University****Panellists:** **Dr. Mahendra Pakala, Applied Materials****Dr. Si-woo Lee, Samsung****Dr. Ryota Katsumata-, Kioxia****Dr. Siva Ramesh, IMEC****Dr. Joodong Park, SK Hynix****Banquet 7:00PM – 9:00PM****Wednesday May 15th****Session #7 8:30AM – 10:10AM** **Ferro****Chairs:** **Laurent Grenouillet, CEA-Leti****Jinseong Heo, Samsung**8:30AM **[7.1] Ashonita Chavan, Micron Technology**, "Materials Engineering for High Performance and High Endurance Ferroelectric Memory". -- **Invited**8:55AM **[7.2S] Boncheol Ku, Hanyang University**, "A Novel 3D Gate-All-Around Vertical FeFET with Back-Gate Structure for Disturbance-Less Program Operation".9:20AM **[7.3] Maximilian Lederer, Fraunhofer IPMS**, "Enhanced reliability and trapping behavior in ferroelectric FETs under cryogenic conditions"9:45AM **[7.4] Olivier Billoint, Univ of Grenoble Alpes**, "Charge-based Sense Demonstration in 1T-1C HZO FeRAM Arrays to Overcome CBL-Induced Band Size Limitations".10:10AM **Break****Session #8 10:40AM – 11:50AM** **3D Processing****Chair:** **Sangbum Kim, Seoul National University**10:40AM **[8.1] Wei-Chen Chen, Macronix**, "Improved 3D DRAM Design Based on Gate-Controlled Thyristor Featuring Two Asymmetrical Horizontal WL's and Vertical BL for Better Cell Size Scaling and Array Selection"11:05AM **[8.2] Gaurav Mehta, Applied Materials**, "D2W Hybrid Bonding Challenges for HBM." -- **Invited**11:30AM **Antonio Arreghini, Closing Remarks**11:40AM **Haitao Liu, Best Paper Award Announcement****Premium Sponsor****Local Sponsors****Platinum Sponsor****Gold Sponsors****Silver Sponsors**