Practical Papers, Articles and Application Notes

Robert G. Olsen, Technical Editor

In this issue you will find two practical papers that should interest members of the EMC community. The first is entitled, "Comparison of Frequency Domain and Time Domain Measurement Procedures for Ultra Wideband Antennas," by W. Sörgel, F. Pivit, and W. Wiesbeck. In this paper, the authors discuss the issue of characterizing antennas for ultra wideband (UWB) applications and some of the implications for EMC. This material forms some of the background for answering interesting questions concerning the co-existence of narrowband and UWB devices. This paper was originally presented at the 2003 Antenna Measurement and Techniques Association (AMTA) Conference. The second paper is entitled, "Electromagnetic Modeling of Switching Noise in On-chip Power Distribution Networks," by J. Mao, W. Kim, S. Choi, M. Swaminathan, J. Libous and D. O'Connor. In this paper, the authors investigate of the effect of substrate loss on simultaneous switching noise in on-chip power distribution networks, a very relevant topic. The paper won the Shri. Mukhopadyay Best Paper Award at the INCEMIC '03 Symposium, which was held in Chennai, India.

The purpose of this section is to disseminate practical information to the EMC community. In some cases the material is entirely original. In others, the material is not new but has been made either more understandable or accessible to the community. In others, the material has been previously presented at a conference, but has been deemed especially worthy of wider dissemination. Readers wishing to share such information with colleagues in the EMC community are encouraged to submit papers or application notes for this section of the Newsletter. See page 3 for my e-mail, FAX and real mail address. While all material will be reviewed prior to acceptance, the criteria are different from those of Transactions papers. Specifically, while it is not necessary that the paper be archival, it is necessary that the paper be useful and of interest to readers of the Newsletter.

Comments from readers concerning these papers are welcome, either as a letter (or e-mail) to the Associate Editor or directly to the authors.

Comparison of Frequency Domain and Time Domain Measurement Procedures for Ultra Wideband Antennas

W. Sörgel, F. Pivit, and W. Wiesbeck

Abstract

Spectrum is presently one of the most valuable goods worldwide as the demand is permanently increasing and it can be traded only locally. The United States FCC has opened a portion of the spectrum from 3.1 GHz to 10.6 GHz, i.e. a bandwidth of 7.5 GHz, for unlicensed use with up to –41.25 dBm/MHz EIRP [1]. Numerous applications in communications and sensor areas are showing up now. Like all wireless devices, these devices have an antenna as an integral part of the air interface. The antennas are modeled as linear time invariant (LTI) systems with a transfer function. The measurement of the antenna's frequency dependent directional transfer function is described. Furthermore, the measured transfer function is transformed into time domain, where it is used to characterize pulse-shaping properties of the antennas. Additionally, measurements in time domain, which were performed with a picosecond pulse generator and a 50 GHz sampling oscilloscope, are presented and compared to the transformed frequency domain measurements. These measurements enable the realistic characterization of ultra wideband antennas for UWB link level simulations.

Keywords: Ultra Wideband, Time Domain Antenna Measurement, Dispersive Antenna Effects.

Antenna Model

In general, the electrical properties of antennas are characterized by input impedance, efficiency, gain, effective area, radiation pattern and polarization properties [2, 3]. For narrow band applications it is possible to analyze these at the center frequency of the system. For larger bandwidths, all of them become more or less frequency dependent. In order to calculate the transient radiation behavior, these parameters have to be evaluated in terms of amplitude and phase over the ultra wideband frequency range. The magnitude information alone is not sufficient for the characterization of the transient radiation behavior. One proper approach to take transient phenomena into account is to model the antenna as a linear time invariant transmission system with the exciting voltage V_{exc} as input parameter and the radiated electrical far field E_{rad} as output

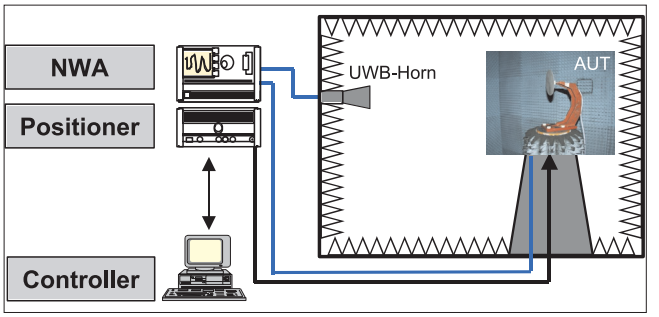

Fig. 1. Measurement setup for transmission measurement with the vector network analyzer (VNWA).

parameter. This system can be fully characterized by its impulse response. Assuming free space propagation, this can be written like equation (1) as shown in [4, 5, 6, 7, 9]. The dimension of the antenna's normalized impulse response $h_n(\tau, \theta, \psi)$ is m/s, which relates to the meaning of an effective antenna height.

$$\frac{\vec{E}_{\mathrm{rad}}(t, r, \theta, \psi)}{\sqrt{Z_0}} = \frac{1}{2\pi\, r\, \mathrm{c}}\, \delta\left(\tau - \frac{r}{c}\right) * \vec{h}_{\mathrm{n}}(\tau, \theta, \psi) * \frac{1}{\sqrt{Z_{\mathrm{C}}}} \frac{dV_{\mathrm{exc}}(t)}{\mathrm{d}t} \tag{1}$$

The radiated far field is given by the convolution of the antennas normalized impulse response h_{n} with the time derivative of the driving voltage. The derivative character of the antenna model can be explained by the fact that there has to be a capacitive or inductive coupling of the source voltage to the radiated wave. Therefore, there is no far field radiation of static fields with $\mathrm{d}\cdot/\mathrm{dt} = 0$. The coupling characteristics are covered by the properties of the impulse response h_{n}. Z_0 denotes the characteristic free space impedance, Z_{c} is the reference impedance at the antenna connector (assumed to be frequency independent), r is the distance from the antenna. The convolution with the Dirac function $\delta(\tau - r/\mathrm{c})$ represents the time delay due to the finite speed of light c. Together with the attenuation $\sim 1/\mathrm{r}$ this models the free space propagation channel. The antennas impulse response depends on the direction (Θ, ψ) of the radiation and is a vector according to the polarization vector properties (co-polarization and cross-polarization) of the modeled antenna.

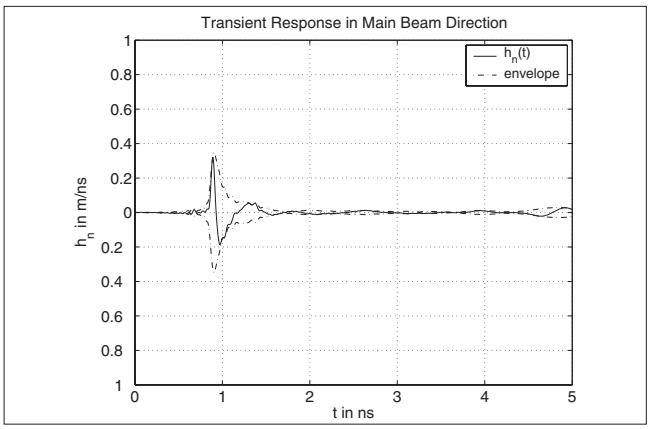

Fig. 3. Vivaldi antenna: Impulse response for main beam direction (measurement bandwidth 20 GHz).

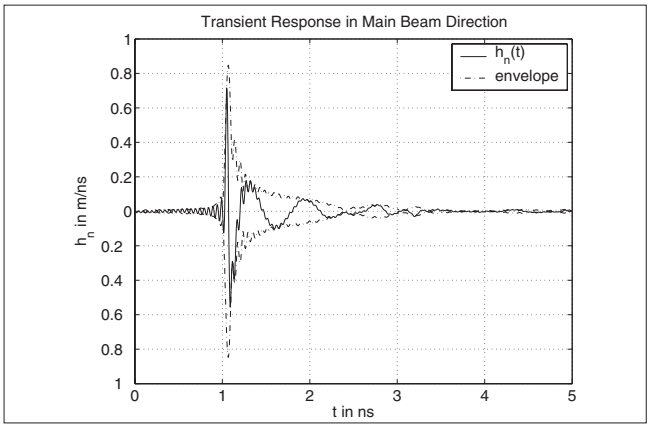

Fig. 2. Horn: Impulse response for main beam direction and co-polarization (measurement bandwidth 20 GHz).

Assuming an incident plane wave on the antenna in the direction $(\Theta_{\mathrm{w}}, \psi_{\mathrm{w}})$ with the polarized field strength E_{inc}, the given model fulfils the reciprocity theorem [4] and the output voltage of the antenna in the receive mode can be characterized by

$$\frac{V_{\mathrm{rec}}(t)}{\sqrt{Z_{\mathrm{C}}}} = \vec{h}_{\mathrm{n}}(\tau, \theta_{\mathrm{w}}, \psi_{\mathrm{w}}) * \frac{\vec{E}_{\mathrm{inc}}(t)}{\sqrt{Z_0}} \tag{2}$$

The main advantage of this antenna model is the option to describe the radiation of arbitrary waveforms like Gaussian pulses, chirps, orthogonal frequency division multiplex (OFDM) signals, etc. The model covers all dispersive effects that result from a particular antenna structure (e.g. the influence of coupled resonators and the related varying group delay due to nonlinear phase response). The influence of frequency dependent matching and ohmic losses are also covered.

Frequency Domain Measurement Setup and Signal Processing

The frequency domain measurements presented here have been performed with a HP8530A vector network analyzer and a PHYTRON positioner supporting the antenna under test (AUT) within an anechoic chamber (Fig. 1). As reference antenna, an ultra wide band TEM horn antenna is used. The measurement system is fully computer controlled. The measurement frequency range is 400 MHz to 20 GHz (24.5 MHz resolution). A proper calibration has been used in order to eliminate dispersive and attenuation effects of the connecting cables. The direct result of the measurement is the transmission coefficient

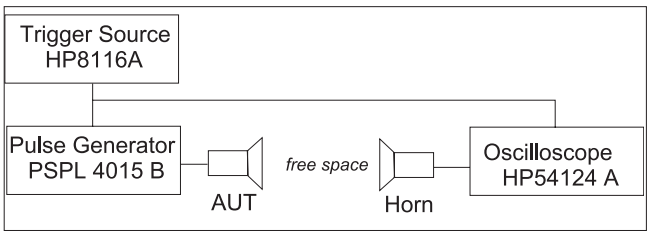

Fig. 4. Schematic of the setup for time domain transmission measurement.

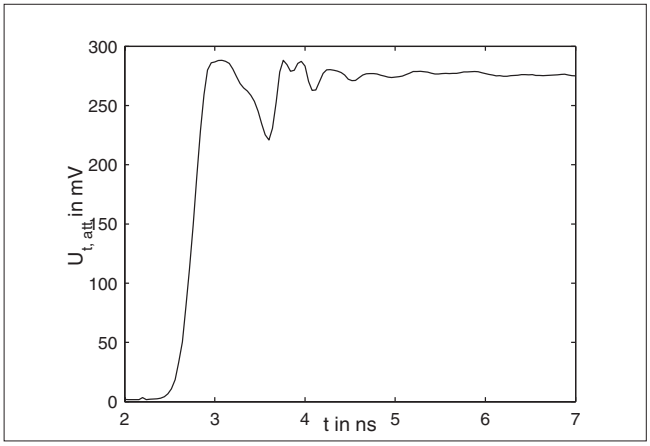

Fig. 5. Measurement of the pulse generators output (rising edge, 30 dB attenuation).

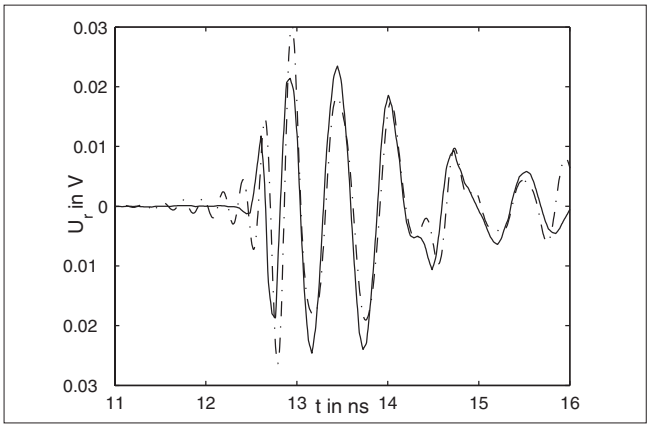

Fig. 6. Transmission from horn to horn (excitation as shown in Fig. 5): measurement averaged over 512 shots (solid line) and simulation (dashed line).

S_{21} between the ports of the AUT and the reference antenna, which can be determined by combining eq. (1) and (2) and transforming the result into frequency domain:

$$S_{21}(\omega) = \frac{U_{\mathrm{rx}}(\omega)}{U_{\mathrm{tx}}(\omega)} = H_{\mathrm{ref}}(\omega)\; H_{\mathrm{AUT}}(\omega)\; \frac{j\omega}{2\pi Rc} e^{-j\omega R/c}. \tag{3}$$

With two identical UWB horn antennas, the complex transfer function $H_{\mathrm{ref}}(f)$ of the reference horn antenna can be calculated from (3) since the distance R between the two antennas is known:

$$H_{\mathrm{ref}}(\omega) = \sqrt{\frac{2\pi Rc}{j\omega} S_{21}(\omega)\, e^{j\omega R/c}}. \tag{4}$$

In order to obtain physical results, the phase of the transmission coefficient S_{21} has to be unwrapped correctly. Thus a proper frequency resolution is needed. With the known reference $H_{\mathrm{tx}}(f)$ the transfer functions of the AUT is easily calculated solving (3) for $H_{\mathrm{rx}}(f)$.

$$H_{\mathrm{AUT}}(\omega) = \frac{2\pi Rc}{j\omega} \frac{S_{21}(\omega)}{H_{\mathrm{ref}}}\, e^{j\omega R/c} \tag{5}$$

This has to be done for all relevant 2-D cuts of the antenna radiation pattern at two orthogonal polarizations (co- and cross-polarization). The resulting complex transfer function is obtained for discrete positive frequencies with a resolution Δf. It can be transformed into time domain by an inverse discrete Fourier transform (IDFT) with the appropriate scale factor:

$$h_{\mathrm{AUT}}(k\Delta t) = \frac{1}{N\Delta t} \sum_{n=0}^{N-1} H_{\mathrm{AUT}}(n\Delta f)\, e^{j\frac{2\pi}{N}kn} \tag{6}$$

The result of (6) is a complex discrete time function with a sampling rate $\Delta t_{\mathrm{raw}} = 1/f_{\max}$. The measured data is complemented by zero padding for 0 – 400 MHz and 20 – 200 GHz. This leads to a fine interpolation of the antenna's impulse response with an interpolated time resolution of $\Delta t = 5$ ps. Since only positive frequencies are employed for the transformation, it yields a complex time discrete "analytical" impulse response. Its magnitude is referred to as impulse response envelope $|h_{\mathrm{AUT}}|$.

For the evaluation of V_{rec} according to (1) and (2) together with the measured h_{AUT}, the derivative of the simulated time domain excitation voltage has to be converted first into a discrete time "analytical" signal by the discrete Hilbert transform [6]. The estimate for the output voltage of the receiving antenna is then computed in frequency domain by multiplying the discrete frequency vectors of the antennas' transfer functions with the exciting signals according to (3). This procedure makes use of the cyclic convolution properties of the discrete Fourier transform, and it has to be ensured that the length of the time vectors is sufficient in order to avoid ambiguities.

The transfer functions of the connecting cables are measured separately and inserted in the simulation. Therefore, it is assumed that the cables are matched and no multiple reflections occur. The obtained V_{rec} again is a complex time discrete "analytical" signal and is transformed into a real valued time function by applying the inverse Hilbert transform [7].

Measurement Results in Frequency Domain

The impulse response of the employed reference horn antenna (double ridged TEM horn, 2–20 GHz) in the E-plane shows a sharp and high peak value in the main beam direction as can be seen from Fig. 2. This is expected since the TEM horn structure is non resonant and provides a smooth transition from the transmission line to the free space. However a perceptible ringing does occur. This ringing is due to reflections at the aperture of the antenna for lower frequencies at approximately 1.4 GHz, which are in fact out of the specified frequency range of the antenna.

The antennas were placed in a distance of 2.64 m and were aligned for co-polarization and maximum gain.

The impulse response of a Vivaldi antenna, which has been designed for the UWB frequency range and which was presented in [8] shows an impulse response with a sharp peak

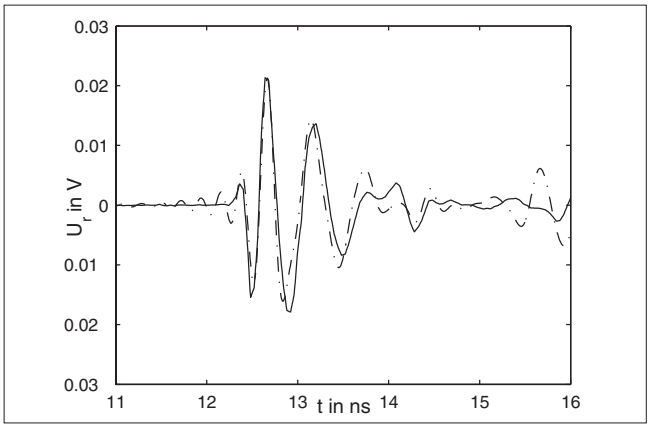

Fig. 7. Transmission from Vivaldi to horn (excitation as shown in Fig. 5): measurement averaged over 512 shots (solid line) and simulation (dashed line).

and low ringing (Fig. 3) like the horn antenna. The antenna has significantly less gain then the horn antenna, which is mainly due to its smaller aperture (50 mm tapered slot width). Therefore, the peak magnitude of its impulse response is with p = 0.35 m/ns lower than that of the Horn p = 0.93 m/ns. The directional evaluation of the properties of their impulse response shows an almost constant behavior within the main lobe [10, 11].

Measurement in Time Domain

In order to verify the frequency domain measurements of the impulse responses, the signal processing antenna measurements in the time domain have been performed for the horn antenna and the Vivaldi antenna.

The principle set up for the transmission measurement consists of a Pico Second Pulse Labs (PSPL) 4015 B pulse generator and a HP54124A 50 GHz sampling oscilloscope (Fig. 4). The antennas are placed within an anechoic chamber. The AUT is placed on the positioner and directly connected to the pulse generator with a short coax cable (Suhner Sukoflex, 50 cm). The receiving ridged horn antenna is mounted in a fixed position on the enclosure of the anechoic chamber. It is connected to the sampling head of the oscilloscope with a second short coax cable (Suhner Sukoflex, 100 cm). The transmitting and receiving antennas have been aligned for co-polarization and maximum gain. The pulse generator and the oscilloscope are triggered by a common trigger source with $V_{pp} = 200\,mV$, which is connected with equal length BNC cables to both instruments. The pulse generator produces a rectangular output voltage, which drops from 9 V to 0 V and steps back up to 9 V after 10 ns with a rise time of 247 ps. In the following this rising edge has been used. The maximum input voltage range of the HP54124A is ±2 V. Therefore, a 30~dB attenuator had to be used for the measurement of the pulse generators output voltage, which is shown in Fig. 5.

Due to the wide measurement bandwidth, the noise floor of the HP54124A is about 30 mV without averaging. This is improved to 2 mV by averaging over 512 shots.

In Fig. 6 the solid line shows the result of the time domain transmission measurement for two ridged horn antennas. It is compared to a simulation using the NWA measured impulse response of the horn antenna and together with the de-attenuated time domain measurement of the excitation. Both graphs agree very well. The measurement was repeated for the Vivaldi antenna (Fig. 7), which shows again a very good agreement between the simulation including the processed frequency domain measurement of the transfer functions of horn and Vivaldi. The simulation shows some high frequency oscillation of low amplitude at the beginning of the pulse, which is due to processing artifacts.

Comparison of Measurement Procedures

Since antennas are linear time invariant systems, they can be fully described in both frequency or time domain. The particular representation of the antenna's transfer function yields the full information in each domain. However, some effects like ringing, maximum pulse amplitudes, group delay characteristics or frequency selective behavior are investigated best in the domain where they are defined. Therefore, one measurement in either frequency or time domain will provide this information by applying adequate signal processing for the transformation between both domains. The measurement in frequency domain exhibits standardized and easy calibration methods and has a dynamic range above 90 dB. In time domain, the lower dynamic range and the bandwidth restrictions due to the used pulse shape complicate the measurement. Since the results of both measurements match perfectly well, the use of a network analyzer is preferred for the measurement of the antenna's transfer function because it enables one to measure small antennas with low gain due to its high dynamic range.

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Biographies

Werner Sörgel *was born in Karlsruhe, Germany in 1974. He received the Dipl.-Ing. degree in electrical engineering (M.S.E.E.) in 2001. Since May 2001 he has been with the Institut für Höchstfrequenztechnik und Elektronik (IHE), University of Karlsruhe, Germany, as a research associate. He is currently working towards the Dr.-Ing. (Ph.D.E.E.) degree. His present research topics are mainly focused on Ultra Wideband (UWB) antenna design and characterization. He has been awarded the 2003 best student paper award of the Antenna Measurement Techniques Association. Furthermore, he has experience with electromagnetic wave propagation, microwave heating applicators, and electromagnetic compatibility. He has been a student member of the IEEE since 2001.*

Florian Pivit *was born in Backnang, Germany, 1972. He received the Dipl.-Ing. (M.S.E.E.) degree in electrical engineering from the University of Karlsruhe, Karlsruhe, Germany in 2000. In 1997, he spent six months as an intern at the Alaskan SAR Facility (ASF) in Fairbanks, AK, working on SAR-calibration. From 1999 to 2000 he was a cooperator with Anaren Microwave Inc., NY, where he worked on passive antenna feed network designs in LTCC. He joined the Institut für Höchstfrequenztechnik und Elektronik at the University of Karlsruhe, where he performs research on analog frontend design for multi standard base stations and on multi- and broadband base station antennas. His further professional interests are on passive and active circuit design and on high power RF-amplifier design. He also gives tutorials in antenna design at the University of Karlsruhe.*

Werner Wiesbeck *(SM 87, F 94) received the Dipl.-Ing. (M.S.E.E.) and the Dr.-Ing. (Ph.D.E.E.) degrees from the Technical University Munich in 1969 and 1972, respectively. From 1972 to 1983 he was with AEG-Telefunken in various positions including that of head of R&D of the Microwave Division in Flensburg and marketing director, Receiver and Direction Finder Division, Ulm. During this period he had product responsibility for mm-wave radars, receivers, direction finders and electronic warfare systems. Since 1983 he has been director of the Institut für Höchstfrequenztechnik und Elektronik (IHE) at the University of Karlsruhe (TH), where he had been dean of the Faculty of Electrical Engineering. Research topics include radar, remote sensing, wireless communication and antennas. In 1989 and 1994, respectively, he spent a six month sabbatical at the Jet Propulsion Laboratory, Pasadena. He is a member of the IEEE GRS-S AdCom (1992 - 2000), Chairman of the GRS-S Awards Committee (1994 - 1998, 2002 - to present), Executive Vice President IEEE GRS-S (1998 - 1999), President IEEE GRS-S (2000 - 2001), Associate Editor IEEE-AP Transactions (1996-1999), past and present Treasurer of the IEEE German Section (1987-1996, 2003-2005). He has been General Chairman of the '88 Heinrich Hertz Centenial Symposium, the '93 Conference on Microwaves and Optics (MIOP '93), the Technical Chairman of the International mm-Wave and Infrared Conference 2004, and he has been a member of the scientific committees of many conferences. For the Carl Cranz Series for Scientific Education, he serves as a permanent lecturer for radar system engineering, wave propagation, and mobile communication network planning. He is a member of an Advisory Committee of the EU - Joint Research Centre (Ispra/Italy), and he is an advisor to the German Research Council (DFG), to the Federal German Ministry for Research (BMBF) and to industry in Germany. He is recipient of a number of awards, lately the IEEE Millennium Award, and the IEEE GRS Distinguished Achivement Award. He is a Fellow of the IEEE, a Member of the Heidelberger Academy of Sciences, and a Member of Acatech (German Academy of Engineering).*

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Electromagnetic Modeling of Switching Noise in On-chip Power Distribution Networks

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Abstract

An investigation of the effect of substrate loss on simultaneous switching noise (SSN) in on-chip power distribution networks is presented. In order to characterize the multi-layered power buses accurately for on-chip switching noise simulation, modeling of Vdd/Ground rails over finite-resistivity substrates should include dielectric loss. The complete circuit model of power rails is then represented using RLCG elements. The waveform and propagation pattern of the noise are captured using the finite difference time domain (FDTD) technique. This paper shows the effect of silicon substrate with different resistivities on the propagation of on-chip switching noise.

Introduction

Advanced System-on-Chip (SoC) or System-on-Package (SOP) designs combine analog, radio frequency (RF), and mixed analog/digital circuits into a single chip, or highly integrated chip sets. Simultaneous switching noise caused by switching activity of high-speed CMOS circuits not only affects digital functionality but also deteriorates the performance of its neighboring analog and RF circuits, such as causing multi-tone outputs in Low-Noise Amplifier (LNA) and jitter in phase-locked loops [1]. As the clock frequency approaches 10 GHz, future microprocessor sizes are expected to be comparable to a wavelength, in which electromagnetic wave effects become significant [2]. The deep sub-micron trend in semiconductors increases the number of CMOS transistors on die dramatically and simultaneously reduces supply voltage, in accordance with the CMOS scaling rules. This leads to degradation in the signal-to-noise ratio. Hence, modeling and simulation of on-chip power distribution become an important problem, which currently does not have a good solution.

Extensive research has been carried out by numerous authors for on-chip switching noise analysis [2–5]. Full-chip power supply analysis from [3] adopted the periodicity of on-

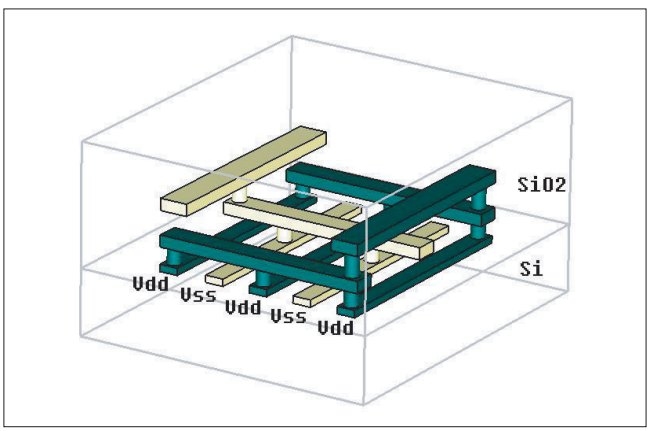

Fig. 1. Side view of on-chip power grid.

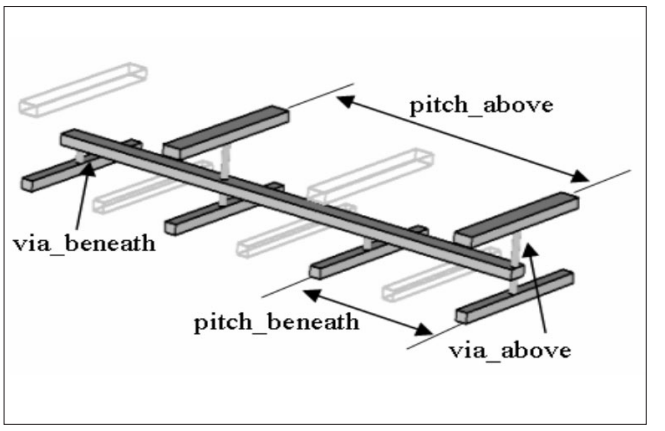

Fig. 2. On-chip power bus connection.

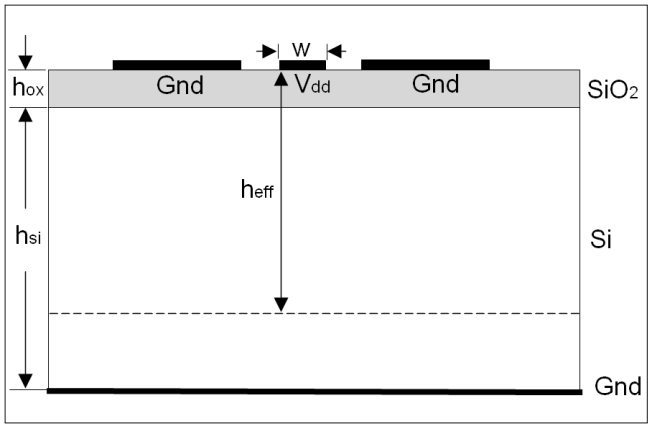

Fig. 3. On-chip coplanar waveguide.

chip power grid and used a unit cell approach. After constructing the model for a unit cell, the rest of the grids were established by repeating/mirroring the unit cell. Depending on the size of the unit cell, the iso-potential assumption of this approach and artificial boundary introduced can result in erroneous noise voltages.

In [4], the RLC equivalent circuit of on-chip power rails was used to characterize switching noise and analytical expressions were derived. But single R, L and C representation can depict neither the parasitics of the complex multi-conductor structure nor the distributed effect at high frequencies. In addition, the resonant frequency defined by one LC pair can underestimate the frequency response of on-chip power distribution networks. Though resonance analysis has been discussed in [5] and noise upper bounds have been provided, the effect of lossy substrate is not included in the simulation.

The equivalent circuit representation of an on-chip power distribution network requires an enormous number of circuit nodes. SPICE-like simulators use modified nodal approach (MNA) to construct the system matrix equation and invert it with sparse matrix algorithms. The matrix inversion is time consuming and CPU time increases dramatically with the order of unknowns. Instead, the Latency Insertion Method (LIM) along with branch capacitors [2], [6] can be used to analyze large network problems using Finite Difference Time Domain techniques.

This paper provides details on the simulation of on-chip power distribution networks by including lossy silicon substrate effects. The results have been compared for low resistivity and high resistivity silicon substrates.

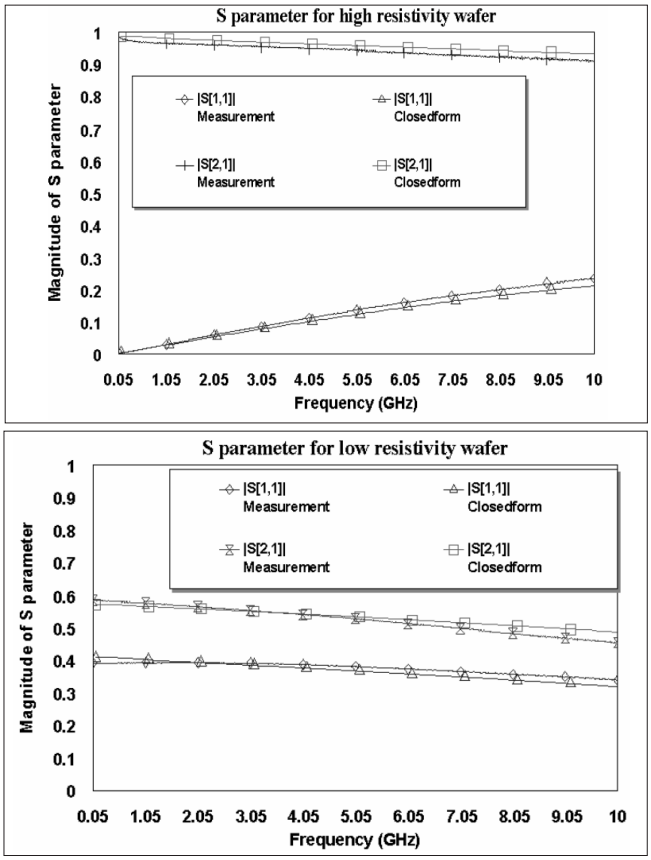

Fig. 4. S parameter of CPW on wafer with different resistivity.

On-Chip Power Grid

A side view of on-chip power grid is shown in Fig. 1.

On-chip power grid distribution uses a grid instead of planes to deliver voltage to active circuits on the chip. The power (Vdd) and ground (Vss) buses are parallel in the same layer, but orthogonal to each other on neighboring layers. Vias are used where there is a crossover of two buses with the same potential. Pitch between buses is relatively large at the chip-package

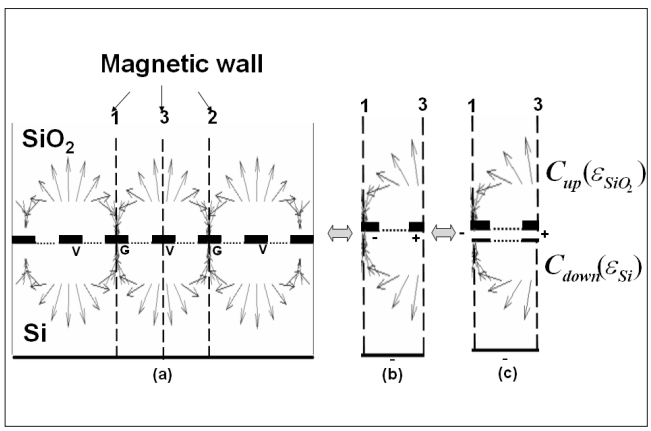

Fig. 5. Electric field of CMC and capacitor calculation.

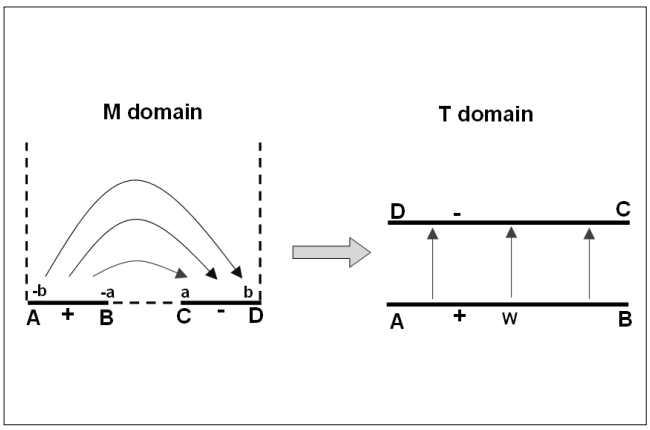

Fig. 6. Conformal mapping of Cup.

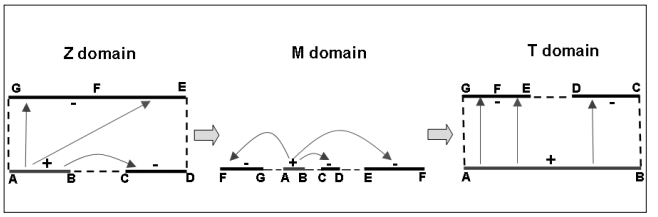

Fig. 7. Conformal mapping of Cdown.

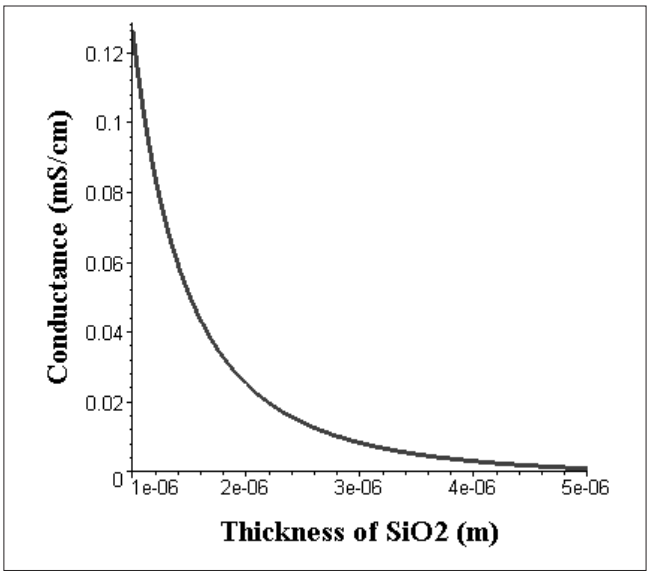

Fig. 8. Conductance Vs. SiO_2 thickness.

interface and it shrinks gradually as the power buses get closer to active circuits on the silicon. The 3-D power grid is embedded in SiO_2 and is present over the silicon substrate.

Several terminologies will be defined here to ease further discussion. Parameters "via_beneath" and "via_above" denote the via used to connect the current layer to the layer beneath and above it, respectively. Parameters "pitch_beneath" and "pitch_above" denote the distance between two via-beneaths and two via-aboves, which is the pitch of the layer beneath and above the current layer. Parameter "pitch_current" denotes the pitch of current layer. It is assumed that the chip has a square shape and "chip_size" denotes the length of the edge. Each Vdd/Gnd metal line can be split into several sections, each of which has the length of "pitch_above." One section can be divided into several segments, each of which has the length of "pitch_beneath." The graphical representation of these parameters is shown in Fig. 2.

The feature of on-chip power grid results in procedures for the construction of circuit models as follows:

1. At each layer, the number of Vdd/Gnd buses is determined by chip_size/pitch_current.
2. The number of sections along each bus is determined by chip_size/pitch_above.
3. The number of segments within every section is determined by pitch_above/pitch_beneath.
4. Via_beneath and via_above are distributed along Vdd/Gnd buses with the period of pitch_beneath and pitch_above, respectively.

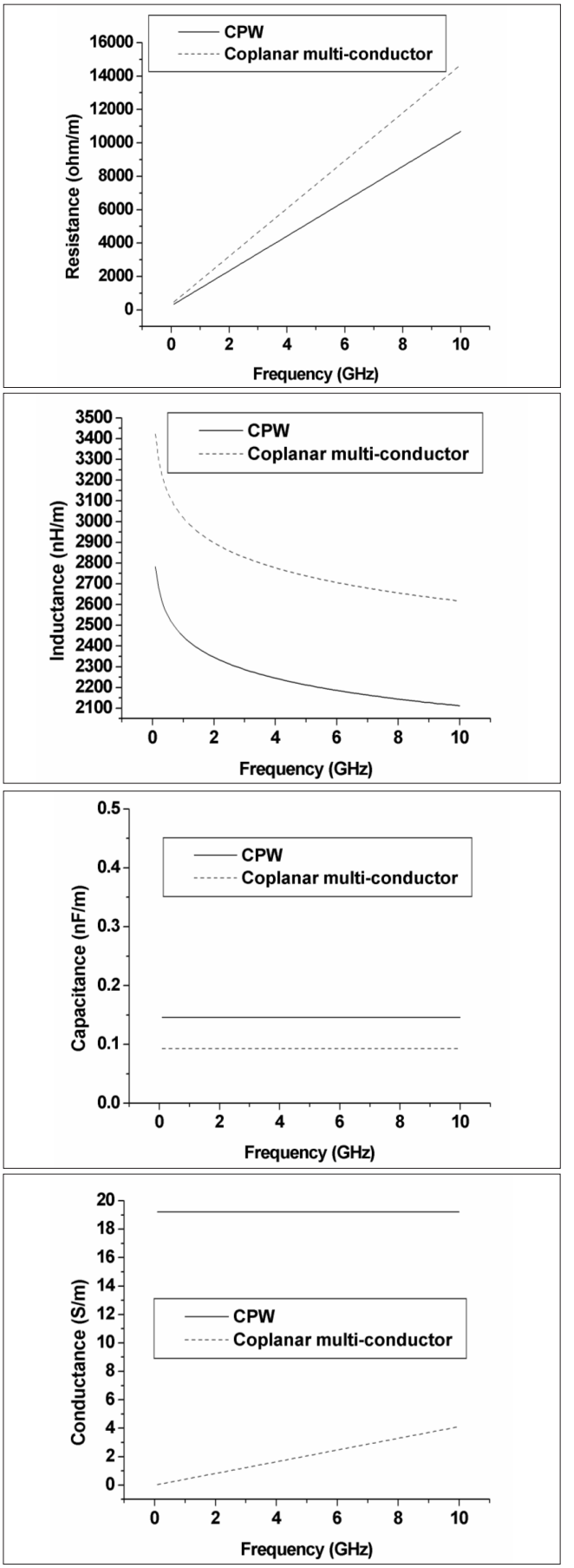

Fig. 9. RLGC parameter of CPW and coplanar multi-conductor.

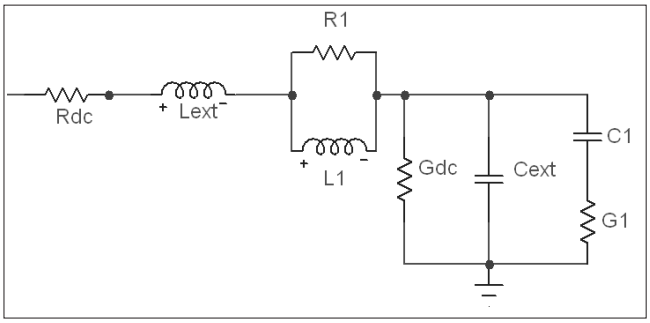

Fig. 10. Implementation of first order Debye approximation.

5. The top layer uses pitch_current as "pitch_above" and the bottom layer uses the pitch_current as "pitch_below."

A software program was developed in C++ language to build the on-chip power grid model automatically, which takes the following data as input: 1) size of the chip, 2) number of power grid layers, 3) permittivity of the SiO_2, 4) pitch, width, thickness, sheet resistance and conductivity of each power layer. The outputs of the program are a group of text files, which are either in the format of SPICE netlist or in a format readable by further parameter extraction tools, which will be discussed later.

Application of Complex Image Theory

A transmission line model with constant RLGC parameters is not suitable for high-speed applications. The intrinsic frequency dependency of on-chip power bus requires a convenient method for characterizing dispersion. Complex image theory [7] can be used for this problem by extending image theory to include the effect of conductive substrates. To take into account the loss due to eddy currents in the silicon substrate, the substrate is approximately replaced by a conducting image plane located at a complex distance h_{eff} from the metal.

The effective height h_{eff}, which is obtained by forcing the first two coefficients of Green's function to zero [8], is a function of frequency and substrate conductivity σ, given by

$$h_{eff} = h_{ox} + \frac{1-j}{2}\delta \tanh[(1+j)h_{Si}/\delta], \quad \delta = 1/\sqrt{\pi f \mu_0 \sigma} \tag{1}$$

Complex image theory has been applied to coplanar waveguide (CPW) over SiO_2-Si substrate as shown in Fig. 3. Instead of closed form parameters of coupled transmission lines, expressions of effective permittivity ε_{eff}, characteristic impedance Z_0 and propagation constant γ of conductor-backed CPW [9] are adopted to characterize the on-chip CPW. The analytical solutions can be derived from quasi-static approximation of transmission line (2), such as

$$\varepsilon_{eff} = \frac{C_{line}}{C_0}, \quad Z_0 = \frac{1}{cC_0\sqrt{\varepsilon_{eff}}}, \quad \gamma = j\varpi\sqrt{\mu_0\varepsilon_0\varepsilon_{eff}} \tag{2}$$

where c is the speed of light, C_{line} is the line capacitance of the transmission line, and C_0 is the line capacitance when no dielectric exists. In (2), ω, ε_0 and μ_0 denote angular frequency, air permittivity and air permeability. Parameters C_{line} and C_0 have to be found first in order to obtain the other parameters. The line capacitor of CPW is derived through two intermediate conformal mappings under the condition that two side ground wires are assumed to be infinitely wide and the dielectric is lossless. Therefore, the combination of (1) and (2) completes the CPW modeling by taking into account the geometry as well as substrate losses.

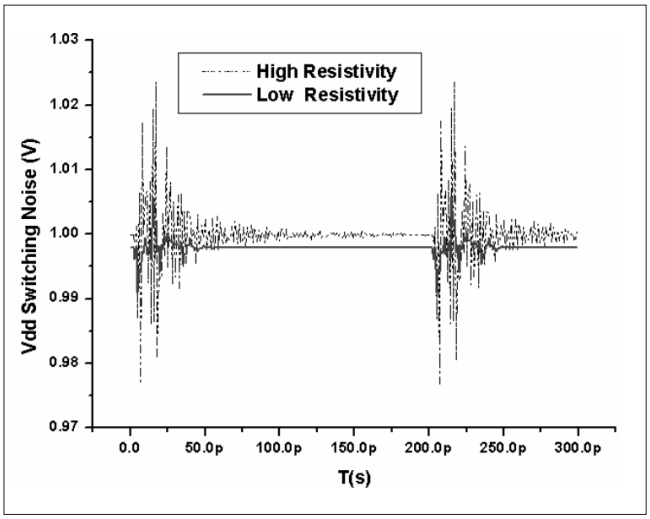

Fig. 11. Switching noise on wafers with different resistivity.

The numerical result shows good agreement with measurement from the Vector Network Analyzer for both CPW on wafers with high resistivity (2000 Ω-cm) and low resistivity (100 Ω-cm), as shown in Fig. 4. The parameters of CPW transmission line used are as follows: $W_{vdd} = 25\ \mu$m, $W_{gnd} = 300\ \mu$m, $h_{ox} = 1\ \mu$m and $h_{Si} = 500\ \mu$m.

Conformal Mapping for On-chip Power Distribution

The results in the previous section verify the accuracy of complex image theory for a CPW transmission line. However, the expressions of CPW cannot be directly used for on-chip power distribution, due to the periodicity of the structure. In this paper, the on-chip power distribution is called a coplanar multiconductor (CMC) structure, details of which are shown in Fig. 5. The common feature shared by CPW and CMC is that the neighboring buses assume opposite potentials. However, CMC has two distinct features, namely, 1) Its uniform topology causes a symmetric field around the center of each wire as shown in Fig. 5 and 2) The return current distribution is changed since ground wires have the same dimension as Vdd wires. Hence, the capacitor calculation is different from CPW, but the application of a conformal mapping technique can still be used.

Fig. 5 shows the electric field distribution for a CMC, obtained through electromagnetic simulations [9]. Based on the field distribution, enforcing magnetic-walls 1, 2 and 3 in Fig. 5 does not change the field distribution because there is no electric field normal to the line perpendicular to the center of each wire. The field confined by magnetic walls 1 and 2 con-

tributes to the line capacitor $C_{multi\text{-}conductor}$. It is efficient to calculate the electric field only on one side of the magnetic wall 3 to reduce the computational complexity since the electric field is symmetric about magnetic wall 3. Furthermore, as shown in Fig. 5, $C_{multi\text{-}conductor}$ is given by doubling the summation of $C_{up}(\varepsilon_{SiO_2})$ and $C_{down}(\varepsilon_{Si})$, which could be obtained through conformal mapping.

$C_{up}(\varepsilon_{SiO_2})$ is determined by using Schwarz-Christoffel mapping derived in (3) and shown in Fig. 6.

$$T = \int_{0}^{M} \frac{dt}{\sqrt{t^2 - a^2}}, \quad C_{up}(\varepsilon_{SiO_2}) = \frac{\varepsilon_0 \varepsilon_{SiO_2} W}{d}$$
$$W = \int_{-b}^{-a} \frac{dt}{\sqrt{t^2 - a^2}}, \quad d = \frac{1}{j}\int_{-a}^{a} \frac{dt}{\sqrt{t^2 - a^2}} \tag{3}$$

Capacitor $C_{down}(\varepsilon_{Si})$ is obtained by going through two successive Schwarz-Christoffel mappings derived in (4) and shown in Fig. 7.

$$Z = \frac{b}{k}\int_{0}^{M} \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}},$$
$$T = \int_{}^{M} \frac{dt}{\sqrt{(t+1/k)(t+1)(t^2-x^2)}}$$
$$\frac{K}{K'} = \frac{b}{h} \quad K = \int_{0}^{1} \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}} x = sn\left(\frac{aK}{b}, k\right)$$
$$C_{Down}(\varepsilon_{Si}) = \frac{\varepsilon_0 \varepsilon_{Si}(W + W_1 + W_2)}{2d} \tag{4}$$
$$W = \int_{-1}^{-x} \frac{dt}{\sqrt{(t+1/k)(t+1)(t^2-x^2)}}$$
$$W_1 = \int_{x}^{1} \frac{dt}{\sqrt{(t+1/k)(t+1)(t^2-x^2)}}$$
$$W_2 = \int_{-1}^{-x} \frac{dt}{\sqrt{(t+1/k)(t+1)(t^2-x^2)}}$$
$$d = \frac{1}{j}\int_{-x}^{x} \frac{dt}{\sqrt{(t+1/k)(t+1)(t^2-x^2)}}$$

where sn is the Jacobi elliptic function.

Since the loss of a power grid contributes to the attenuation of on-chip switching noise, the effect of SiO_2 thickness on silicon loss has been studied by observing the conductance G as a function of oxide thickness h_{ox} in equation (5). As the thickness of SiO_2 increases, the substrate loss G decreases as shown in Fig. 8.

$$G = 4\pi^2 f^2 \sigma_{Si} \varepsilon_{Si}^2 \varepsilon_{SiO_2}^3 w^3 C_\infty \Bigg/ \left(\varepsilon_0 h_{ox}^3 \left(\frac{\varepsilon_{Si}\varepsilon_{SiO_2} w}{h_{ox}} - C_\infty \right) \right.$$
$$\left(\frac{\sigma_{Si}^2 \varepsilon_{SiO_2}^2 w^2 C_\infty^2}{\varepsilon_0^2 h_{ox}^2 \left(\frac{\varepsilon_{Si}\varepsilon_{SiO_2} w}{h_{ox}} - C_\infty \right)^2} + 4\pi^2 f^2 \left(\frac{\varepsilon_{Si}\varepsilon_{SiO_2} w C_\infty}{h_{ox}\left(\frac{\varepsilon_{Si}\varepsilon_{SiO_2} w}{h_{ox}} - C_\infty \right)} \right.\right.$$
$$\left.\left. + \frac{\varepsilon_{Si}\varepsilon_{SiO_2} w}{h_{ox}} \right)^2 \right) \Bigg) \tag{5}$$

where f is frequency; $\varepsilon_0, \varepsilon_{Si}, \varepsilon_{SiO_2}$ is the permittivity of air, silicon and SiO_2, respectively; σ_{Si} is silicon conductivity; w is the width of interconnect, and C_∞ is the capacitance defined in [8]. The conductance of a test case with $w = 4\ \mu$m, $h_{Si} = 500\ \mu$m [8] and frequency at 5 GHz is shown in Fig. 8.

The differences of the RLGC parameter of a CPW and CMC with the same geometry, namely $w = 25\ \mu$m, $h_{ox} = 1\ \mu$m, $h_{Si} = 500\ \mu$m as defined in Fig. 3, except the width of Vdd, is shown in Fig. 9.

Frequency Dependence Approximation

On-chip power grid analysis is difficult because the electrical models that represent the grid can be very large, easily reaching up to millions of components and nodes. Hence, SPICE [4] can be computationally expensive due to time and memory constraints. Finite Difference Time Domain (FDTD) has been used for circuit simulation [3], in which current value is updated over all branches of the power grid and then voltage is updated over all nodes at each time step. Computations of branch currents and node voltages are alternated as time progresses.

The frequency dependent RLGC parameters of each segment of the power grid demand a more accurate model than a simple representation, which only has R_{dc}, G_{dc} (DC resistance and conductance) L_{ext} and C_{ext} (low frequency inductance and capacitance). Instead, N serially connected first-order Debye terms [10] could be used to approximate both serial impedance Z (6) and shunt admittance Y (7). During the approximation, the number of poles N must be chosen and then the corresponding R_i, L_i, G_i and C_i can be determined by an optimization procedure. Numerical experiments show that a good match is obtained using no more than three or four Debye terms. Debye rational approximation for $N = 1$ is used for frequency dependent power grid simulation as shown in Fig. 10. Computational efficiency of FDTD is maintained since it only takes a slight modification in the algorithm to include the first-order Debye circuit model as shown in equations (8) and (9).

$$Z = R_{dc} + j\varpi L_{ext} + j\varpi \sum_{i=1}^{N} \frac{L_i}{1 + j\varpi L_i / R_i} \tag{6}$$

$$Y = G_{dc} + j\varpi C_{ext} + j\varpi \sum_{i=1}^{N} \frac{C_i}{1 + j\varpi C_i / G_i} \quad (7)$$

$$\frac{\partial V(\varpi, z)}{\partial z} = -j\varpi L_{ext} B,$$
$$B = \left(\frac{R_{dc}}{j\varpi L_{ext}} + \frac{L_1}{L_{ex}} + \frac{1}{1 + j\varpi L_1 / R_1} + 1 \right) I \quad (8)$$

$$\frac{\partial I(\varpi, z)}{\partial z} = -j\varpi C_{ext} D,$$
$$D = \left(\frac{G_{dc}}{j\varpi C_{ext}} + \frac{C_1}{C_{ext}} + \frac{1}{1 + j\varpi C_1 / G_1} + 1 \right) V \quad (9)$$

Full Chip Power Grid Simulation

The substrate impacts the power distribution network in two ways. First, the substrate reduces the distribution network's DC voltage drop. Second, the voltage swing is reduced due to the conductance and the decoupling effect of a parasitic capacitor between power buses and substrate. Consequently, a power distribution analysis without the substrate effect can lead to an over-designed distribution network and result in wasting chip resources. The effect of substrate resistivity on SSN is demonstrated through a simple test vehicle, which is a 4 mm × 4 mm chip with a three-layer power supply and the pitches of each layer are 20 μm, 40 μm, and 80 μm. The width of the power bus is 5 μm and the thickness is 1 μm. Switching current is modeled as a triangular current pulse with 10 ps rise time and 20 ps fall time. The supply voltage is 1 v and the power density at the center of the chip is 300 mw/(mm^2). Two simulations are done for the chip with the same physical setup but different substrates, namely, high resistivity with $\rho = 100\,\Omega$-cm and low resistivity with $\rho = 5\,\Omega$-cm. The voltage of a node 1mm away from the chip center at the bottom layer is recorded. The waveforms of both are compared in Fig. 11. It can be clearly seen that lossy substrate helps attenuate the on-chip simultaneous switching noise by reducing the peak-to-peak value and accelerating the damping of the voltage swing.

Conclusion

The closed-form expression of an RLGC parameter for on-chip power distribution network and FDTD implementation for frequency dependent interconnects has been presented. The effect of substrate loss on switching noise in an on-chip power distribution network has been quantified through full-chip simulation. The proposed approach can easily be incorporated into chip and system power integrity design.

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Biographies

Jifeng Mao *received his B.S degree in electrical engineering from Shanghai Jiao Tong University and M.S. degree in electrical and computer engineering from Georgia Institute of Technology where he is currently pursuing the Ph.D degree in electrical and computer engineering. His work has been focused on modeling and characterizing interconnects, power distribution networks for high frequency integrated circuits and packages. He is the recipient of the Shri. Mukhopadhyay best paper award at the International Conference on Electromagnetic Interference and Compatibility in 2003.*

Madhavan Swaminathan *received the M.S. and Ph.D. degrees in Electrical Engineering from Syracuse University. He is currently a Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology (Georgia Tech), Atlanta, and the Deputy Director of the Packaging Research Center (PRC), Georgia Tech. He is the cofounder of Jacket Micro Devices, a company specializing in integrated passive devices for RF applications where he serves as the Chief Scientist. Prior to joining Georgia Tech, he was with the Advanced Packaging Laboratory, IBM, working on packaging for super computers. While at IBM, he reached the second invention plateau. He has more than 150 publications in refereed journals and conferences, has co-authored three*

book chapters, has nine issued patents and has nine patents pending. His research interests are in digital, RF, optoelectronics and mixed-signal packaging with emphasis on design, modeling, characterization, and test. Dr. Swaminathan is the recipient of the 2002 Outstanding Graduate Research Advisor Award from the School of Electrical and Computer Engineering, Georgia Tech and the 2003 Outstanding Faculty Leadership Award for the advisement of GRAs from Georgia Tech. He is also the recipient of the 2003 Presidential Special Recognition Award from the IEEE CPMT Society for his leadership of TC-12. He has also served as the coauthor for a number of outstanding student paper awards at EPEP '00, EPEP '02, EPEP '03, ECTC '98 and the 1997 IMAPS Education Award. He is the recipient of the Shri Mukhopadhyay best paper award presented at the International Conference on Electromagnetic Interference and Compatibility in 2003. He served as the Co-Chair for the 1998 and 1999 IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), as the Technical and General Chair for the IMAPS Next Generation IC & Package Design Workshop, and as the Co-Chair for the 2001 IEEE Future Directions in IC and Package Design Workshop. He serves as the Chair of TC-12, the Technical Committee on Electrical Design, Modeling, and Simulation within the IEEE CPMT society. He is the cofounder of the IMAPS Next Generation IC & Package Design Workshop and the IEEE Future Directions in IC and Package Design Workshop. He also serves on the technical program committees of EPEP, Signal Propagation on Interconnects workshop, Solid State Devices and Materials Conference (SSDM), Electronic Components and Technology Conference (ECTC), and Interpack. He has been a Guest Editor for the IEEE Transactions on Advanced Packaging and IEEE Transactions on Microwave Theory and Techniques. He was the Associate Editor of the IEEE Transactions on Components and Packaging Technologies.

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"News Flash"

The EMCS Moves to Full Paper Submission for Consideration in EMCS Symposia

By Elya B. Joffe, Vice-President for Conferences and Symposia

Introduction

The EMCS BoD approved at its November 2003 meeting a policy requiring that papers submitted for consideration for the IEEE Symposia on EMC will be submitted in the form of a "Preliminary Manuscript," similar in content and format to the final paper.

Additions and changes (such as inclusion of final analysis and test results) will be allowed in the final "camera ready" paper, however, those changes will not be allowed to significantly amend or change the scope and/or significance of the paper.

The new policy will be effective as of the 2005 IEEE International Symposium on EMC in Chicago.

Background

Submission of papers for consideration for the IEEE International Symposia on EMC is currently done by submission of an "Abstract" (50-100 words) and a "Summary" (1000 words). It has been repeatedly shown that submissions received in that form can often be improperly considered for acceptance or rejection, both from the technical point of view as well as from the commercialism point of view.

Recognizing this, several global symposia, for example, consider only full paper submission. In addition, the 2003 IEEE International Symposium in Istanbul also required full paper submission, in the form of a "Preliminary Manuscript".

We believe that the fact that a full paper is submitted will significantly improve the quality of papers accepted at our IEEE EMC symposia, as well as shorten the time required for the "camera ready" submission, thus allowing for a later preliminary submission and a longer review time. **EMC**