Practical Papers, Articles and Application Notes

Robert G. Olsen, Technical Editor

In this issue you will find two practical papers that should be of interest to members of the EMC community. The first is entitled "PDN Design Strategies: III. Planes and Materials – Are They Important Factors in Power Bus Design? by James L. Knighten, Bruce Archambeault, Jun Fan, Giuseppe Selli, Liang Xue, Samuel Connor, and James L. Drewniak." This is the third in a series of papers they are writing. If you enjoyed the first two (and I suspect that you did), you will enjoy this one. The second paper is entitled, "Photonic Crystal Power Substrate for Wideband Suppression of Power/Ground Bounce Noise and Radiated Emission in High-speed Packages" by Sin-Ting Chen, Tzyy-Sheng Horng and Tzong-Lin Wu. In this paper the authors discuss a new substrate material for suppressing the ground bounce noise and radiated emissions from high speed digital package substrates. It complements the work presented in this section by the authors of the first paper. This paper was first presented at the Asia Pacific Symposium on EMC, APEMC'2005, which took place in Taipei, Taiwan, in December, 2005 and was selected as the "Best Symposium Paper." It has been reprinted here by permission of the Symposium Committee.

The purpose of this section is to disseminate practical information to the EMC community. In some cases the material is entirely original. In others, the material is not new but has been made either more understandable or accessible to the community. In others, the material has been previously presented at a conference but has been deemed especially worthy of wider dissemination. Readers wishing to share such information with colleagues in the EMC community are encouraged to submit papers or application notes for this section of the Newsletter. See page 3 for my e-mail, FAX and real mail address. While all material will be reviewed prior to acceptance, the criteria are different from those of Transactions papers. Specifically, while it is not necessary that the paper be archival, it is necessary that the paper be useful and of interest to readers of the Newsletter.

Comments from readers concerning these papers are welcome, either as a letter (or e-mail) to the Technical Editor or directly to the authors.

PDN Design Strategies: III. Planes and Materials – Are They Important Factors in Power Bus Design?

James L. Knighten[1], Bruce Archambeault[2], Jun Fan[1], Giuseppe Selli[3], Liang Xue[3], Samuel Connor[2], and James L. Drewniak[3]

I. INTRODUCTION

This is the third in a series of papers on design strategies for effectively decoupling dc power distribution networks (PDN) on digital printed circuit boards (PCB). The first paper examined means for choosing the appropriate values of high-frequency decoupling capacitors when designing multi-layered PCBs intended for digital circuits with medium-to-high-speed switching [1]. The second paper examined the importance of the location of the decoupling capacitor on the PDN [2].

This paper examines the properties of parallel-planar structures formed by planes in the PDN, some important properties of the dielectric materials used to separate the planes of a power bus, and the significance of these to high-frequency decoupling. Planes, plane pair and plane fills are routinely used in PCBs intended for use with high-speed digital electronics. They are also used in PCBs in lower speed applications. Planes offer numerous advantages to the electrical performance of the PCB versus the PCB that does not contain planes.

Planes provide the opportunity for superior decoupling performance in high-speed digital applications. They are used for both supplying dc voltage levels to circuits (power) and dc current return (power return). They support timely charge delivery during the initial switching periods of digital integrated circuits (IC). The rapidity of charge delivery is partially a result of the low inductance circuit path afforded the charge stored in the planar structure (parallel-plate capacitor) as compared to the higher inductances usually associated with discrete decoupling capacitors and their interconnection means. Easy charge availability during early periods of the IC's switching of states is advantageous to an IC's proper functional operation in meeting its need to either acquire or disgorge charge. The early time charge availability also supports maintaining limits on the ac ripple voltage on the dc voltage on the planes.

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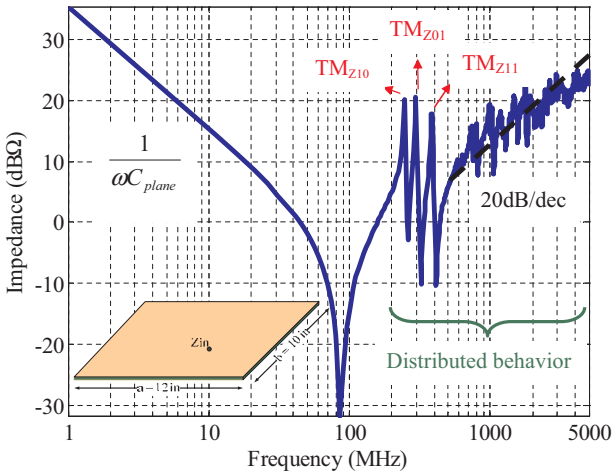

Figure 1: Input impedance of a parallel plate configuration with the pair of planes separated by 40 mils. The -20 dB/dec initial slope corresponds to the capacitance of the board. The dip at 100 MHz corresponds to the resonance of the interplane capacitance and the inductance of the input port. Above 100 MHz, the distributed behavior determines the impedance, but the trend at high frequencies is +20 dB/dec, corresponding to the inductance of the input port.

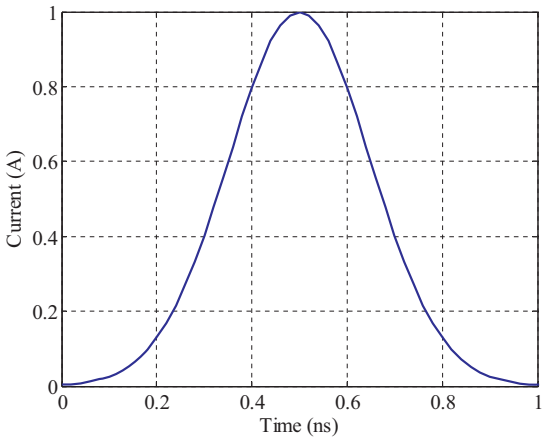

Figure 3: A current pulse at Port 1 of 1 ns pulse width, a time to peak of 0.5 ns, and peak amplitude 1A is applied to Port 1 to simulate current draw from an IC switching states at Port 1.

Planes within the PCB stack-up can be advantageous in terms of the fidelity of the digital signal. Planes can provide lower impedance paths for return currents associated with signal traces than is usually seen with discrete return current traces. These more efficient return current paths usually benefit the fidelity of the waveshape of a digital signal. While not explicitly covered in this paper, note that, in PCB structures with multiple layers and multiple planes, care may be needed during design to provide capacitive coupling (decoupling) between planes that are not members of the same power bus in order to facilitate a low impedance path for signal return currents. This is primarily true for signal traces that traverse multiple layers on the PCB. Examples of potential ill effects of this are shown in [3].

The use of planes may also be advantageous in terms of reducing or containing electromagnetic interference (EMI) radiated emissions from a PCB, as opposed to may have been experienced with no planes. A detailed examination of this is beyond the scope of this discussion.

Planes may be advantageous to efficient PCB design in that they may facilitate an increase in component density, i.e., routing density. Power or ground connections can be obtained at virtually any location on the PCB using a via, rather than using routing space for power or ground traces. In summary, the benefits of planes is so strong that the PCB with multiple layers, some for signal traces and some layers containing planes for power or for ground (power return and signal return) is the paradigm of the PCB for high-speed digital applications.

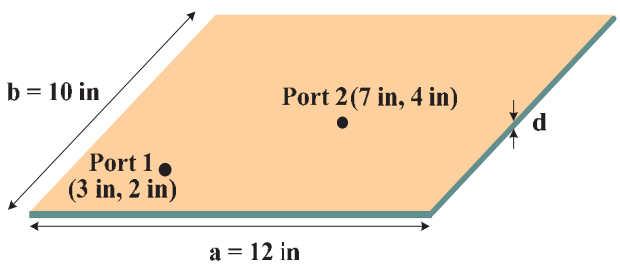

Figure 2: PCB configuration used for all simulations in this paper.

II. CHARACTERISTICS OF THE SINGLE PLANE PAIR

The goals of decoupling on a PCB are two-fold. First, it is desired to achieve a power bus impedance that remains low over a wide range of frequencies. This assures that the noise voltages that are created by inevitable noise currents remain small. Secondly, it is desired to provide adequate charge in a timely manner to ICs that are switching states. This assures orderly functional operation. The first of these criteria is more naturally described in the frequency domain and the second in the time domain. Hence, as the properties of planar power bus structures are examined in this paper, both frequency and time

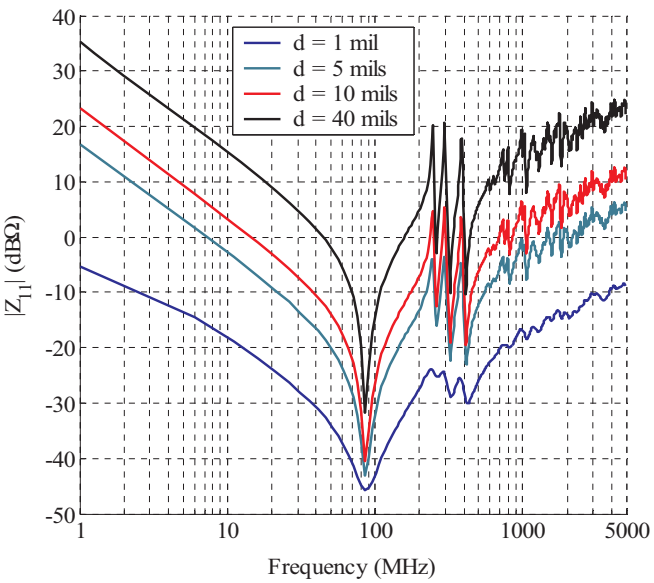

Figure 4: $|Z_{11}|$ of the power bus configuration in Figure 2 for the case of various values of plane spacing, showing the lowering of impedance as the planes become closer (ε_r = 4.0).

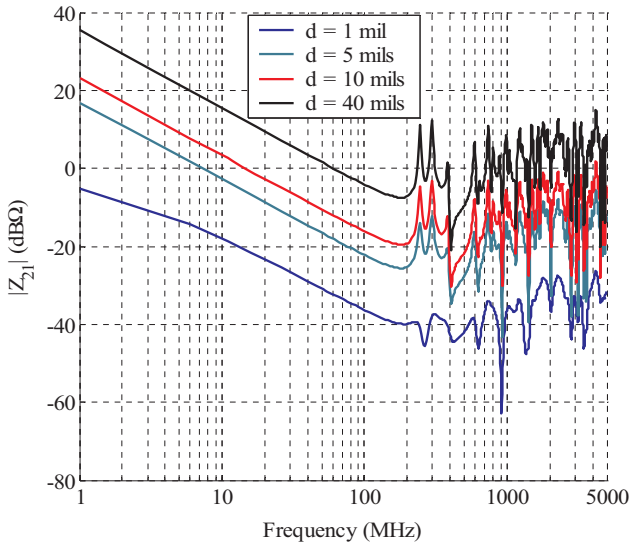

Figure 5: $|Z_{21}|$ of the power bus configuration in Figure 2 for the case of various values of plane spacing, (ε_r = 4.0).

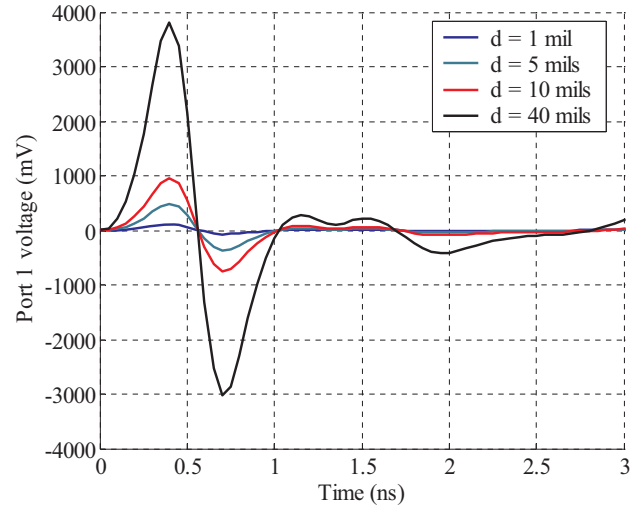

Figure 7: Port 1 voltage vs. time for various values of plane spacing, d, showing a lowering of peak voltage as the planes become closer. Fixed parameters are identical to those in Figures 4 and 5.

domain characterizations are examined to facilitate clarity.

A pair of planes in a PCB stack-up naturally forms a parallel-plate capacitor, often called an inter-plane capacitor. The value of this inter-plane capacitance can be estimated by (neglecting fringing and other effects):

$$C_{Plane} = \frac{\epsilon S}{d}, \qquad (1)$$

where *S* is the plane area, *d* is the spacing between power and ground planes, and ε is the permittivity of the dielectric layer between the power and ground planes. At low frequencies, charge stored in the planes is proportional to the value of the capacitance. The larger the capacitance, the more charge stored and available to support logic transitions. At the same time, the impedance of the plane pair is inversely proportional to the capacitance value. Therefore, in order to maintain low impedance over a frequency range, a larger capacitance value is desirable. This implies that small values of *d* or large values of ϵ, are desirable.

However, the power/ground plane parallel-plate structure can be modeled accurately as the inter-plane capacitance described in (1) only at low frequencies. Low frequencies are defined as frequencies well below the frequencies where the resonances of the planar structure are manifested. At low frequencies, the wavelength is long compared to PCB dimensions and the displacement current in the dielectric material is nearly uniform over the plane surface, *S*, except near the PCB edges. Figure 1 shows the input impedance of a parallel-plate cavity corresponding to a PCB power bus. From Figure 1, the frequencies

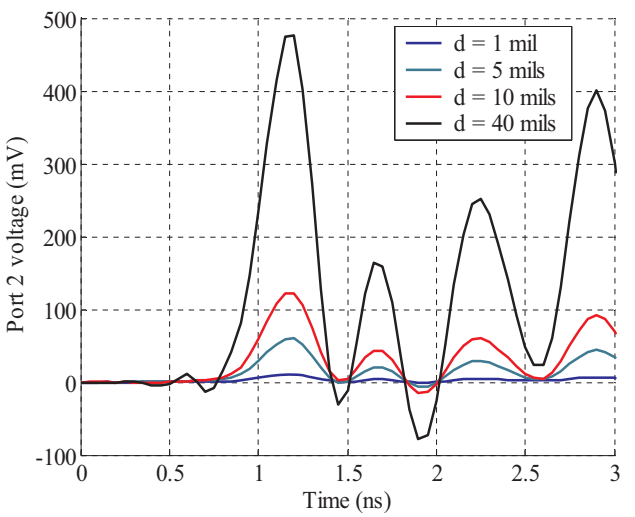

Figure 6: Port 2 voltage vs. time for various values of plane spacing, d, showing a lowering of peak voltage as the planes become closer. Fixed parameters are identical to those in Figures 4 and 5.

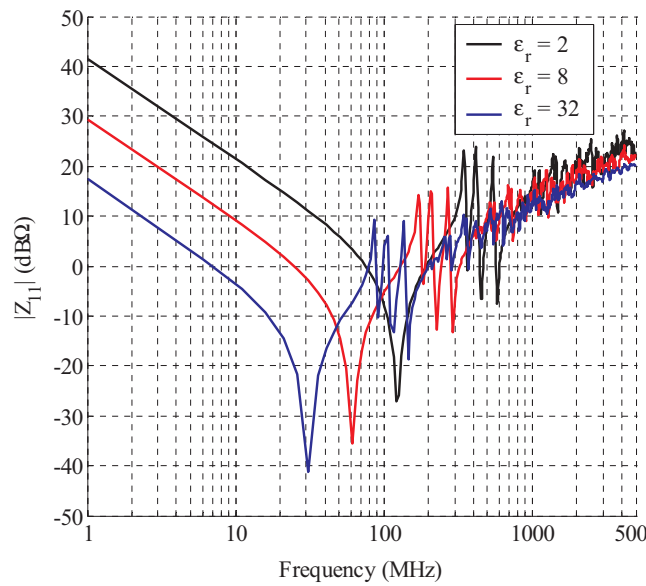

Figure 8: $|Z_{11}|$ for the power bus configuration seen in Figure 2 for the case of various values of dielectric constant, showing shifts in frequency and magnitude in the impedance profile, lowering the resonant frequencies as permittivity increases (d = 40 mils).

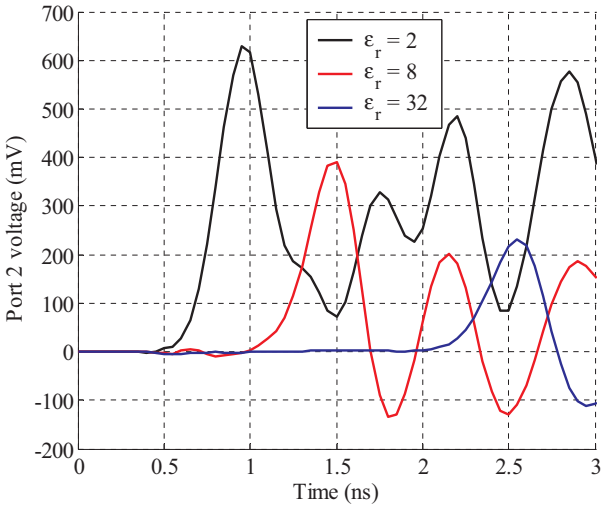

Figure 9: Port 2 voltage vs. time for various values of dielectric constant, showing lower peak voltage for higher dielectric constant values, but shifted in time, corresponding to different velocities of propagation. Fixed parameters are identical to those in Figure 8.

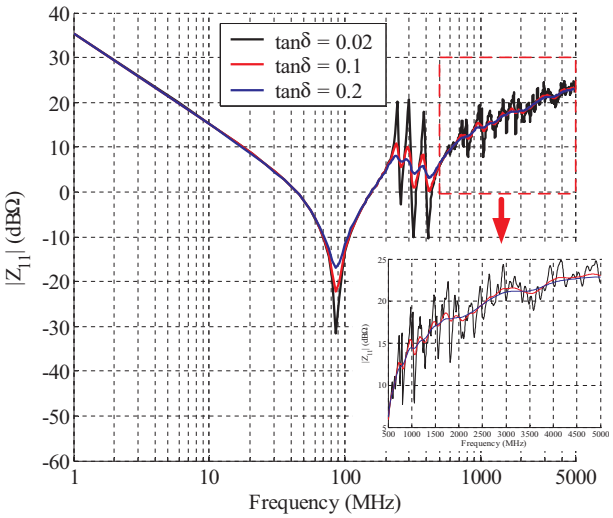

Figure 11: $|Z_{11}|$ for the power bus configuration seen in Figure 2 for the case of various values of loss tangent, showing the lowering of resonant peaks as loss increase (ε_r = 4.0, d = 40 mils).

where the inter-plane impedance behaves as a simple lumped capacitor lie below 100 MHz, where the lowest frequency resonance occurs.

The resonance observed near 100 MHz in Figure 1 is a resonance due to the combination of the lumped inter-plane capacitance and the inductance of the feeding Port 1 (The port inductance emulates inductances of the via and pad interconnection of a decoupling capacitor that are associated with a capacitor mounted on a PCB. The mounted decoupling capacitor will exhibit a resonance similar to the 100 MHz resonance seen in Figure 1.). At higher frequencies, the inductive behavior associated with the port is superimposed with the distributed resonances of the plane pair and impedance generally rises with frequency with resonant peaks and valleys superimposed.

The parallel-plate structure may also be viewed as a parallel-plate cavity. When the frequency rises to values where standing waves are established between the planes, the power/ground pair exhibits resonances and the magnitude of the plane input and transfer impedances demonstrate peaks and valleys (poles and zeros) in an alternating pattern. These impedances can attain high values at the frequencies corresponding to the resonant peaks, which are related to the board physical dimensions and dielectric constant as

$$f_{RES(mn)} = \frac{1}{2\pi\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \qquad (2)$$

where a and b are the largest and smallest dimensions of the rectangular parallel-plates, respectively. ε and μ are the dielectric constant and permittivity of the dielectric material, respectively.

From Figure 1, when frequencies are higher than that of the lowest resonant frequency, an inductive impedance rise with fre-

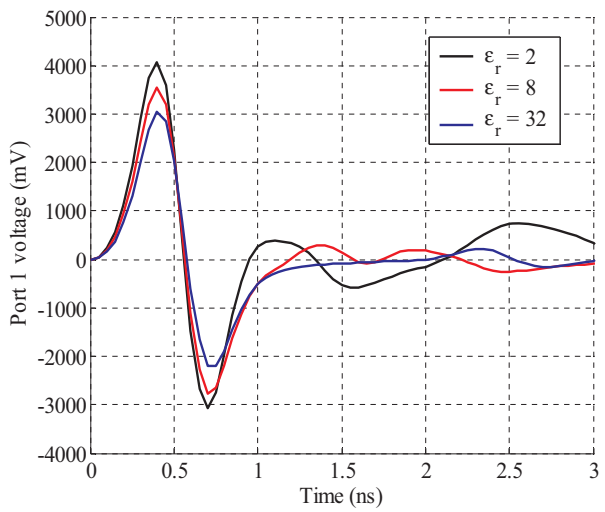

Figure 10: Port 1 voltage vs. time for various values of dielectric constant, showing lower peak voltage for higher dielectric constant values, but with no shifts in time. Fixed parameters are identical to those in Figure 8.

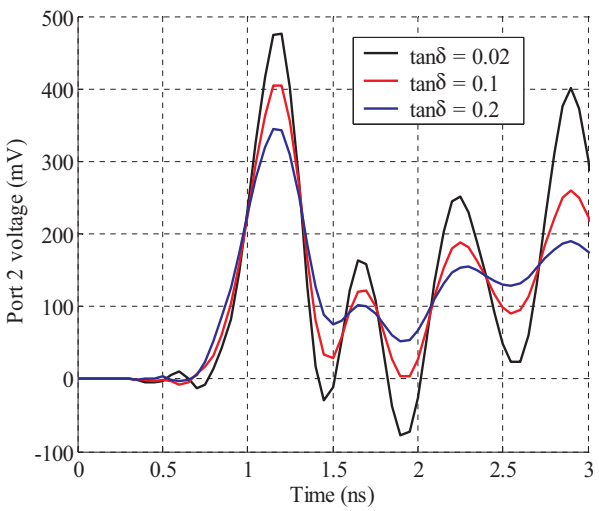

Figure 12: Port 2 voltage vs. time for various values of loss tangent, showing a lowering of peak voltage as dielectric loss increases (εr = 4.0, d = 40 mils).

quency is superimposed with the distributed resonances described in (2). The modes associated with those resonances are TM_z, i.e., transverse magnetic [4]. The impedance profile shown in Figure 1 corresponds to that of a parallel plate configuration of 1 mm thickness of FR-4 dielectric material (ε_r = 4.0) and dimensions of a = 12 in. and b = 10 in.

Analyses of planar power bus structures in this paper are accomplished by means of a cavity analysis [5, 6, 7, 8]. The cavity model formulation is suitable for the analysis of the power delivery network (PDN) of printed circuit boards (PCB). A cavity model analysis software implementation based on first principles Maxwell's Equations was developed along with the ability to extract SPICE models from the simulation [9, 10]. This was used in previous papers in this series and was again used in all simulations herein. The driving point impedance at a port i, and the transfer impedance between two ports i and j can be expressed from this formulation as

$$Z_{ij}(\omega) = \frac{d}{ab\varepsilon}\sum_{n=0}^{N}\sum_{m=0}^{M}\frac{N_{mn}(x_i,y_i)\,N_{mn}(x_j,y_j)}{\frac{\omega_{mn}^2}{j\omega}+j\omega+\omega_{mn}\left(\tan\delta+\frac{\delta_S(\omega_{mn})}{d}\right)}+ \\ +j\omega\mu\frac{d}{ab}X_0(x_i,\,y_i,\,x_j,\,y_j) \qquad (3)$$

While (3) appears formidable, a comprehensive understanding of it is not necessary to study the effects of planes and materials on decoupling. Nevertheless, it is valuable to review the equation as the effects of certain design methods are studied. The results shown in the next section will be clear by inspecting the various terms in (3). The $N_{mn}(x,y)$ terms in (3) describe the wave physics associated with the cavity geometry. The term in the double summation are the propagating modes in the cavity, and have modal resonant frequencies that are given by (2). The second term $j\omega\mu$ (d/ab)X_0, describes the evanescent modes around the ports, and is associated with the port inductance. The multiplicative constant before the summation is exactly the inverse of the plane static capacitance

$$C_{\text{Plane}} = \frac{ab\varepsilon}{d}\,, \qquad (4)$$

where a and b are the plane dimensions and d is the plane separation. The impedance seen looking into the board at different points or between different points is different as a result of the wave nature of the behavior of the power planes at high frequency. As frequency increases, the self-impedance of a port, e.g., Z_{11}, is dominated by the second term $j\omega\mu$ (d/ab)X_0, so that the impedance looking into the input port is inductive at high frequencies, and increases at 20 dB/decade as might be expected. The term

$$\left(\tan\delta+\frac{\delta_S(\omega_{mn})}{d}\right)$$

accounts for the dielectric and skin-effect conductor losses, where tanδ is the loss tangent of the material, δ_S is the skin depth at frequency ω_{mn}, and d is the layer spacing. As the spacing d gets small, typically 2 mils or less, the conductive losses of the planes dominate and damp out the plane resonances as shown in the results.

There are three common design techniques that may aid in the achievement of a reduction of power bus impedance and the prompt availability of charge. They are:

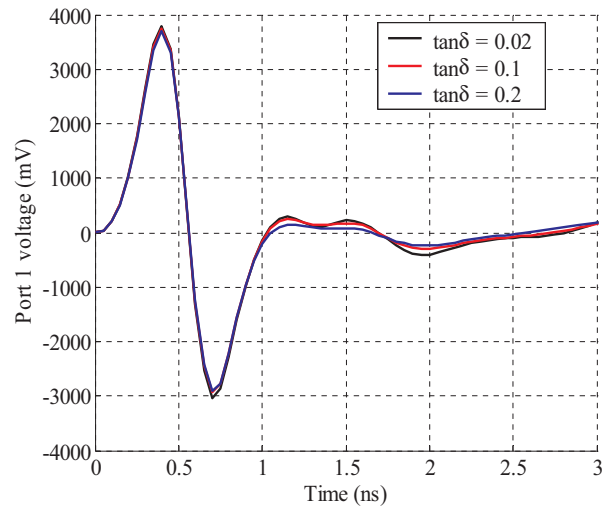

Figure 13: Port 1 voltage vs. time for various values of loss tangent (ε_r = 4.0, d = 40 mils).

- Reducing of plane spacing, d, of the planes of the power bus.
- Increasing dielectric constant of the material between the power bus planes.
- Increasing dielectric loss of the material between the power bus planes.

As will be shown later in detail, decreasing the spacing between the planes increases the inter-plane capacitance and lowers impedance, as seen in (3), and does not have the side effect of lowering resonant frequencies. Increasing the dielectric constant material between the power/ground planes decreases power bus impedance, as shown in (3), but not uniformly over a wide frequency range, since dielectric constant does not appear in all terms in Equation (3). Increasing dielectric loss in the power bus material does not affect the inter-plane capacitance nor the location of resonant peaks in the impedance, but it can have the beneficial effect of damping resonances (lowering the

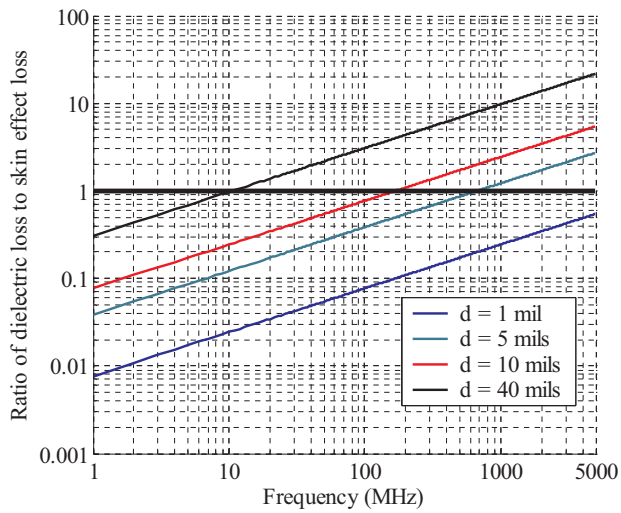

Figure 14: The balance between dielectric and skin effect losses vs. frequency shows that closely spaced planes are biased toward more conduction loss, whereas, plane pair that are more widely separated experience more dielectric loss (ε_r = 4.5, loss tangent = 0.02, and plane conductivity = 5.8 x10^{+7}).

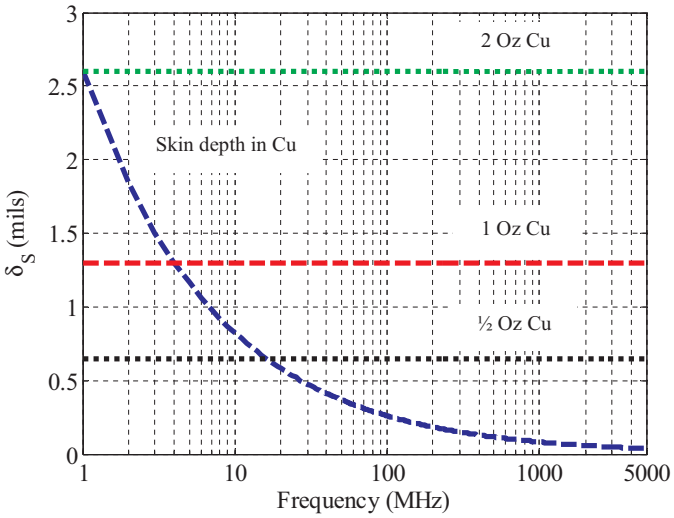

Figure 15: Copper skin depth vs. frequency and the thicknesses of copper foils.

impedance peaks) at frequencies higher than the lowest frequency i.e., lumped resonance. This method is not commonly used today in industry. These design techniques are based on PCB designer experience, particularly with decoupling for high-speed digital applications. In addition to the experience base, the use of these techniques is consistent with the description of the power bus physics described in Equation (3).

It is worth noting that in some design environments the flexibility to alter PCB design (stack-up, materials, etc.) to improve decoupling may be limited. Designs may be dictated by other constraints such as materials costs, board yields, etc. For instance, cost constraints may dictate the use of inexpensive, readily available dielectric material (FR-4 fiber glass epoxy resin), which will have a relative dielectric constant, ε_r, which has a value approximately 4. The PCB stack-up may be dictated by the number of layers needed for routing, or by cost constraints that limit the number of layers. Materials with high dielectric constants may be shunned because of the lack of manufacturing experience. However, even when facing rigid design constraints, opportunities to experiment and demonstrate ways to enhance future designs can present themselves, perhaps through test boards.

In order to examine the benefits of each these three power bus design techniques, a standard power bus structure, Figure 2, is used as a simulation model to compare the characteristics of each of these three design techniques. The power bus consists of two parallel conducting planes separated by a distance, d. The region between the planes is filled with a dielectric material with a relative dielectric constant, ε_r and a loss tangent, tan δ. Two ports are defined on the power bus. Port 1 serves as the driven port, where the current is defined as a Gaussian pulse of duration of 1 ns, peak magnitude of 1A, and a time to peak of 0.5 ns, as seen in Figure 3. The voltage between the planes is evaluated at Port 1 and 2. The driving point impedance, Z_{11} at Port 1 indicates the ratio of the voltage and current driven at Port 1. The transfer impedance, Z_{21}, indicates the ratio of the voltage at Port 2 to the current at Port 1. (Impedance parameters have Port 2 open circuited.) The voltage measured at Port 1 is an indication of the voltage disturbance caused by the current pulse disturbance at the location of the current disturbance, i.e., a self-induced noise voltage. The voltage at Port 2 is the voltage disturbance transmitted to Port 2 by the current disturbance at Port 1.

For simplicity, previous papers in this series used an isosceles triangular waveform to simulate the current draw at Port 1 caused by a switching IC [2]. In this paper, however, a Gaussian waveform is chosen in order to avoid the sharp changes in inflection of the triangular current's time profile, and the exaggerated effects these sharp corners can have on the spectrum. The Gaussian waveform is more consistent with the current waveform of the switching IC and produces voltage waveforms that have a more realistic appearance than does the triangle.

The first design technique investigated for reducing power bus impedance and voltage ripple magnitude is the reduction of plane spacing, d. Figures 4 and 5 show the effects on driving point and transfer impedances, $|Z_{11}|$ and $|Z_{21}|$, of holding dielectric constant and loss tangent fixed in the structure from Figure 2, and varying the plane spacing, d. Parameters for the simulations that produced these figures are: dielectric constant of the power bus material is 4.0, plane conductivity is that of copper, 5.8 x10^{+7} S/m, and the loss tangent of the dielectric material is 0.02 (a value typical of common PCB laminate materials used in high-speed designs). From (3), the impedance is directly proportional to the plane spacing, d, so a reduction in plane spacing will reduce power bus impedance over a wide frequency range. This is clearly visible in Figures 4 and 5. In addition, there are no shifts in resonant frequencies as the plane spacing is varied, hence, no dramatic changes in the spectral behavior of the structure. The Q of the impedance curve (easily seen in Figure 4) increases as plane spacing increases indicating changes in the relative loss characteristics of the planar structure with respect to total energy stored. Very thin plane spacings do not support strong resonant peaks in the impedance, either self or transfer impedance, hence, provide a good platform for effective decoupling. A later discussion will show that as plane spacing decreases, copper losses in the planes increase. For very small (thin) plane spacings, increased copper loss is the dominant reason that strong resonant peaks are not supported.

Figure 6 illustrates the early time waveform of the voltage at Port 2 for each of the selected plane spacings, d. These voltages are indicative of the disturbance caused at Port 2 by the current pulse at Port 1; hence, Port 2 is a victim port for a disturbance at Port 1. There is an evident time lag in the Port 2 voltage, indicating the time necessary for the disturbance at Port 1 to reach Port 2. The peaks in the voltage waveform are aligned in time, regardless of the plane spacing. This lack of a shift in time indicates that the spectral character of the voltage at Port 2 is not affected by changes in plane spacing, i.e., the resonant frequencies are unchanged. For the largest plane spacing examined (d = 40 mils), the peak amplitude of the voltage is the largest seen for any of the smaller plane spacing values. As the plane spacing decreases, the peak amplitude of the voltage disturbance at Port 2 decreases. (This is consistent with the power bus impedance being proportional to d, as shown in Equation (3) and Port 2 voltage being the product of the power bus transfer impedance and current in Port 1.) The early time peak voltage is nearly linear (proportional) with plane spacing, d. This is consistent with the power bus impedance increasing as plane spacing increases, as seen in (3). Decreasing plane spacing has a dramatic effect on the voltage at Port 2. Decreasing the plane spac-

ing from 40 mils to 10 mils (a x4 reduction) reduces the peak voltage at Port 2 by 74%. Reducing the plane spacing further to 5 mils (x2 reduction) reduces the peak voltage at Port 2 by another 51%. Further decreasing the plane spacing to 1 mil (x4 reduction) reduces the peak voltage at Port 2 by yet another 82%.

Figure 7 illustrates the Port 1 voltage (driving point voltage) for the different plane spacings. Port 1 voltages are akin to a self-induced interference voltage at Port 1 from a current disturbance at Port 1. The Port 1 voltages are almost 800% larger than Port 2 voltages at their largest, but they also vary nearly proportionally to plane spacing. The voltages at Port 1 for different plane spacings are aligned in time, as was the case with Port 2 and they do not exhibit the time delay that is seen at Port 2. The percentage decreases in Port 1 voltage due to decreasing plane spacing tracks the decreases seen at Port 2. For instance, when shrinking the plane spacing from 40 to 10 mils, the peak Port 1 voltage shrinks by 74%, a number almost identical to that seen at Port 2.

Decreasing the dielectric thickness between the power and ground planes linearly decreases the power bus impedance (meaning less noise generated) at both low and high frequencies, and significantly reduce power bus noise voltage both at the driven and the transmitted ports. It is to be expected that this reduced power bus noise voltage (often referred to as ripple in the design process) will reduce EMI that may be radiated from the power bus.

The second design method for reducing power bus impedance and voltage ripple is the increase in relative dielectric constant, ϵr. The effect on power bus impedance that results from changing the dielectric constant between the planes in the power bus can be seen from Figure 8 which illustrates the changes in $|Z_{11}|$ that result from altering the value of dielectric constant, but maintaining a fixed plane spacing. The values of the plane conductivity and the loss tangent of the dielectric material is the same as in the examples of varying plane spacing. The resonant frequencies and the impedance shift lower as dielectric constant is increased. The value of the lowest resonant frequency (lumped element resonance) in $|Z_{11}|$ is inversely proportional to $\sqrt{\epsilon r}$. The value of impedance at frequencies below this first resonance is inversely proportional to the value of dielectric constant, as seen in (3). In addition, the higher dielectric constant material slows the propagation velocity of electromagnetic waves, so it has the effect of increasing the electrical dimensions of the planes. Thus, distributed resonant frequencies are lowered, thereby reducing the frequency band for effective decoupling. This side effect may not be desirable in that power bus resonant frequencies may be shifted into regions of the spectra of signals or into frequencies that find an easy path for radiation due to system configuration. For brevity, $|Z_{21}|$ is not displayed, but it also is reduced as dielectric constant is increased, as indicated by (3).

The effect of changes in the dielectric constant also has an effect on the time response of the voltage at Port 2, as is seen in Figure 9. This shows time delays at Port 2 relative to the excitation at Port 1, which are 0.95, 1.51, and 2.55 ns, respectively, as the value of dielectric constant moves from 2 to 8 to 32, respectively. These time delays reflect the decreasing speed of propagation in the material as the value of dielectric constant increases. The early time voltage peaks at Port 2 are higher for

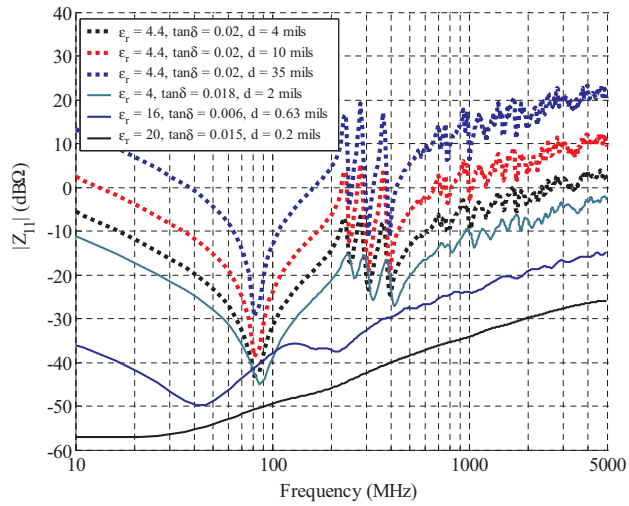

Figure 16: The driving point impedance, $|Z_{11}|$, of the representative commercially available classes of PCB materials from Table 1.

Table 1: Representative PCB laminate materials properties of classes of materials appropriate for decoupling applications. The material properties are used in the impedance plots in Figure 16.

Dk	Loss Tangent	Thickness, d	Comment
4.4	0.02	4, 10, 35 mils	better quality fiberglass/ epoxy resin material
4	0.02	2 mils	patented thin FR4 core, widely used.
16	0.006	16 microns (0.63 mils)	ultra-thin material commercially available
20	0.015	0.2 mils	ultra-thin material from [11, 12].

lower dielectric constant materials than for higher dielectric constant materials. This is consistent with the notion that the higher dielectric constant materials provide lower impedance, better decoupling, and a lower voltage disturbance at Port 2. The early time peaks are not linearly related to dielectric constant and are seen to have amplitudes in the same general ranges as seen in Figure 6. As the dielectric constant is quadrupled in value from 2 to 8, the peak early time voltage at Port 2 is decreased by slightly less than 40%. As the dielectric constant is again quadrupled from 8 to 32, the peak voltage at Port 2 decreases by a little more than 40%.

Figure 10 shows the voltage at Port 1, the driven port, for

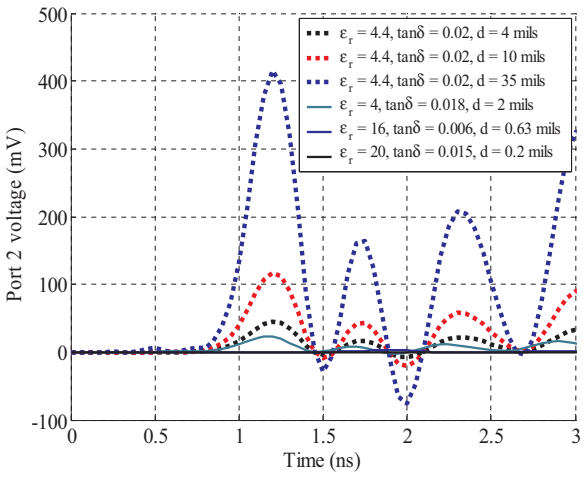

Figure 17: Port 2 voltages for the cases of the representative commercially available classes of PCB materials from Table 1.

the same values of thickness and dielectric constant shown in Figure 9. The voltage at Port 1 begins to rise immediately, reflecting that the voltage is calculated at the same point as the disturbance. The peak values of the voltage waveform are measured in thousands of mV, rather than hundreds of mV reflecting the much larger overall amplitude of the voltages at Port 1. Yet, as the value of dielectric constant is increased from 2 to 8 to 32, the reduction in peak voltage at Port 1 is only approximately 15% at each step.

The third design method for reducing power bus impedance and voltage ripple is the increase of dielectric loss (loss tangent, or tan δ) in the material of the power bus. Figure 11 shows results for varying loss tangent on the power bus input impedance, $|Z_{11}|$, while dielectric constant and plane spacing are held constant. The relative dielectric constant is 4.0, plane spacing is 40 mils, and copper plane conductivity is assumed. There is little change in the power bus impedance, other than at resonant frequencies, since the dielectric constant does not change. From these figures, the impedance curves do not shift in amplitude; only the sharpness of the resonant peaks is changed (varying Q). The resonances above the lowest frequency resonance (lumped element resonance) are substantially attenuated.

Figure 12 shows the time domain voltage at Port 2 as a result of varying loss tangent. The curves for each of the loss tangent values are aligned again implying that the waveforms ring at the same frequency and there is no shift in resonant frequencies in the spectrum of the power bus impedance. Increased dielectric loss results in high frequency filtering (low pass). The peak amplitude is largest when the loss tangent is smallest (low loss) and the duration of the ringing is longer. The peak voltage at Port 2 varies approximately 25% as the loss tangent varies by a factor of 10 (0.2 to 0.02). Figure 13 shows Port 1 voltage as loss tangent is varied. There is very little change in the peak voltage disturbance at Port 1 as dielectric loss is varied. Decoupling noise suppression benefits from increased dielectric loss in the power bus, but not as greatly as with variations in plane spacing or dielectric constant.

If materials with increased dielectric loss are used in the signal areas of the PCB, the result may not be desirable. The high frequency filtering effect of the increased loss may filter high-frequency spectral content from the signal, rounding edges of signal pulses or slowing rise-times.

Loss in the power bus actually has two components, dielectric loss in the material between the planes and resistive loss from current flowing in the planes themselves. The determination of which type of loss is dominant in a specific power bus depends on the plane spacing, d. Thin and ultra-thin dielectric layers between planes can effectively damp all resonant peaks, even though there is very little dielectric material present. This is due to the increase of the skin-effect losses due to the decreased spacing between the power and ground planes. With the decreased spacing, the field intensity between the power and ground planes increases, provided that the voltage applied between the planes is constant. Hence, the tangential H-field (surface currents) on the conductor surfaces increases. This increases resistive (skin-effect) losses, which in turn reduce the power bus impedance. Figure 14 shows the ratio of dielectric loss vs. resistive loss in a single plane pair power bus of various thicknesses. For values of the ratio greater than unity, dielectric losses are dominant. For values less than unity, resistive losses are dominant. The trend shows that for a power bus thickness greater than 10 mils, the dielectric loss is much greater than the conduction loss for frequencies higher than a few hundred MHz.

Increasing the skin-effect losses by using an embedded thin or ultra-thin capacitance material is a superior way to achieve power bus design objectives. However, mechanically there are a few issues associated with the decreased spacing between the power and ground planes, such as power/ground shorts, material breakdown, as well as some reliability concerns. Board assembly may require additional or special processes/handling in order to achieve necessary yields. Nevertheless, with the continuous advance of the technology, it is very promising that the embedded capacitance should become a practical, effective solution to obtain low power-bus impedance at GHz frequencies.

III. DESIGN IMPLICATIONS

The effects of varying power bus plane spacing, dielectric constant and dielectric loss on power bus impedance and voltage disturbance levels are examined in detail in the previous section. The EMC performance of a power/ground plane pair is improved when impedance and voltage disturbance levels are kept low. Reducing the spacing between power and ground planes is a very effective means of accomplishing improved EMC performance without altering electrical characteristics, such as power bus resonant frequencies. Increasing the dielectric constant of the material between the planes can lower the power bus impedance, but more so for frequencies below the lumped element resonant frequency than above and more so for transmitted noise voltages than for noise voltage disturbances built up at the source. A potentially unattractive side effect of increasing dielectric constant between the planes of a power bus is that the electrical dimensions of the power bus are enlarged and power bus resonances occur at lower frequencies than before. Conceivably, signal frequencies could lie within the band of power bus resonant frequencies possible causing distortion of the signal waveform and resulting bit errors. Increasing dielectric loss between the planes does reduce high frequency resonances, but is only marginally effective in reducing transmitted noise disturbances. This is not a commonly

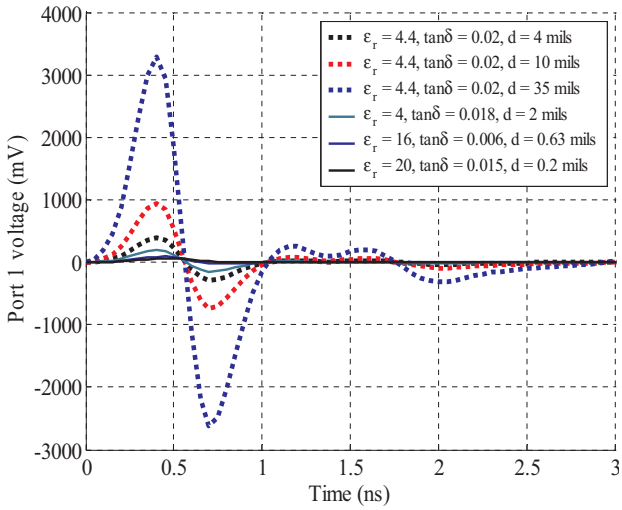

Figure 18: Port 1 voltages for the cases of the representative commercially available classes of PCB materials from Table 1.

applied method for enhancing power bus decoupling.

Materials designers sometimes focus on increased dielectric constant as a goal for the development of new dielectric materials to appeal decoupling applications. This may be a manifestation of a lack of understanding of the overall result of increased dielectric constants. New materials sometimes offer increased ability to sustain thin power bus separations and it is the separation that can be more important than the increased dielectric constant.

PCB designers sometimes think that the thickness of the copper planes affects decoupling effectiveness. At first glance, it might seem that thicker metal planes provide lower inductance, therefore improving the decoupling performance. Certainly thicker metal planes provide lower resistance at dc. However, as frequency increases, the current is restricted to a small portion of the total metal thickness due to skin effect. The skin depth is defined by:

$$\delta_S = \frac{1}{\sqrt{f\pi\mu\sigma}} \qquad (5)$$

where σ is the conductivity of the metal, μ is permeability, and f is frequency.

From Equation (5), as frequency increases, the skin depth decreases. Figure 15 shows the skin depth varies with frequency and compares this depth to typical PCB plane thicknesses. When frequency rises as high as 4 MHz, the skin depth is the same as the thickness of 1 oz copper. By the time frequency rises to 100 MHz, the current uses only about one-quarter mil of copper. Therefore, if the copper plane thickness were increased in thickness from 1 oz copper to 2 oz copper, there will be no change to the decoupling performance of the planes. Note that the formulation in (3) assumes that plane thickness is greater than skin depth.

Table 1 lists some representative values of commercially available PCB laminate materials that are appropriate for use in decoupling applications. These sets of material properties were selected to represent commonly available materials and also some special materials that may not be in common use, but

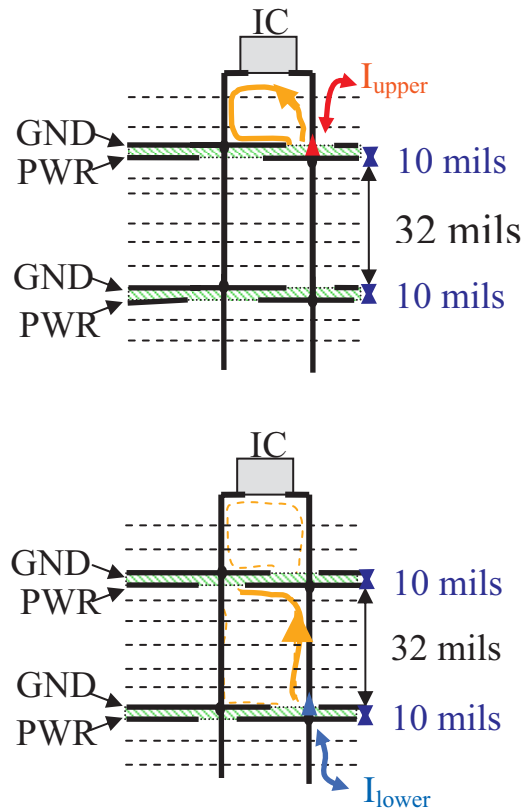

Figure 19: Multiple power bus structures in a PCB stackup that provide the same dc voltage level may not provide the same amount of current to the IC during initial switching period because of differences in the inductances of the current paths. (Displacement currents are not shown.)

which are commercially available. An effort was made to select material properties that are representative of classes of materials, rather than to attempt to present every possible set of material properties. Figure 16 shows the power bus impedances $|Z_{11}|$ for some representative values of commercially available dielectric thicknesses, dielectric constant, and loss tangent (using the geometry of Figure 2). Clearly the materials with high dielectric constant, especially with their typically very thin thickness, provide the best (lowest) impedance. The 2 mil thick material with a dielectric constant of 4 is representative of the patented process of forming very thin FR-4 cores that do not suffer shorting. This class of material is widely available and is even available in cores thinner than 2 mils. The ultra-thin materials exhibit very low impedances along with weak to non-existent resonances as losses are dominantly resistive, rather than loss in the dielectric (Figure 14) [11]. These ultra-thin materials present manufacturing challenges to provide processes for use that offer acceptable yields for the finished boards and also avoids electrical shorts between the ultra-close copper planes. These challenges have been met in the sense that ultra-thin core materials are available from more than a single manufacturer.

Figures 17 and 18 show the time domain noise voltages at Port 2 and Port 1, respectively, for the dielectric materials and thicknesses for the same simulation conditions from Figure 16 and Table 1. The high dielectric constant materials that are accompanied by very thin power bus thicknesses have noise levels

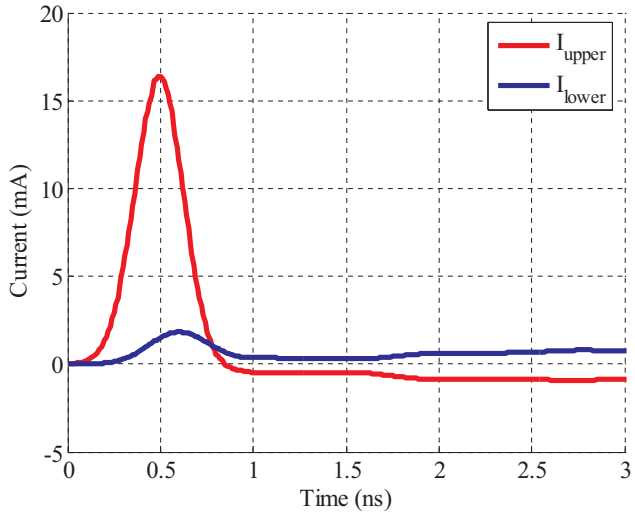

Figure 20: When a decoupling capacitor is connected to two power bus structures within a PCB, more current is drawn from the plane pair whose interconnection path provides the lower inductance (I_1) than from the plane pair that has the higher inductance interconnection (I_3).

that are not even visible compared to the typical FR-4 materials.

Another consideration is the use of multiple plane pair to provide the same dc voltage level. This is sometimes done in PCB design to reduce the dc resistance for power delivery, i.e., to attempt to provide more charge with less voltage drop. Naturally, there are many different possible configurations for multiple sets of power/ground planes, but Figure 19 shows an example with two power bus plane pair providing the same dc voltage to the IC. The connection inductance between the IC and the planes has a large effect on the decoupling performance of planes at high frequencies [2]. Clearly, the IC, when connected to the upper plane pair experiences a lower loop inductance than when connected to the lower plane pair. The ratio of these loop inductances provides a quick indication of the relative effectiveness of the lower plane pair in supplying high frequency current (current available immediately after switching). Figure 20 shows the relative current (calculated with the cavity model) that can be drawn from each set of power bus structures for a specific example, consistent with the 62 mil finished thickness geometries used in this paper (10 x 12 inch PCB, 10 mil power bus cores, 32 mils separating the power buses, relative dielectric constant of 4, copper conductivity, loss tangent of 0.02, and with the port at the same location as Port 2 in Figure 2. The peak current drawn from the lower plane pair is only 11% of the peak current drawn from the upper plane pair. Therefore, adding a second power bus, even it is thin may not benefit high frequency, early time decoupling if the resulting interconnection inductance is high.

IV. CONCLUSIONS

In this third installment in the series of papers on PDN design and decoupling, the effects of the plane size, dielectric constant, and dielectric thickness on the PDN impedance and voltage ripple are examined. The size of the planes determines the lowest frequency at which the cavity mode resonates, above which distributed behavior dominates the PDN impedance and its decoupling performance. The larger the planes, the lower the lowest distributed resonant frequency.

The single most effective design technique for lowering power bus impedance and voltage ripple is to decrease the spacing of the power/ground planes in the power bus. Decreasing the plane spacing from 40 to 10 mils is shown to decrease power bus impedance by greater than 10 dB (Figure 4). There are no electrical side effects associated with changing plane spacing. Very thin dielectrics reduce both the PDN impedance, and greatly dampen the high frequency distributed mode resonances. Reducing power bus plane spacing can mean PCB stack-up changes and the use of more expensive cores. On the other hand, reducing power bus plane spacing can offer the opportunity for more signal layers. A deleterious side effect of thin plane spacings between power and ground can be unintended electrical short circuits (shorting due to copper plane surface irregularities). Prevention of unintended electrical short circuits on planes that are closely spaced is a manufacturing process issue that has usually been solved by the time closely spaced planes are commercially available, usually as a PCB core material.

The second best means of reducing power bus impedance and voltage ripple is to increase the dielectric constant of the material in the power bus. Higher dielectric constant improves PDN performance by lowering the impedance between the planes. Increasing the dielectric constant by a factor of four results in lowering the PDN impedance by approximately 12 dB for frequencies lower than the lumped resonant frequency. While the first distributed mode resonant frequency is lower for higher dielectric constants, the maximum impedance of these resonances is lower by 6-10 dB (Figure 8). The undesirable side effect of raising dielectric constant is the downward frequency shift of power bus resonances. The design ramification of this is that resonant frequencies may be shifted into regions that overlap signal spectra possibly causing signal distortion and bit errors. There are limited sets of materials that are available in dielectric constants higher than 4.0 that are available in a multitude of thicknesses and are intended for use in the PDN. (There are a number with dielectric constants lower than 4.0, but these are usually intended for use in signal layers, not in the power bus.)

When thin dielectrics and high dielectric constant can be combined, even better performance is obtained. Naturally, the connection to the PDN must be a low inductance connection to realize these benefits.

The use of lossy dielectric material in the power bus is of limited utility in isolation because the resulting reductions in power bus impedance and voltage ripple are small, except for specific resonant frequencies. However, the use of all three design methods together provides the best enhancement of decoupling. Perception and design rules are relative. In the microwave signaling community, FR-4 PCB material with a loss tangent of 0.02 is considered extremely lossy as it is without the consideration of adding additional loss. In that application with the use of extremely low loss dielectrics, signal losses are always dominated by skin effect resistive losses, not dielectric losses.

The next paper in this decoupling series will address the source of the noise in the PDN. The first three papers have dis-

cussed the performance of the physical structure without discussing what the impedance/noise goal should be for this structure. In order to know what target impedance to design for, we must have an understanding of the amount of noise created by the IC. Naturally, this is a very complex question, and to get a 'perfect' answer requires detailed knowledge of the inner workings of the IC. This kind of detail is seldom available to us, so some reasonable assumptions allow good engineering estimates.

V. REFERENCES

1. Knighten, J., B. Archambeault, J. Fan, G. Selli, S. Connor, J. Drewniak, "PDN Design Strategies: I. Ceramic SMT Decoupling Capacitors – What Values Should I Choose?," IEEE EMC Society Newsletter, Issue No. 207, Fall 2005, pp. 46-53.
2. Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," IEEE EMC Society Newsletter, Issue No. 208, Winter 2006, pp. 56-67.
3. Fan, J., J. Knighten, N. Smith, R. Alexander, "The Effects of Reference Capacitors on Signal Transmission through Single-Ended Traces in Multi-Layer PCBs," 2003 IEEE International Symposium on Electromagnetic Compatibility, Boston MA, August 18-22, 2003, pp. 690-694.
4. Pozar, David M., Microwave Engineering, 2nd Ed, Wiley, 1998.
5. Lo, Y., D. Solomon, W. Richards, "Theory and experiment on microstrip antennas," IEEE Trans. Antennas and Propagation, vol. 27, pp. 137-145, March 1979.
6. T. Okoshi and T. Miyodhi, "The planar circuit – an approach to microwave integrated circuitry," IEEE Trans. Microwave Theory and Technique, Vol. 20, No. 4, April 1972, pp. 245 – 252.
7. G.T. Lei, R.W. Techentin, R.P. Hayes, D.J. Schwab, and B.K.Gilbert," Wave model to the Ground/Power Plane Noise Problem," IEEE Transactions on Instrumentations and Measurements, Vol.44, No.2, April 1995, pp. 300-303.
8. N. Na, J. Choi, S. Chun, M. Swaminatham, and J. Srinivasan, "Modeling and transient Simulation of planes in electronic packages," IEEE Transactions on Advanced Packaging, Vol. 23, No. 3, Aug. 2000, pp. 340- 352.
9. C. Wang, J. Mao, G. Selli, S. Luan, L. Zhang, J. Fan, D. J. Pommerenke, R. E. DuBroff, and J. L. Drewniak, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductance," IEEE Trans. Advanced Packaging, Vol. 29, No. 2, May 2006.
10. EZ-PowerPlane, http://www.ems-plus.com/.
11. "Embedded decoupling capacitance (edc) project—Final Report," National Center for Manufacturing Sciences, Ann Arbor, MI, Final Rep. 0091RE00, 2000
12. Xu, M., T. Hubing, J. Chen, T. Van Doren, J. Drewniak, R. DuBroff, "Power-Bus Decoupling With Embedded Capacitance in Printed Circuit Board Design," IEEE Trans. Electromagnetic Compatibility, Vol. 45, No.1, February 2003, pp. 22-30.

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Photonic Crystal Power Substrate for Wideband Suppression of Power/Ground Bounce Noise and Radiated Emission in High-speed Packages

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Abstract — In this work, we demonstrated a novel electromagnetic bandgap (EBG) design for the substrate of the power delivery network (PDN) to suppress the propagation of the ground bounce noise (GBN) or the simultaneous switching noise (SSN) and radiated emissions in high-speed digital package substrates. Two layers package substrates were fabricated with keeping power/ground planes solid and embedded several high dielectric constant (High-DK) rods in the substrate. The noise suppression performance and the electromagnetic interference (EMI) reduction capability were simulated and measured for the proposed design. Good agreement is seen.

Index Terms — electromagnetic bandgap (EBG), power delivery network (PDN), simultaneous switching noise (SSN), electromagnetic interference (EMI).

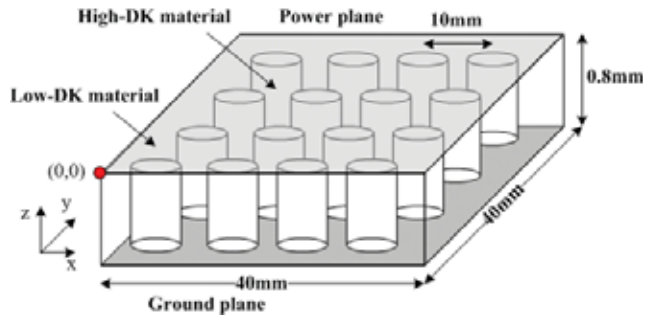
I. INTRODUCTION

With the fast edge rates, high clock frequency and low voltage level for high-speed circuits, simultaneous switching noise (SSN) on the power delivery network (PDN) become the most important factors to determine the system performance. The resonance modes of the parallel-plate waveguide can be excited by SSN and cause serious signal integrity (SI) and electromagnetic interference (EMI) problems [1]-[2].

Several researches have been proposed to suppress the SSN coupling. Adding decoupling capacitors between the power and ground planes is a traditional method to suppress SSN and EMI, but they are effective at higher frequency ranges due to the equivalent series inductance (ESL). Recently, various forms of electromagnetic bandgap (EBG) structures have been proposed to suppress SSN and EMI [3]-[5]. Most of these EBG structures were etched some patterns periodically on the metal layer of the PDN and may cause some signal integrity problems.

In this work, we proposed a novel EBG substrate with embedding several high-DK rods in the substrate material but keeping the metal layer (power and ground) continuous. The photonic bandgap appear for this power substrate with excellent power noise suppression capability. The distinctive behavior of the EBG substrate both in broadband suppression of the SSN and EMI is validated by measurement and simulation.

II. DESIGN CONCEPT OF THE EBG SUBSTRATE



(a)

(b)

Fig. 1. (a) Schematic diagram of the proposed EBG structure. (b) The high-DK materials.

Fig. 1(a) shows geometry of the proposed EBG substrate. The dimension of this structure is 40mm by 40mm and the thickness is 0.8mm. The top and bottom layers of this structure are covered with copper completely. The material of the substrate is ROGERS RT/duroid 5870 ($\epsilon_r = 2.33$, tan $\delta = 0.0012$) and the dielectric constant of the high-DK material embedded in the substrate is 110. The radius of the high-DK rod is 2mm. These high-DK rods are embedded in ROGERS RT/duroid 5870 and the spacing between each rod is 10mm. The Fig. 1(b) shows the high-DK material. Measurement ports 1 and 2 are located at (16.5mm, 10mm) and (10mm, 15mm) of the test substrate and they places between power and ground planes. The original point (0, 0) is on the left corner of the EBG substrate as shown in Fig. 1(a).

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Broadband SSN suppression

Fig. 2 shows the measured and simulated |S21| for the designed EBG substrate. The insertion loss of the reference board is also presented in this figure for comparison. The EM tool ANSOFT HFSS is used to simulate the SSN behavior of this structure. Compared with the reference board, it is clearly seen that the EBG substrate behaves highly efficient SSN suppression in a broadband range from about 2.8 GHz to 5 GHz and 5.7 GHz to 7.6 GHz. The bandwidth is defined by the insertion loss lower than -25 dB. Within the first stopband, the proposed power substrate achieve averagely over 30 dB of noise suppression. Fig 3 shows the dispersion diagram of this EBG substrate and there are two band gaps. The band characteristic is scanned along the edge of the Brillouin zone, which represents the irreducible value of the propagation vectors in the lattice. It is clearly seen that the stopband regions in the band structure diagram are consistent with those shown in Fig. 2.

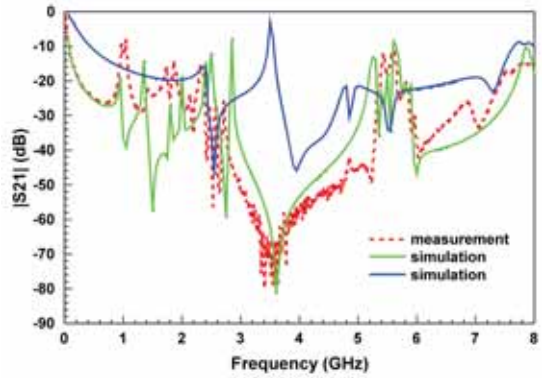


Fig. 2. Comparison of |S21| between the EBG substrate and the reference board by HFSS simulation and the measurement.

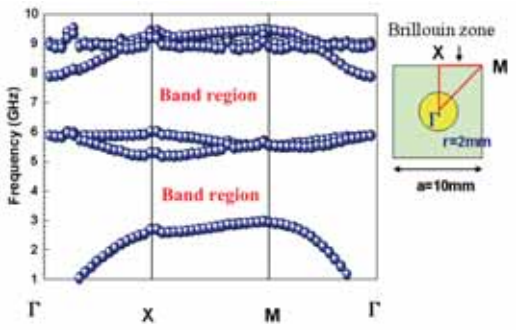


Fig. 3. The dispersion diagram for the high-DK rods with a 2mm radius in a square lattice in a duriod host with a period of 10mm.

B. Radiation suppression

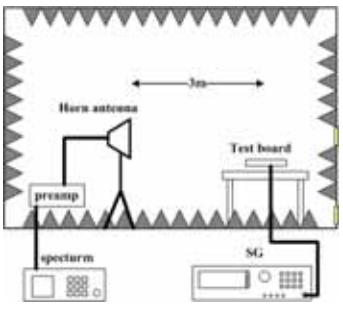


Fig. 4. Measurement setup for EMI in 3m fully anechoic chamber.

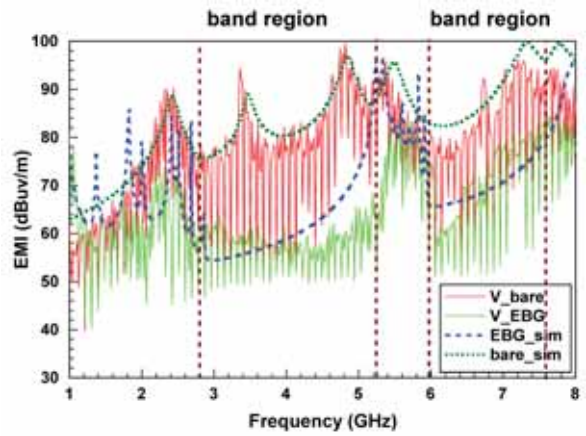


Fig. 5. Simulated and measured EMI radiation at 3m for the EBG substrate.

Low radiation is important in high-speed circuits for the compliance of the strict electromagnetic compatibility (EMC) regulations. We investigate the EMI performance of the proposed EBG substrate by comparing with the reference board.

Fig. 4 shows the EMI measurement setup in an EMC fully anechoic chamber. The test board is put on the wooden table, and the RF signal of 0dBm generated by the signal source (Anritsu 68147C) is launched into power plane of the board through SMA connector. The radiated E-file is measured by hone antenna (R&S HF906) and the distance between the test board and the antenna is fixed at 3m. The maximum radiated E-field is recorded by the spectrum analyzer (R&S FSP) with 100kHz resolution bandwidth. The simulation for the E-field radiation is modeled by ANSOFT HFSS.

Fig. 5 shows the simulated and measured EMI radiation at 3m distance for the EBG substrate. It is seen that the agreement between the measurement and the simulation is resonance good. At the frequency range of the band gap, the radiation resulted from the SSN is significantly suppressed with over 30dB reduction. This design is quite helpful for low EMI package in high-speed circuits.

V. CONCLUSION

A novel EBG substrate design using high-DK material embedded in the low-DK substrate is proposed to suppress the SSN in the high-speed circuits. The performance of efficient and wideband noise suppression is theoretically and experiment demonstrated in this paper. In addition, the proposed design performs low radiation emission resulted from the SSN at the designed stopband. It has been shown that the EBG substrate behaves two stop bands to suppress SSN and EMI.

REFERENCES

[1] T. L. Wu, Y. H. Lin, J. N. Hwang, J. J. Lin, "The effect of test system impedance on measurements of ground bounce in printed circuit boards," IEEE Transactions on Electromagnetic Compatibility, vol. 43, May 2001, pp. 600-607.

[2] G. Lei, R. W. Techentin, and B. K. Bilbert, "High-frequency characterization of power/ground-plane structures," IEEE Transactions on Microwave Theory Tech-

niques, vol. 47, pp. 562–569, May 1999.
[3] T. Kamgaing, and O. M. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface," IEEE Microwave and Wireless Components Letters, vol. 13 no. 1 pp. 21-23, January 2003.
[4] T. L. Wu, Y. H. Lin, and S. T. Chen, "A Novel Power Planes With Low Radiation and Broadband Suppression of Ground Bounce Noise Using Photonic Bandgap Structures," IEEE Microwave and Wireless Components Letters, vol. 14, no. 7, pp. 337-339, Jul. 2004.
[5] S. Shahparnia, O. M. Ramahi, "Electromagnetic interference (EMI) reduction from printed circuit boards (PCB) using electromagnetic bandgap structures," IEEE Transactions on Electromagnetic Compatibility, vol. 46, November 2004, pp. 580-587.

Biographies

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Consultants Network

Professor Bob Olsen was an invited speaker at the EMC Mexico 2006 seminar in Mexico City on June 27-28. Held at the new conference facilities at the Unidad Politecnica para el Desarrollo de la Competitividad Empresarial (UPDECE) at IPN, this event was a catalyst for activity to launch a new EMC Chapter in Mexico. Professor Olsen gave two presentations "BPL Communications: EMI/EMC Aspects" and "Evaluation of RF Measurement Instruments in Strong ELF Electric Fields" which were very well received by the local IEEE members and guests. There were several good papers presented at the two day seminar. Professor Olsen may just select one for inclusion in a future edition of the EMC Newsletter!