SOT-MRAM : an ultra-fast, infinitely endurant, non-volatile Memory.

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Merging memory and logic into the so-called logic-in-memory architecture is a long-awaited objective of the IT industry. It would improve both data bandwidth and latency, as logic and storage are closer to each other. Moreover it would naturally solve one of the major roadblocks for this industry, which is the energy cost of transferring data between the memory and the processor (the energy spent to send or receive data from/to an external DRAM memory is already three orders of magnitude higher than the one used to perform a double precision floating-point operation [1]).

The development of an electrically addressable Non-Volatile Memory (NVM) combining processor clock speed and infinite endurance is essential for fusing logic and memory together. Amongst the many emerging non-volatile memory technologies, STT-MRAM has been identified as one of the most promising candidate: it combines CMOS compatibility, high retention time and large endurance. However, its writing time (down to 4 ns for reliable switching in perpendicular STT-MRAM) is still too long.

Recently, we have proposed a novel memory concept, named Spin-Orbit Torque-MRAM (SOT-MRAM) [2,3,4] that combines the STT advantages with a writing speed in the deep sub-ns regime [5] (compatible with the processor multi-GHz frequency). Moreover, as the writing current is now flowing beneath the cell and not through the memory dot, read and write paths are decoupled: a truly infinite endurance is expected as no voltage stress is applied on the thin insulating layer; and the read speed and process margin are improved. Finally, we propose an integrable and scalable solution for sub-ns field free switching.

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