Session Topic 1 -- Nanoelectronics and Nanodevices

Chairs: Nafiz Karabudak, Lockheed Martin
Dwight Woolard, Army Research Office

TUESDAY, Salon C

Paper ID	Time	Title	Authors & Affiliations
PID 596495	10:00 - 10:30	*A Novel Three Dimensional Field Effect Transistor based on Single-Walled Carbon Nanotubes*	Selvapraba Selvarasah, Northeastern University, USA; Prashanth Makaram, Northeastern University, USA; Chia-Ling Chen, Northeastern University, USA; Huiyan Pan, Northeastern University, USA; Ahmed Busnaina, Northeastern University, USA; and Mehmet Dokmeci, Northeastern University, USA
PID 583956	10:30 - 11:00	*Heating Effects in Dual-Gate Devices*	Stephen Goodnick, Arizona State University, USA; Katerina Raleva, University Ss. Cyril Methodius, Skopje, Republic of Macedonia; and Dragica Vasileska, Arizona State University, USA
PID 545911 PID 596522	11:00 - 11:30	*Modeling of high-k gate stack of tunnel barrier in nonvolatile memory MOS structures*	Wei Wang, Southeast University, China; J. P. Sun, University of Michigan, USA; Toru Toyabe, Toyo University, Japan; Ning Gu, Southeast University, China; and Pinaki Mazumder, University of Michigan, USA
PID 555809	11:30 - 12:00	*Focused Ion Beam Fabrication of Sub-20nm Inter-electrode Gaps for Room Temperature Operating Single Electron Transistor*	Manoranjan Acharya, Michigan Technological University, USA; P. Santosh Kumar Karre, Michigan Technological University, USA; and Paul L. Bergstrom, Michigan Technological University, USA
	12:00 - 2:00	***Lunch***	
	2:00 - 2:15	***Poster Session***	
PID 596158	2:15 -- 2:45	*Effect of Temperature Variation on Gate Tunneling Currents in Nanoscale MOSFETs*	Garima Joshi, UIET, Panjab University, Chandigarh, India; D.N Singh, UIET, Panjab University, Chandigarh, India; and Sharmelee Thangjam, UIET, Panjab University, Chandigarh, India
	2:45 - 3:00	***Break***	
PID 553301	3:00 - 3:30	*Analyzing N-Curve Metrics for Sub-threshold 65nm CMOS SRAM*	Mamatha Samson, International Institute of Information Technology, India; and Srinivas M.B, International Institute of Information Technology, India
PID 594544	3:30 - 4:00	*Modulation of Coulomb Blockade Behavior of Room Temperature Operational Single Electron Transistors by Tunnel Junction*	P. Santosh Kumar Karre, Michigan Technological University, USA; Aditya Kapoor, Michigan Technological University, USA; Govind Mallick, US Army Research Laboratory , USA; Shashi P. Karna, US Army Research Laboratory , USA; and Paul L. Bergstrom, Michigan Technological University, USA
Poster Session on Tuesday (2:00 - 2:15)			
PID 543943	Poster	*Design Methodology for Electron-Trap Memory Cells*	Bingxi Li, University of Windsor, Canada; and Chunhong Chen, University of Windsor, Canada
PID 551891	Poster	*Molecular and Biomolecular Processing: Three-Dimensional-Topology Processing and Memory Cells*	Marina Lyshevski, Microsystems and Nanotechnologies, USA; and Sergey Lyshevski, RIT, USA
PID 595875	Poster	*Effects of Random Distribution of Dopants in Nano-Scaled MOSFETs*	Vijay Lamba, Haryana College of Technology & Management, India; and Derick Engles, GNDU Amritsar, India